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A 126 μW Readout circuit in 65nm CMOS with Successive Approximation Based Thresholding for Domain Wall Magnet Based Random Number Generator

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***Abstract*—We present a novel readout circuit for a ferromagnetic Hall cross-bar based random number generator. The random orientation of magnetic domains are result of anomalous Hall-effect. These ferromagnetic Hall cross-bar structures can be integrated with the read out circuit to form a plug and play random number generator. The system can resolve up to 15–20 μV Hall-voltages from Hall probe. Application of current densities around $10^{12}A/m^2$ through the Ferromagnetic Hall cross-bar produces random Hall-voltage on the output terminals. To amplify the weak Hall-voltages (10–100 μV) in the presence of DC offsets, a modulation scheme is used to up-convert the signal and a band-pass amplifier is used to amplify the modulated signal. The band-pass amplifier circuit, motivated by neural recording amplifier is designed in 65nm CMOS and consumes 126 μW of power from a 1.2 V supply. Further, we present a successive approximation algorithm and its embedded implementation to set the desired threshold for digitizing the amplified Hall-voltage in presence of signal drift. Experimental results show that the resulting system can tolerate drifts in voltage up to 440 μV.**

I. Introduction

Random bit streams find application in generating keys in cryptography and initialization of parameters in a encrypted communication protocols. Random number generators are useful in realising Physically Unclonable Function (PUF) in microprocessors [1], [2]. These streams are also useful in stochastic simulations, gaming and events where random sampling is required. Random number generators can be divided into two classes based on their source, namely true random number generator (TRNG) and pseudo random number generator (PRNG). TRNG generates randomness from inherent stochastic physical feature of the source. On the other hand PRNG generates lengthy stream of digital bits which are difficult to predict. Most on-chip TRNG of present day use techniques like sampling of thermal noise [3] or exploiting meta stability of latching circuits [4]. Recently, magnetic random number generators (MRNG) have been proposed which can exploit the already existing MRAM (magnetoresistive random-access memory) technology.

In such MRNGs, switching probability of a magnetic tunnel junction (MTJ) is adjusted with injected current to obtain stochastic orientation of free layer of random numbers [5], [6]. However, reliable fabrication of MTJ based random number generators is quite difficult. MTJs are multilayered structures compared to perpendicular magnetic anisotropy (PMA) ferromagnetic Hall cross-bar (FHC). In addition, growth of oxide layer in MTJs is not straightforward and requires lots of optimizations. Current shunting through the oxide pinholes and side walls is a major issue in MTJ fabrication process. Tuning of tunnelling magnetoresistance (TMR) ratio of MTJs with existing CMOS technology is another big challenge. Hence, PMA FHC developed by [7], [8] is a strong candidate for implementation of TRNG. MTJs on the other hand have higher speed than conventional DRAM and much higher density than SRAM. This is the only non-volatile technology with nearly infinite endurance and require much lower write power as compared to Flash albeit at a lower density. The domain wall based devices combine all the advantages of MTJ along with the potential of realizing larger (100x) density (i.e., 3D architecture). But, the existing MTJs are complex to fabricate and suffer from tunnel barrier degradation. The only advantage is lower write-voltage operation, but it can be incorporated in our device by using the novel spin-orbit torque for writing. Moreover, in future generation of the device, it is indeed favorable to integrate the MTJ with our Hall device so that Hall-voltage will be enhanced due to TMR and reduce the dependence on external circuitry.

The FHC MRNG produces a low amplitude Hall-voltage in the range of 10–100 μV along with drift in signals over time. The offset voltage of differential amplifier and resistance of cross-bar Hall-sensor are important challenges for the readout circuit. In this work, we propose one such readout circuit that is inspired by the DC offset free amplifiers used in neural recording techniques [9], [10].

The rest of the paper is organized as follows. We present details of FHC and the challenges involved in detection of random bit in next Section. Section III discusses the architecture and details of the readout circuit for conversion of Hall-voltage to random bit. The section also describes the compensation algorithm used to provide resilience to

*Corresponding Author is Arindam Basu. Equal contribution of Govind and Joydeep. Financial support for this work was provided by Ministry of Education, Singapore through grant MOE2013-T2-2-017

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Manuscript received XXXX XX, 2019; revised XXXX XX, 2019.

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signal drift over time. Finally, we present the results from fabricated bandpass amplifier and illustrate the effectiveness of the proposed drift compensation algorithm in Section IV; and conclude the paper in the last Section.

II. Magnetic Random Number Generator

A magnetic true random number generator (TRNG) has been developed by utilizing the unique stochasticity behaviour of magnetization dynamics of a PMA structure as an entropy source. The fundamental driving arises from the spin-transfer torque [11] and spin-orbit torque phenomena [12]. The proposed devices comprise of ferromagnetic Hall cross-shaped structures as shown in Fig. 1 [7], [8]. The 500 nm wide nanowire is patterned using electron beam lithography and Ar ion-milling techniques. Two Ta(5 nm)/Cu(100 nm) electrodes (labelled A and B) are formed at both ends of the nanowire to flow current through the nanowire and generate local Oersted field. The thickness of the Hall plate is around 20 nm. Material composition of FHC is Ta/Pt/Co/Ni/Co/Ta, being sputtered on silicon coated with silicon dioxide. A pulse generator is connected at electrode A for injecting a pulsed current along the longitudinal wire, and the Hall probe is used to detect the change in magnetization in the nanowire. The utilized single Co/Ni layer film has lower crystalline anisotropy (K_u) as compared to conventional PMA films. The nanowire is ferromagnetic and can be magnetized by an external magnetic field. Due to this, the domains are aligned in one direction yielding a net magnetization. However, a current through the nanowire also produces a field which depends on the current and the distance from the wire. The application of in-plane pulsed current above a certain magnitude can nucleate and simultaneously drive the domain walls (DW) for which 200 Oe is sufficient in general. It should be mentioned that due to the weak perpendicular anisotropy of our system ($\approx 10^4$ ergs/cc), the thermal effects or Joule heating induced by nanosecond pulse of relatively large amplitude ($\approx$ 10 V) can destabilize the spins which are then free to take either up or down orientation leading to stochasticity, and this has been verified by testing for over 10^6 write pulses. However, at extreme temperatures ($>$350°C), the system might lose perpendicular anisotropy and become in-plane. The Hall resistance which is proportional to the perpendicular magnetization of the Hall cross junction, is estimated by measuring the voltage across the Hall probe while flowing a constant DC bias current between electrodes A and B. With each subsequent pulse, the DWs can annihilate or nucleate again thereby changing the Hall-voltage to different values.

Hall-voltage is read using the phenomenon of anomalous Hall effect (AHE) [8]. The presence of magnetic Hall probe creates a natural gradient of anisotropy and higher demagnetization energy at the four corners of the Hall cross-junction. The canted spins resulting due to the fringing field at the four corners are driven by spin transfer torque effect and are responsible for DW nucleation and propagation [7]. The nucleation process is stochastic due to competition between anisotropy and demagnetization energy which are also dependent on extrinsic device features. The stochastic nucleation of DWs are detected as random analog output voltage across the Hall probe. This Hall-voltage can be digitized and detected as a random signal. The addition of heavy metal leads to spin orbit torque (SOT) effect which aids in the DW nucleation process.

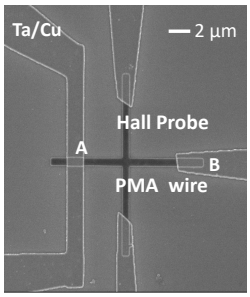

Fig. 1: SEM image of the fabricated ferromagnetic Hall cross-bar sensor [8].

TABLE I: Parameters of the cross-bar Hall sensor

Parameter	Value
Read current	100 μA
Write current resistance	1.5 kΩ
Write pulse amplitude	10 V
Nanowire width	500 nm
Cross-wire length	5 μm

The randomness is due to thermal effects enhanced by low anisotropy and enhanced demagnetization at the edges of the Hall cross. The domain walls look like dark and bright contrast in Kerr image [7]. As depicted in the full system diagram in Fig. 2, application of a sense current, I_{sense} would generate AHE resulting in output voltage V_{sense}. Representative device parameters for the FHC device are provided in Table I [7]. The device dimensions are related to imaging purposes as lower dimensions are not easy to resolve using conventional Kerr microscopy techniques. Moreover, it adds to higher demagnetization hence, randomness. Interested readers can refer to [8] for further details on the FHC sensor. Measurements of the AHE after each write pulse using digital multimeter have shown that it generates random differential-voltages in the range of $\pm$10–100 μV, but the absolute values of the high and low levels vary over time.

III. System Architecture

As described in the last section, the AHE voltages generated from the FHC device are in the range of tens of μV with a variation in common-mode level. Measurement of such small DC voltages presents several challenges to the circuit as described below. The offset present between the input terminals of a high gain DC coupled differential amplifier will saturate the output to high or low. The thermal noise of the circuit also makes it hard to resolve the random bit. The output resistance of the FHC is high (in kΩ). We next describe the special techniques implemented in the low-noise readout circuit (as in Fig. 2) to overcome the problems described earlier. The read or sense current I_{sense} is modulated with the help of a clock. This modulation moves the Hall sensor

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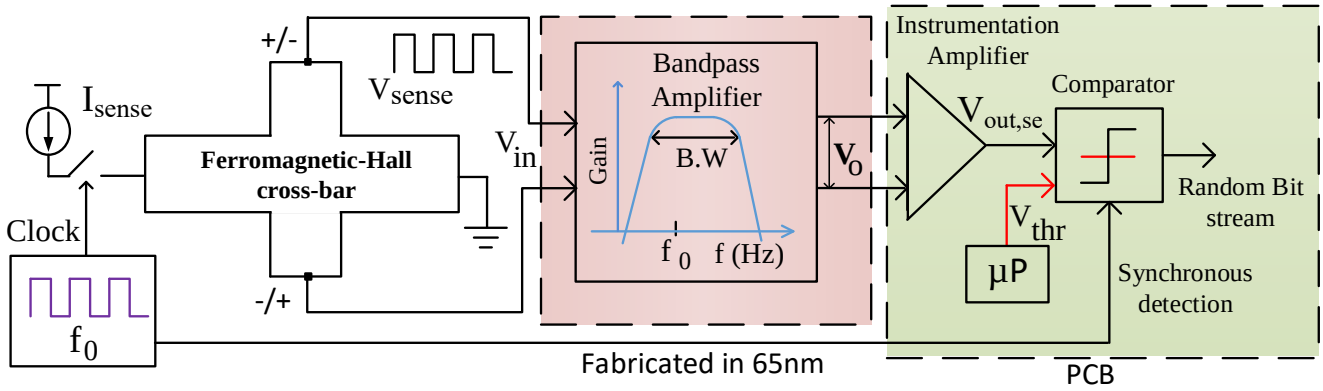

Fig. 2: The read current used for sensing the Hall-voltage is modulated by clock f_0. The modulated Hall sensor voltage is amplified to V_o by the bandpass amplifier thus reducing the effect of DC offset. The detection of random bit is done by comparing V_o with a programmable threshold V_{thr}. The comparator outputs can be latched with the help of the same falling/rising clock edge.

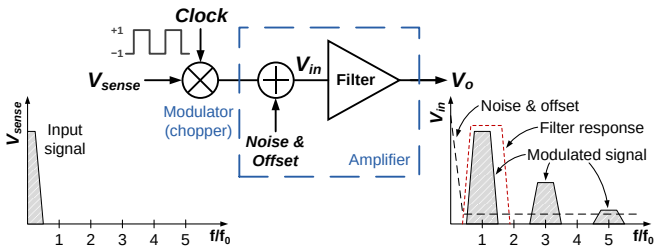

Fig. 3: The sensor signal V_{sense} is modulated by a clock of frequency f_0, and fed to the bandpass amplifier (filter).

output V_{sense} to a higher frequency band compared to the subsequent amplifier's input offset and flicker noise [13], thus mitigating the effect of the latter. A representative illustration of the modulation scheme is provided in Fig. 3, showing that the frequency up-translation can be achieved by multiplying the input signal with a clock waveform; while the bandpass response of the following amplifier filters out all undesirable spectral components. The write pulse source as required to be applied to the sensor (as in later Fig. 10) is not shown in Fig. 2 for simplicity.

A. Readout Amplifier

The first block in detection of V_{sense} is a differential low-noise bandpass amplifier. Although circuit noise from the amplifier can add to stochasticity of the generated bit, nonetheless, in this work, we wanted a readout circuit that would aid in characterizing the randomness in the FHC. Hence, noise generated from the circuit is required to be lowered. As discussed, the output voltage signal from the FHC is modulated to a higher frequency. In this regard, it should be emphasized that the proposed method is different from conventional chopping techniques (as in [14], [15]) in the sense that we do not need to chop back to baseband. Instead, we generate the output random bits at a rate equal to the modulation frequency. The filter has to be designed such that the modulating clock frequency f_0 will lie within the pass-band of the amplifier and the effect of input offset would be largely attenuated. In designing the amplifier, we exploit the fact that linearity is not important in this application. Hence, we take inspiration from neural recording amplifiers [9], [10], [16] which face similar challenges of amplifying small AC signals in the presence of DC offset. Fig. 4(a) depicts the topology of the fully differential bandpass amplifier as used in this work, constituted using two cascaded capacitive-feedback amplifier stages designed to provide an overall mid-band gain of 10,000.

To optimize the noise performance of the cascade, thermal noise floor for the first amplifier is kept low by using a large bias current to increase its transconductance (g_m') while the second stage is biased with a relatively lower current to limit its bandwidth and consequently, the total integrated thermal noise of the system [17]. Trying to limit the bandwidth in the first stage itself would require quite large capacitors thereby imposing severe area penalty. The two stage design thus provides a nice trade-off between noise performance, area and power requirement. The mid-band gain A_0 is set by the ratio of the capacitors as $A_0 = \frac{C_1'}{C_2'}\frac{C_1''}{C_2''}$, and the highpass corner f_l is defined by the C_2 capacitors and the value of the pseudoresistors R_f (realized using back-to-back connected PMOS transistors M_a, M_b and M_c, M_d biased in deep sub-threshold region). The low-pass corner f_h is given by $f_h = \frac{\beta g_m}{C_L}$ where g_m denotes transconductance of the constituent amplifiers, C_L is the corresponding output load capacitance, and β is defined as $C_2/(C_1 + C_2 + C_P)$ where C_P is the parasitic capacitance at the input of the transconductance amplifiers. The lower cut-off frequency of the bandpass amplifier can be adjusted using the bias voltage V_b of the pseudoresistors. Using s to denote complex frequency, the overall transfer function of the bandpass amplifier is given by the following expression:

$$\frac{V_o}{V_{in}} \approx \left(\frac{C_1'}{C_2'}\frac{-sC_2'R_f'}{(1+sC_2'R_f')(1+\frac{sC_L'}{\beta' g_m'})}\right)\times \left(\frac{C_1''}{C_2''}\frac{-sC_2''R_f''}{(1+sC_2''R_f'')(1+\frac{sC_L''}{\beta'' g_m''})}\right) \quad (1)$$

Large signal swings can cause the amplifier output to saturate due to non-linearity of pseudo resistors. However, this will

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Capacitor Values

Parameter	Value
C_L	0.85pF
$C_1^{'}$	10.0pF
$C_2^{'}$	100.0fF
$C_1^{''}$	5.0pF
$C_2^{''}$	50.0fF

Device size parameters

Name	W/L ratio
$M_{a,b,c,d}$	10/3
$M_{1,2}$	80/2
$M_{5,6,7,8}$	40/3
M_0	80/3
$M_{3,4}$	5/3
$M_{9,10}$	1.6/12

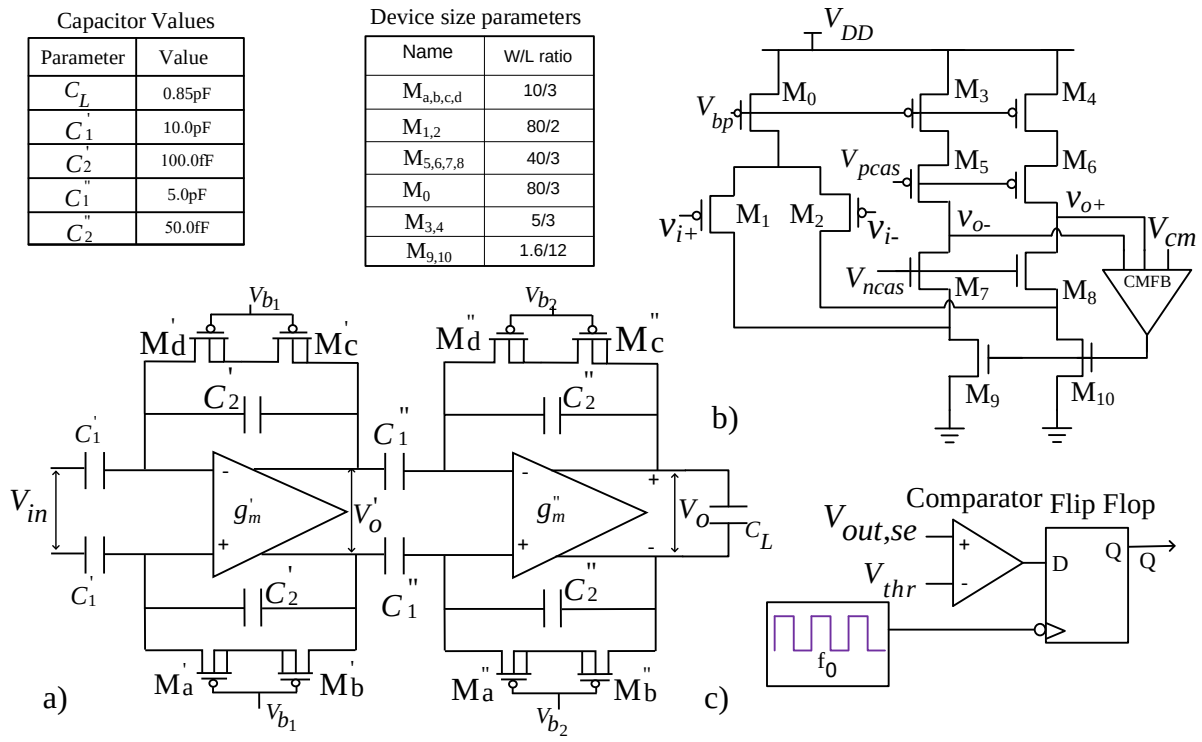

Fig. 4: Bandpass amplifier for Hall sensor. a) The input signal from the Hall sensor is applied to the bandpass amplifier made up of two cascaded capacitive-feedback amplifier stages. The pseudoresistors can be tuned to provide a lower cut-off frequency from 1 Hz to 2 kHz. b) Fully differential folded-cascode opamp with common mode feedback (CMFB) stabilization, as used in each of the stages. c) The differential output V_o from the bandpass amplifier is converted to a single ended signal $V_{out,se}$ by an instrumentation amplifier (off-chip in our case) and compared with a threshold V_{thr}. Latching of the comparator output at negative edge of clock will produce the random bit Q.

not cause trouble in the present application since we are only concerned with evaluation of single bit quantized version of the input signal. Schematic of the constituent transcondutance amplifiers is shown in Fig. 4(b). It is a fully differential folded cascode amplifier with load capacitance based compensation [18]. The transistor dimensions for the amplifier are provided in the inset within the figure.

The input referred noise power spectral density ($S_{v_n}^i$) of the bandpass amplifier can be derived as follows assuming noise due to the second stage is negligible:

$$S_{v_n}^i = \left(S_{v_n}^{A_1} \frac{1+(\omega R_f^{'}(C_1^{'}+C_2^{'}+C_P^{'}))^2}{1+(\omega R_f^{'} C_2^{'})^2} + \frac{8kTR_f^{'}}{1+(\omega R_f^{'} C_2^{'})^2} \right) \left(\frac{C_2^{'}}{C_1^{'}} \right)^2 \quad (2)$$

Transistor-level simulations of the bandpass amplifier has been performed using CMOS 65nm models. The values of bias current (i.e., through M_0 in Fig. 4(b)) are 8.1 and 6.2 μA for the two successive stages respectively. The mid-band gain obtained from simulation is about 80 dB. Theoretically calculated value of $S_{v_n}^i$ (at $\approx$ 3 kHz) is 22 nV/$\sqrt{Hz}$ while neglecting the effect of Flicker noise. The simulated output noise PSD at 3 kHz is 296 μV/$\sqrt{Hz}$ which when referred back to the input by dividing by the gain yields 29.6 nV/$\sqrt{Hz}$. Further, the integrated input referred noise is 4.72 μV in a bandwidth of 1 MHz. From simulation, the upper cutoff poles of the two stages are located at 14 kHz and 43 kHz respectively; while analytical values of the same are 12 kHz and 49 kHz respectively. The fabricated IC has this bandpass amplifier while the subsequent signal processing is done on the test PCB.

B. Detection of Random Bit

The amplified signal V_o from the on-chip bandpass amplifier is fully differential which is converted to a single-ended signal $V_{out,se}$ by an instrumentation amplifier (part INA333) on the PCB (Fig. 2). It can be performed on-chip in future versions for fully integrated solutions. This single ended output ($V_{out,se}$ in Fig. 4) is compared with a threshold V_{thr} that is set according to algorithm specified in the next section. For the generation of the random bit Q, the comparator output is latched on the falling edge of the clock which is used to modulate the FHC output V_{sense}. The limited bandwidth of the amplifier of the comparator delays its output, ensuring $V_{out,se}$ is stable for some time after the negative clock edge thus taking care of hold time violation. The sharp falling edge of the clock latches the comparator output created by the previous rising edge of V_{sense}. SPICE simulation results for the bit generation are shown in Fig. 5. In this example, the output bit $Q = 1$ since the output $V_{out,se} > V_{thr}$. It should be noted that the clock frequency directly dictates the bit rate of the system–hence, it is desirable to have higher clock frequencies. But increasing

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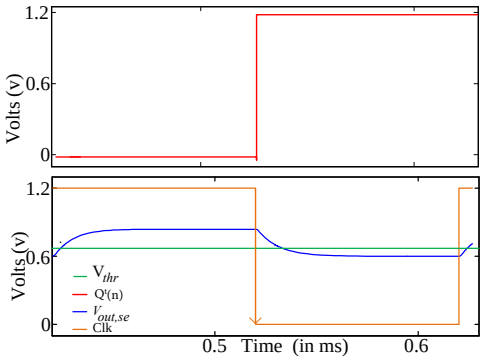

Fig. 5: Simulated waveform illustrating change of the random bit Q at falling edge of the clock. Since $V_{out,se} > V_{thr}$ till the clock edge, thus Q switches to 1 (from say initial 0) at the falling edge.

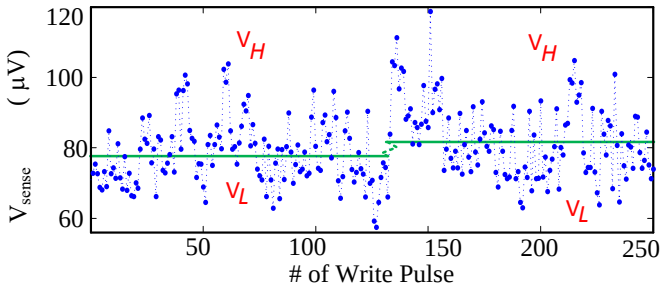

Fig. 6: Hall sensor outputs with application of write pulses. The green lines depict the time-average of the Hall sensor outputs during two successive time periods. By appropriately setting the threshold (V_{thr}), we can distinguish the logic levels corresponding to V_H and V_L. By converting V_H to high bit or '1' and V_L to low bit or '0' we can obtain a random bit stream.

the clock frequency has an adverse effect on system power and noise. Moreover, in arrays of such sensors where multiple amplifiers are placed next to each other in a constrained pitch, higher clock frequency will lead to more cross-talk. Keeping this in mind, we chose a clock frequency < 10 kHz in this work but point this out as a topic for future optimization.

C. Drift in Hall-voltage: Successive Approximation Algorithm to Set Threshold

The Hall-voltage V_{sense} fluctuates between voltages V_H and V_L randomly over successive write pulses. Setting an appropriate value of V_{thr}, these voltage levels can be distinguished as logical '1' or '0' after the comparator. While this works well over a short period of time, over a longer period of time (applying many more write pulses) there is unfortunately a drift in the values of V_H and V_L shifting their mean. Fig. 6 shows a sequence of Hall-voltages against application of write pulses illustrating the problem. To still generate an unbiased random number stream, the value of the threshold V_{thr} (shown in Fig. 2) should track the shift in V_H and V_L and ideally be set close to the mean of these signals (with a small difference equivalent to the offset of the comparator and readout). To overcome this issue, a successive approximation scheme to update V_{thr} is described next.

The intuition behind the algorithm stems from the fact that a random bit stream should have on average an equal number of '1's and '0's. Hence, the proposed algorithm tries to set V_{thr} such that it balances the number of '0's and '1's. If V_{thr} is much higher than the mean of V_H and V_L, then the number of low bits will be very high and vice versa if V_{thr} is too low. Therefore, to combat this skew in number of '1's , we need to increase V_{thr} if the number of '1's are more than 50% in an observation window of W bits. Alternately, V_{thr} is reduced if number of '0's are higher than 50% in the same window. This algorithm will eventually converge against the drift or change in V_H and V_L. Also note that the algorithm takes into account any offset voltage of the electronics and any associated drfit as well. The detailed flow chart of the algorithm is shown in Fig. 7 and the abbreviations used are provided below.

δ : Threshold of tolerable skew in number of '0's and '1's
t : Cycle index
n : Sample index within cycle
$Q^t(n)$: n-th output bit in t-th cycle
Q^t_{sum} : Sum of $Q^t(n)$ in cycle t
W : Length of cycle
V_{dd} : Power supply voltage
m^t : Dividing factor for t-th cycle

The algorithm is discussed in detail in the following.

- Step 0 is initialization of the first cycle with initial V_{thr} equal to half of power supply voltage.
- For every bit $Q^t(n)$ read in step 2, a variable Q^t_{sum} is updated to hold the running sum of the bits obtained so far where -1 is added for a '0' bit while 1 is added otherwise. This is indicative of moving average of the bits recorded so far in this cycle with an ideal value ≈ 0. δ is a parameter that indicates margin around 0 which is tolerable for the skew.
- In step 4, it is checked if $Q^t_{sum} > \delta$. If Yes, this indicates a relatively larger number of '1's and hence V_{thr} has to be reduced by the quantity $\Delta V_{thr} = \frac{V_{dd} - V^{t-1}_{thr}}{m^t}$ in step 12. The amount of reduction in V_{thr} (or step size in ΔV_{thr}) is controlled by m^t which depends on the outcome in the previous cycle–hence, in step 10 it is checked if $Q^{t-1}_{sum} < -\delta$. If yes, this indicates the current step size is too large and the value of V_{thr} is oscillating between too high and too low values. Hence, in that case m^t is updated to be twice the value in the previous cycle $t-1$ in step 11. If the check in step 10 is negative, then there is no update in the value of m^t. After updating the value of V_{thr} in step 12, the process is restarted from step 1.
- If the check in step 4 is negative, in step 5 it is next checked if $Q^t_{sum} < -\delta$. If Yes, this indicates a relatively larger number of '0's and hence V_{thr} has to be increased by the quantity $\Delta V_{thr} = -\frac{V^{t-1}_{thr}}{m^t}$ in step 9. Similar to the previous logic, we again have to check how to set m^t. Hence, in step 7 it is checked if $Q^{t-1}_{sum} > \delta$. If yes, then this indicates oscillation in increasing and decreasing V_{thr} and hence step size is reduced by increasing m^t by a factor of 2 in step 8. If the check in step 7 yielded a negative result, m^t is unchanged. The process is again started from step 1 after this.
- Lastly, if the check in step 5 was negative, this indicates

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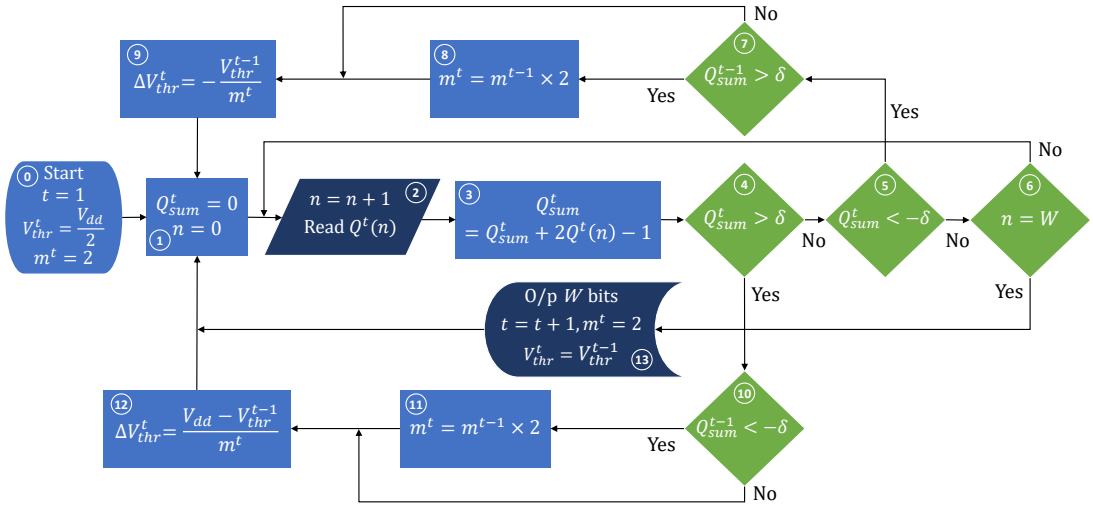

Fig. 7: Flowchart describing algorithm employed to update the threshold of comparator, V_{thr}, to account of for change in V_H and V_L. Each step number of the algorithm is written at the corner of corresponding box in the flow chart. The main concept is to maintain a running sum, Q_{sum}^t (step 3) indicative of the moving average value of the generated bits $Q^t(n)$, monitor Q_{sum}^t continuously for skew in number of 1's and 0's. If absolute value of Q_{sum}^t crosses the margin δ (steps $4, 5$), the number of '1's or '0's are considered skewed and V_{thr} is tuned (steps $9, 12$) to reduce skew as shown above. On the other hand, if the margin is not crossed, this set of W bits are output as valid (step 13).

the value of Q_{sum}^t is acceptably close to 0. Hence, on reading W bits in this loop, we can go to step 13 and output these bits. Then, the process is restarted from step 1 keeping the value of V_{thr} unchanged.

The selection of parameters δ and counter window W involve several trade-offs. If $\frac{\delta}{W}$ is too low, it may lead to difficulty in convergence due to very strict criteria. On the other hand, if W is too small, it may not give a suitable estimation of the mean. The values used in our experiments are described in the next section.

IV. Results

A. Characterization of Fabricated IC

The readout circuit shown in Fig. 4(a) has been fabricated in 65nm CMOS process. The threshold V_{thr} is set externally for the measurements. First, the fabricated bandpass amplifier is characterized separately with results plotted in Fig. 8. Fig. 8(a) depicts transfer function of the two-stage amplifier for different settings of the bias voltage V_{b2}. The bias currents are set similar to the simulation setup described earlier in Section III. The mid-band gain A_0 is indeed close to 80 dB as expected based on simulation. The higher cut-off frequency $f_h \approx 8$ kHz while the lower cut-off f_l is varied by changing V_{b2}. High values of V_{b2} result in higher values of pseudoresistor R_f which in turn leads to lower values of f_l. For these experiments, V_{b1} is kept at a high value of 530 mV, while varying V_{b2} from 325–530 mV changed f_l from $\approx$ 1000–10 Hz as shown in Fig. 8(b). Finally, measured input referred noise spectrum for the readout amplifier is shown in Fig. 8(c). The integrated input referred noise is about 1.5 μV which is lower than the simulated value, possibly due to mismatch in noise model between simulation and reality. Table II summarizes properties of the fabricated amplifier. The power dissipation of the circuit could not be measured separately due to the shared power supply with other circuits on the chip. Instead, we report the maximum power dissipated by the two stages of the bandpass amplifier for the highest bias current setting in simulations. In addition, the bias circuit on the chip dissipates a further $\approx$ 8 μW of power.

TABLE II: Parameters of the fabricated bandpass amplifier

Parameter	Simulated Value	Measured Value
Midband gain	79.1 dB	83 dB
Bandwidth	15 Hz–13.6 KHz	9 Hz–8 KHz
Input referred noise	4.72 μV	1.5 μV
Power consumption	28 μW	–

For electrical characterization of the entire TRNG system, we emulated the Hall-sensor with a balanced arbitrary input. A recurrent pattern of 101010.. was used to excite the readout circuit and convergence of V_{thr} from different conditions were tested. In this case, an external microcontroller (Arduino 101 [19]) was used to run the algorithm described in Fig. 7 and an on-board digital-analog converter (MCP4725 with 12-bit resolution from 5-V power supply) was used to create the V_{thr} voltage as input to the comparators. Hence, the input referred resolution for setting the threshold voltage is ≈ 0.12 μV when divided by the $\approx$ 80 dB gain of the frontend. The detector circuit helped the V_{thr} converge until the saturation of amplifier output at 440 μV of input voltage swing. The lower range of convergence is dictated by the resolution of Hall-voltage of the system. Fig. 9 shows the convergence of V_{thr} according to the implemented algorithm. The detected bits $Q^t(n)$ are plotted in terms of their voltages ranging from 0–3.3 V instead of logical values. In this case, a change in the values of V_H and V_L were programmed at a time of 0.27 s to

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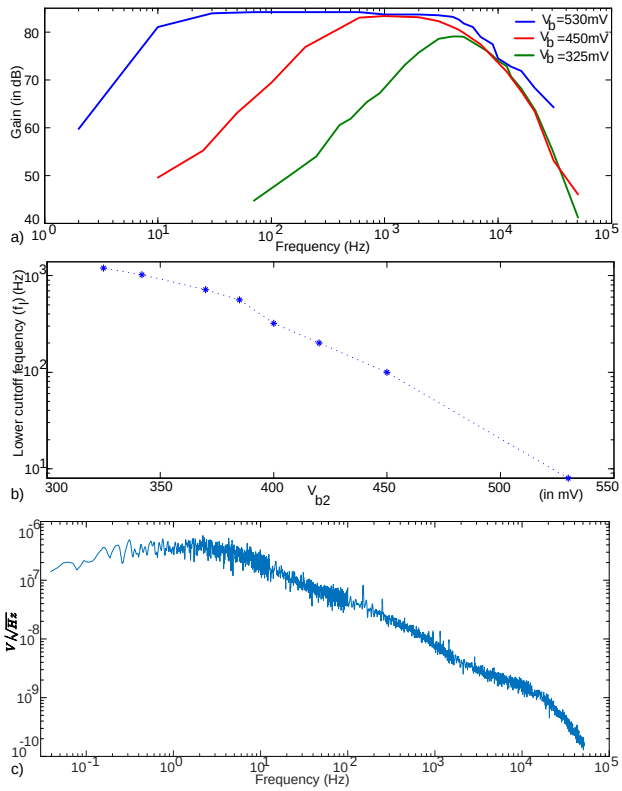

Fig. 8: Measured characteristics of the fabricated chip. a) The lower cut-off frequency f_l of the readout amplifier can be adjusted by tuning (V_{b2}). By decreasing V_{b2}, f_l increases. b) Plot of variation in f_l with decreasing V_{b2} of the second stage amplifier. Here, V_{b1} is kept at a much higher value of 530 mV. (c) Measured input referred noise spectral density of the readout circuit.

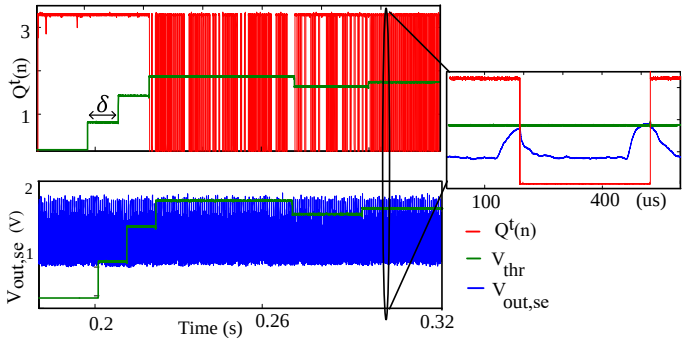

Fig. 9: Convergence of V_{thr} according to the algorithm in Fig. 7. The detected bits $Q^t(n)$ are plotted in terms of their voltages ranging from $0 - 3.3$ V instead of logical values. $f_0 = 3$ kHz is used in this case and a step change in the values of V_H and V_L are applied at time 0.27 sec. It is visible that V_{thr} reaches close to mean of V_H and V_L within 60 cycles (20 ms) of the change. The figure in the right is horizontally zoomed to highlight steady state V_{thr}.

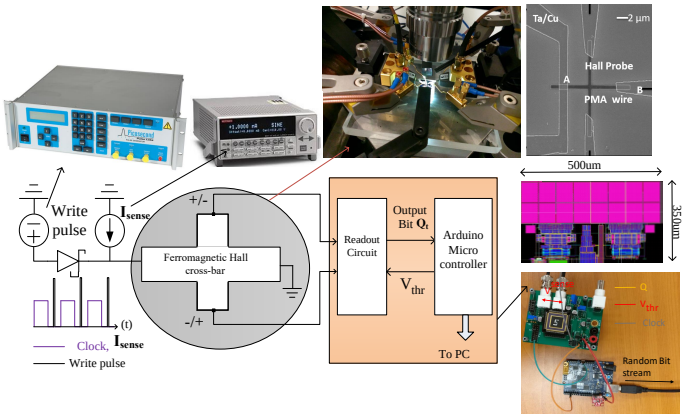

Fig. 10: Block diagram of the experimental setup. Successive application of write pulse and read current I_{sense} produces the random bit stream. The Arduino 101 takes this array of output bits $Q^t(n)$ as input and sets the V_{thr} according to algorithm shown in Fig. 7.

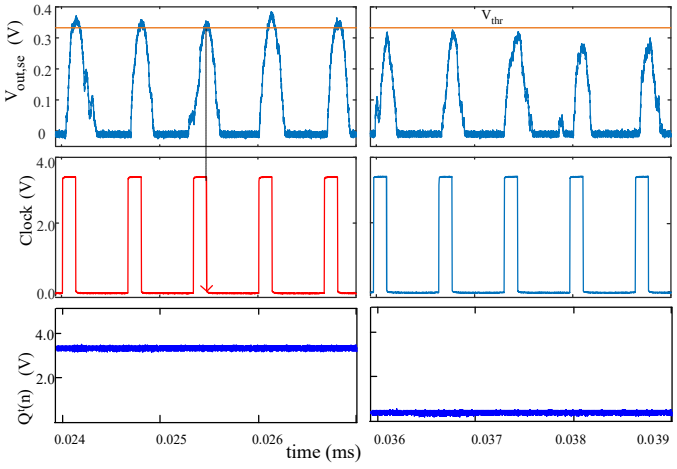

Fig. 11: Detection of bit. The figure shows the distinction made by the circuit after settling to a threshold $V_{thr} = 340$ mV. Two distinct Hall-voltages generated before and after application of write pulse produce the amplifier outputs shown. When the amplifier output $V_{out,se} > V_{thr}$, the comparator produces a high bit on the falling edge of clock and a '1' is latched (left). In the other case, a '0' is latched (right).

check on the convergence of the algorithm under perturbation. It can be seen that V_{thr} converges approximately to desired value within detection of 60 bits that is equivalent to 20 ms for $f_0 = 3$ kHz. The value of δ used here is 15 and V_{thr} was initialized to 0 V. In the initial transient period when V_{thr} is very low, it can be seen that step 4 in the flowchart (Fig. 7) is being checked when $Q^t(n) = 1$ for consecutive δ cycles. Reducing δ helps in converging faster for initial transients but this will lead to disruption of V_{thr} from mean of V_H and V_L with longer stream of 1's or 0's. Moreover, a higher value of δ will help in robustness against noise induced random bits where difference between V_H and V_L are low. Window length (W) prescribes the duration for which skewness of bits should be validated, value of which has been fixed to 100 here. Though it is desirable to increase W for conventional random bit streams, sudden drift in Hall-voltage will prompt us to discard entire array of bits under consideration. This will severely hurt the real throughput. Further, longer validation windows will have to accommodate larger margin parameter δ, leading to slower convergence after transient changes.

B. Experiment with Cross-bar Hall Sensor

The Hall sensor is fabricated and the random Hall-voltages are measured using a probe station (example in Fig. 6). Hall output terminals are connected to the readout circuitry as

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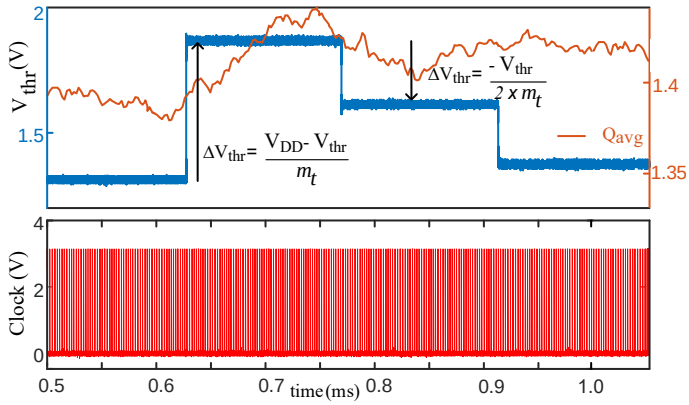

Fig. 12: Convergence of V_{thr} set according to the algorithm in Fig. 7 on testing the random V_{sense} generated from cross-bar Hall sensor. Q_{avg} is the moving average of amplitudes of $V_{out,se}$ after successive write cycles–it is shown to give an estimation of the drift.

shown in Fig. 2. The bandpass amplifier IC described earlier is soldered to the PCB and the output of the amplifier is followed by a commercial instrumentation amplifier with a gain ≈ 1 to convert the differential output of the IC to a single ended signal $V_{out,se}$. The single-ended output is compared to threshold V_{thr}. The comparator has an internal hysteresis of 4 mV for immunity to noise induced switching. The comparator output is sampled at the falling edge of the clock using an on-board flip-flop. The outputs of the flop are read by an Arduino Board using an interrupt mechanism and the threshold V_{thr} is generated according to the algorithm mentioned in the earlier section. A photograph of the experimental setup is given in Fig. 10. Picosecond Pulse Labs 10300B and Keithley 2400 have been utilized for writing and reading respectively.

Fig. 11 illustrates the obtained output from the full system. In this case, the value of V_{thr} is explicitly fixed to a desired value. It can be seen that when $V_{out,se} > V_{thr}$, the detected bit $Q^t(n)$ is always latched as '1' while it is always latched at '0' in the other case. Finally, the results of automatically setting V_{thr} via the algorithm described in Fig. 7 is depicted in Fig. 12. Average value of V_H and V_L is also plotted in the figure (denoted by Q_{avg}) to help indicate the nature of drift in the signal. It can be seen that indeed there is an increase in V_{thr} for increase in Q_{avg} and vice versa demonstrating successful operation of the whole system. Also, the reduction in step size by increasing m^t due to oscillation in setting V_{thr} (successive increase and decrease) can be seen in this case.

Table III compares the performance of our system with other reported circuits. Though there are no prior implementation of integrated Hall-sensor readout circuitry, there are Hall sensors which measure external magnetic field. The power consumption of individual blocks of our system could not be measured as the V_{dd} supply was shared in our test PCB.

Ajbl et. al [20] had presented an integrated Hall-sensor micro-system for readout of magnetic fields. The system is capable of resolving Hall-sensor voltages upto 400 nV. However, the system is very slow in demodulating the chopped signals with a throughput less than 1 Hz. This Hall sensor detection system is not scalable for fast readout of random numbers from cross-bar Hall-structures. Moreover, this method requires external biasing of preamplifier. Similarly, Frounch et. al. [21] developed an integrated micro Hall-sensor system. The major issues with it are an high offset voltage of 28 μV and complex demodulation circuit. Also, both the switched capacitor systems face interference from internal clock frequency of modulation. The output low pass filter cutoff frequency should be contained well within the internal clock frequency. Though there exist very low-power high sensitive current mode Hall-sensor detection [22], [23], our comparison is limited to Hall-voltage sensing circuits since the current sensing method is applicable to sense external magnetic field while in our case, the device has in-built magnetization which we sense through the anomalous Hall voltage. The measured noise (≈ 15 μV) when the front-end IC is connected to the FHC was higher due to noise pickup by the interconnecting cables–this can potentially be eliminated in future by putting the FHC on-chip. Further, since the step size of setting V_{thr} is much less than the measurement precision, it sets the limit for offset correction as well.

TABLE III: Comparison of existing integrated Hall-sensor systems.

Parameter	NEWCAS 2011 [20]	ISSCC 2001 [21]	FTFC 2014 [24]	JSSC 2014 [23]	**This Work**
Resolution (μV)	0.4	2	1000	4.45	1.5 (15)*
Area (mm^2)	2.25	–	0.002	–	0.175
Process	0.35 μm	0.8 μm	0.18 μm	0.18 μm	65 nm
Power (μW)	1200	5000	33	–	126#
Offset (μV)	–	28	–	1.25	<1.5 (15)*
Mid-Band Gain (in dB)	84	54	30	58	83
Drift Compensation	–	NA	–	–	Yes

* 15 μV is the minimum detectable signal when connected to Hall sensor which is larger than circuit noise floor due to additional external noise coupling.

\# Power consumption of associated Arduino is not considered here. The instrumentation amplifier on PCB consumes 90 μW of power.

V. Conclusion

In this paper, we presented a novel magnetic TRNG based on Hall-voltage generated by the magnetization dynamics of a PMA structure as an entropy source. On application of a sense current, the stochastic nucleation of domains can be read as an anomalous Hall-voltage. To sense these low voltages, a readout band-pass, low-noise amplifier is designed in 65nm CMOS technology. Application of current pulses at a frequency $f_0 \approx 3$ kHz naturally modulates the input voltage to the amplifier to a high enough frequency to avoid effects of flicker noise. Thermal noise is reduced by a two stage amplifier structure with low-noise in first stage and low bandwidth in second stage. The resulting circuit is shown to exhibit 80 dB of gain, about 1.5 μV input referred noise, $f_h \approx 8$ kHz with a power dissipation of ≈ 126 μW. Further, to counter the drift in high and low levels of Hall-voltage, a successive approximation algorithm to set the threshold voltage of the comparator generating the bits is described. Full

system measurements of the readout electronics with a Hall cross sensor are also shown.

Future work include long term characterization of the random numbers to test the quality of randomness and integrating parallel readout circuits on the same chip for higher throughput random number generation. A possible direction of future research can also be an extension of the presented concept using techniques reported in [25] and [23] where the former presented a silicon Hall circuit for compass applications with low offset but having low bandwidth, and the later showing how to increase the bandwidth without increasing offset via ripple reduction technique.

REFERENCES

[1] G. E. Suh and S. Devadas, "Physical Unclonable Functions for Device Authentication and secret key generation," in *Design Automation Conference, 2007. DAC'07. 44th ACM/IEEE*. IEEE, 2007, pp. 9–14.

[2] S. Katzenbeisser, Ü. Kocabaş, V. Rožić, A.-R. Sadeghi, I. Verbauwhede, and C. Wachsmann, "PUFs: Myth, Fact or Busted? A Security Evaluation of Physically Unclonable Functions (PUFs) Cast In Silicon," in *International Workshop on Cryptographic Hardware and Embedded Systems*. Springer, 2012, pp. 283–301.

[3] S. K. Mathew, S. Srinivasan, M. A. Anders, H. Kaul, S. K. Hsu, F. Sheikh, A. Agarwal, S. Satpathy, and R. K. Krishnamurthy, "2.4 Gbps, 7 mW All-digital PVT-variation Tolerant True Random Number Generator for 45 nm CMOS high-Performance Microprocessors," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 11, pp. 2807–2821, 2012.

[4] C. Tokunaga, D. Blaauw, and T. Mudge, "True Random Number Generator With a Metastability-based Quality Control," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 1, pp. 78–85, 2008.

[5] W. H. Choi, Y. Lv, J. Kim, A. Deshpande, G. Kang, J.-P. Wang, and C. H. Kim, "A Magnetic Tunnel Junction Based True Random Number Generator with Conditional Perturb and Real-time Output Probability Tracking," in *Electron Devices Meeting (IEDM), 2014 IEEE International*. IEEE, 2014, pp. 12–5.

[6] T. Tanamoto, N. Shimomura, S. Ikegawa, M. Matsumoto, S. Fujita, and H. Yoda, "High-speed Magnetoresistive Random-Access Memory Random Number Generator Using Error-Correcting Code," *Japanese Journal of Applied Physics*, vol. 50, no. 4S, p. 04DM01, 2011.

[7] P. Sethi, C. Murapaka, G. Lim, and W. Lew, "In-plane Current Induced Domain Wall Nucleation and Its Stochasticity in Perpendicular Magnetic Anisotropy Hall Cross Structures," *Applied Physics Letters*, vol. 107, no. 19, p. 192401, 2015.

[8] P. Sethi, "Magnetization dynamics of domain wall based devices for logic and memory applications," Ph.D. dissertation, Nanyang Technological University, Singapore, 2017. [Online]. Available: https://dr.ntu.edu.sg/handle/10356/72731

[9] R. R. Harrison and C. Charles, "A Low-power Low-noise CMOS Amplifier for Neural recording Applications," *IEEE Journal of solid-state circuits*, vol. 38, no. 6, pp. 958–965, 2003.

[10] Y. Chen, A. Basu, L. Liu, X. Zou, R. Rajkumar, G. S. Dawe, and M. Je, "A Digitally Assisted, Signal Folding Neural recording Amplifier," *IEEE transactions on biomedical circuits and systems*, vol. 8, no. 4, pp. 528–542, 2014.

[11] M. D. Stiles and A. Zangwill, "Anatomy of Spin-Transfer Torque," *Physical Review B*, vol. 66, no. 1, p. 014407, 2002.

[12] I. M. Miron, G. Gaudin, S. Auffret, B. Rodmacq, A. Schuhl, S. Pizzini, J. Vogel, and P. Gambardella, "Current-driven Spin Torque Induced by the Rashba Effect in a Ferromagnetic Metal Layer," *Nature materials*, vol. 9, no. 3, p. 230, 2010.

[13] M. Tavakoli, L. Turicchia, and R. Sarpeshkar, "An Ultra-Low-Power Pulse Oximeter Implemented With an Energy-efficient Transimpedance Amplifier," *IEEE transactions on biomedical circuits and systems*, vol. 4, no. 1, pp. 27–38, 2010.

[14] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: Autozeroing, correlated double sampling, and chopper stabilization," *Proceedings of the IEEE*, vol. 84, no. 11, pp. 1584–1614, 1996.

[15] Y. Li, M. Motz, and L. Raghavan, "A Fast T&H Overcurrent Detector for a Spinning Hall Current Sensor With Ping-Pong and Chopping Techniques," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 7, pp. 1852–1861, 2019.

[16] J. Jiang and K. A. A. Makinwa, "Multipath Wide-Bandwidth CMOS Magnetic Sensors," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 1, pp. 198–209, 2017.

[17] W. Wattanapanitch, M. Fee, and R. Sarpeshkar, "An Energy-efficient Micropower Neural Recording Amplifier," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 1, no. 2, pp. 136–147, 2007.

[18] B. Razavi, *Design of Analog CMOS Integrated Circuits*. McGraw Hill Education, 2005.

[19] Arduino. Getting Started with the Arduino/Genuino 101. [Online]. Available: https://www.arduino.cc/en/guide/arduino101

[20] A. Ajbl, M. Pastre, and M. Kayal, "A Current-Mode Back-end for a Sensor Microsystem," in *New Circuits and Systems Conference (NEWCAS), 2011 IEEE 9th International*. IEEE, 2011, pp. 466–469.

[21] J. Frounchi, M. Demierre, Z. Randjelovic, and R. S. Popovic, "Integrated Hall Sensor Array Microsystem," in *Solid-State Circuits Conference, 2001. Digest of Technical Papers. ISSCC. 2001 IEEE International*. IEEE, 2001, pp. 248–249.

[22] H. Heidari, E. Bonizzoni, U. Gatti, and F. Maloberti, "A CMOS Current-mode Magnetic Hall Sensor with Integrated Front-end," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 5, pp. 1270–1278, 2015.

[23] J. Jiang, W. J. Kindt, and K. A. A. Makinwa, "A Continuous-Time Ripple Reduction Technique for Spinning-current Hall Sensors," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 7, pp. 1525–1534, 2014.

[24] A. Mordakhay and A. Fish, "Analog Readout Circuit for Zero Leakage Planar-Hall-Effect-Magnetic-Random-Access-Memory," in *Faible Tension Faible Consommation (FTFC), 2014 IEEE*. IEEE, 2014, pp. 1–4.

[25] J. C. van der Meer, F. R. Riedijk, E. van Kampen, K. A. A. Makinwa, and J. H. Huijsing, "A Fully Integrated CMOS Hall Sensor with a 3.65 μT 3σ Offset for Compass Applications," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*. IEEE, 2005, pp. 246–247.