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Wire-bonding process development for low-*k* materials

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Abstract

A 60-μm bond-pad-pitch wire-bonding process was developed using test dies with a SiO_2 dielectric layer under aluminium pads, and was then fine-tuned for a low-*k* device using three types of gold wires with different mechanical properties. Bulk material hardness of the wires were characterised using a wire-bonding machine, the force applied and diameters of squashed free-air balls. It was found that stiffer wires needed higher ultrasonic-generator (USG) power than a softer wire to deform the ball after impact and achieve equivalent ball size and ball shear responses. Longer bond time was also needed for the low-*k* material than the SiO_2 material, to overcome the energy loss due to the compliance of the low-*k* material. Pad damage on the low-*k* device was proportional to bulk material hardness. The soft 4N (99.99% purity) wire required lower USG power to achieve the bonding specification, and was the most suitable wire to be used in wire bonding of the low-*k* device.

Keywords: Wire bond; Low-*k* material; Aluminium pad; Gold wire; Hardness; Pad damage

1. Introduction

The increasing demands for high electrical performance and pin count have led to significant advances in IC (integrated circuit) fabrication and microelectronics packaging [1–6]. Processing of silicon wafers also plays an enhanced role in microelectronics and micro-electro-mechanical systems [7].

Wire bonding is the most widely used technology in the microelectronics industry [8]. For peripheral array chips, wire bonding is cheaper than flip chip [9,10] if the chip size and the pad pitch are very large [11]. Today's demands for speed, accuracy and reliability are fulfilled with modern cameras and intelligent algorithms [12].

Microelectronics packaging has sparked intensive interest in ultra-thin packages [13]. The bond

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loop height is one of the dominating parameters in reducing the thickness of ultra-thin packages [14]. Besides the most commonly used gold wires, Al–Si wires are also used for microelectronics packaging [15]. To improve the performance of advanced ICs, a transition from Al to Cu metallisation is in progress [16].

High quality of bonds is vital to the performance of an IC chip. Therefore, a proper bonding quality control system is desirable [17]. Parameter settings for successful wire bonding depend on many factors, requiring expert knowledge to optimise critical process characteristics [18]. The principal parameters such as bonding time, normal force, ultrasonic power, etc., can affect wire-bonding quality [19].

Ultrasonic technology can be used for many applications [20,21]. In ultrasonic metal welding, the use of ultrasounds allows metals to be cold-welded [22]. A decisive factor affecting electrical and mechanical proprieties of the bond is the vibrational behaviour of the capillary [23]. Ultra-fine-pitch wire bonding [24] requires higher stability and robustness of ultrasonic vibrations [25].

The evolution of IC devices is governed by Moore's law, achieved largely through die shrinks. This has improved unit die cost and reduction in gate delay. As the semiconductor node moves from 0.25 μm to lower values, a critical point is reached where reduction in signal propagation delay due to a shorter path is offset by a higher resistance of metal trace and an increased effect of inter- and intra- layers of insulating dielectrics [26]. The conventional dielectric SiO_2 is not able to meet the requirement. However, the increase in resistance of metal trace and inter-, intra- insulating layers can be minimised by using copper interconnects (lower resistance) and lower dielectric constant material (lower signal propagation delay).

A dielectric constant <3 is a challenging demand for dielectrics in conventional multilevel metallisation schemes of modern IC technology [27]. Novel IC devices based on the structure of low-dielectric-constant material/Cu have been proposed recently [28]. The requirements for future high-end CMOS (complimentary metal–oxide–semiconductor) logic technologies can only be achieved by using ultra low-k materials ($k \sim 2.3$ or lower) [29].

Low-k dielectric materials are categorised into two major wafer fabrication process categories, namely spin-on dielectric and chemical vapour deposited dielectric materials. Table 1 shows main low-k dielectric materials, dielectric constant values and some mechanical properties [26,30,31].

Bonding on such low modulus materials has resulted in bond pad 'cupping' and delamination of the polymer, lowering bond yield and reducing device reliability [26]. Such polymers tend to absorb ultrasonic energy when they are softened by heat applied during bonding, which further lowers the yield during production. 'Rigidising' the pad with a hard metal (Ni, Ti, Cr, etc.) is a common solution for multi-chip modules, but may not be possible for fine-pitch semiconductor pads [32].

Another polymer-induced bonding problem occurs in fine pitch bonding when the bond pad size is small, comparable to the deformed bond dimensions. This is because if the polymer is soft (its modulus is less than 3 GPa) or it is heated above its T_g (during thermosonic bonding), the rigid but small bond pad can partially sink into the polymer during application of bonding force. This lowers effective impact and bond force after the capillary contacts pads, and thus higher ultrasonic

Table 1
Low-k materials for microelectronics interconnects [26,30,31]

Dielectrics	Dielectric constant (k)	Modulus (GPa)	Hardness (GPa)	Stress (MPa)	Fracture–tough (MPa $m^{1/2}$)
FSG	3.4–4.1	72	7.5	100	0.75
Black Diamond	2.7	7.76	0.13–3.6	–	0.2–0.3
SiLK	2.6	2.5–4.2	0.2–0.28	90	0.62
TEOS (SiO_2)	3.2–4.1	72–100	9.5	–	0.46
Porous SiLK	2.0	1.5–3.0	0.16–0.19	54	0.62
SiO_2	4.1	72	7.5	100	0.75

energy is required to form reliable bonds. 'Cupping' or sinking of bond pads damages low-k diffusion barriers and leads to failure. Therefore, some form of underpad support structures compatible with IC fabrication is required [32]. Advanced automatic wire bonders are now able to overcome this problem using force-controlled bonding modes.

A major task for today's microelectronics industry is to process low-k materials and assemble packages in the same manner for SiO_2 based ICs. Although porous low-k materials are largely used in advanced interconnection technologies such as flip chip, the mainstream assembly method, wire bonding, is still widely used in microelectronics packaging. Much work has been done in identifying and optimising wafer fabrication processes and optimising the wire-bonding process. However, little work has been done on characterising gold wire properties.

This study aims to understand how properties of gold wires interact and influence the bonding process. Three types of wires were chosen for the study: a 2N gold wire (type 1) with 99% purity, a relatively soft gold wire (type 2) with 99.99% (4N) purity, and a stiff gold wire (type 3) with 99.99% (4N) purity. A 60-μm bond-pad-pitch (BPP) wire-bonding process was developed using test dies with a SiO_2 dielectric layer under the aluminium pads, and was then fine-tuned using each of the three wires for a low-k device.

2. Experiments

Free air balls (FABs) were formed using a special process, which allows FABs to be 'flipped' over after they were formed at the electronic-flame-off (EFO) cycle and bonded on the pads of leadframes without deforming FABs. The bonding was also known as cherry pit bonding, shown in Fig. 1. The standing FABs formed without any wire interfering with the circumference allowed the magnified image to be measured using an optical microscope equipped with customised vision software. The objective of the experiment was to confirm that FABs produced using different wire types were identical before actual process optimisation took place.

The next experiment involved the 60-μm-BPP process optimisation using test dies with SiO_2. A stiff wire (4N, type 3) was selected for the baseline experiment, as it was the wire used in most fine-pitch applications. The objective of the experiment was to identify a set of baseline parameters that could be used for bonding the low-k device. An experimental matrix was generated for four variables selected. The experiment was designed and optimised using a response surface with a quadratic function [33].

Finally, the low-k device was bonded on 35×35-mm 450-I/O (input/output) PBGA (plastic ball grid array) substrates. The low-k material with $k = 2.7$ is a thin layer deposited by a chemical

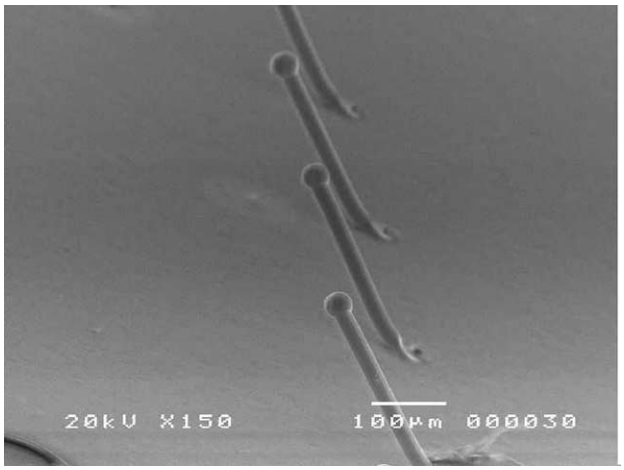

Fig. 1. SEM picture of cherry pit bonding.

vapour deposition process under the aluminium pad. The experiment started with type-3 wire (stiff, 4N), followed by types 1 (2N) and 2 (4N). The bonding parameters established using type-3 wire were used as a starting point. The main objective was first to achieve the ball size and ball shear readings within the specified ranges. If the results were not attained, the parameters would be adjusted accordingly. Inter-layer damage would be checked when the above criteria were met. The response of inter-layer damage would be studied for the three types of wire.

FABs were squashed onto bond pads with a capillary to characterise the hardness property of wires. Fig. 2 illustrates a side view of such a squashed FAB. To eliminate effects of ultrasonic-generator (USG) power and sticking of smashed balls onto pads, USG parameters and bond force were set to zero and the bonding temperature was set at 100 °C. A force of 11.6 g was used to squash FABs, which was the same as the impact force used in bonding of the devices. To further emulate the 'hardness test' of single impact, the feature ''Bump Bond Loop'' was used. This would prevent the machine from squashing the balls a second time at the second bond location. This is because bump bonds are essentially a single bond process. Smashed ball diameters were then measured, and equivalent bulk hardness H_v was calculated using Eqs. (1) and (2) adopted from Vickers hardness test [34].

$$H_v = \frac{F}{A}, \tag{1}$$

$$A = \pi \frac{d^2}{4}, \tag{2}$$

where d is the squashed diameter, and F is the squashing force.

3. Results and discussion

According to a previous study [35], a heat-affected zone (HAZ) is a product of the plasma heat input during the EFO firing. There is a one-to-one monotonic functional relationship between the heat input and the EFO current. When the wire is heated by the plasma from the EFO discharge, the free air ball will re-crystallise. The hardness of the wire is thus proportional to the inverse of the square root of the grain size [35]. The HAZ length is proportional to the temperature during heating, which is related to the EFO current. EFO current was kept constant at 30 mA in this experiment.

Results of the FAB measurements are shown in Table 2. The results indicated that the same parameters could not be used for the 2N wire. This is because while the 4N wires (types 2 and 3) produced compatible FAB sizes, a larger FAB was formed for the 2N wire. This was attributed to its alloy constituents, which lowered the melting

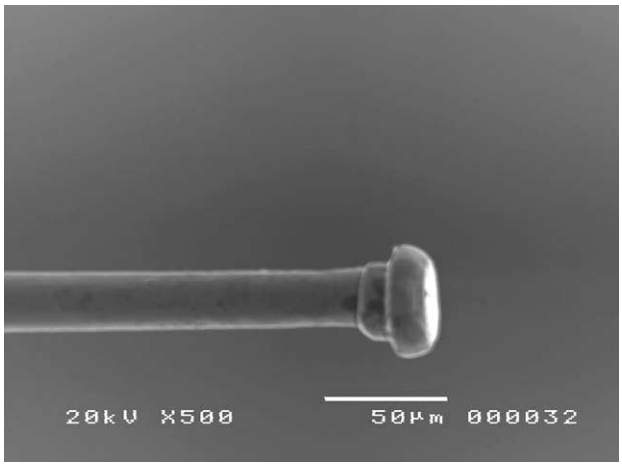

Fig. 2. SEM picture of a squashed FAB.

temperature that caused more volume of the wire to be melted during the EFO discharge, forming a larger FAB. A lower setting value of 'FAB size' was used to achieve comparable FAB sizes. This variable controls the EFO firing time during the FAB formation of the wire bond cycle. In Table 2, run No. 4 for type-1 wire is the result achieved by using a smaller 'FAB size' setting.

This phenomenon is not typical for all 2N alloys but only for the alloy used in this experiment. The alloy compositions of 2N wires strongly influence thermal and mechanical properties of the resultant wires.

Using DOE (design of experiments) with ECHIP® software, the significant variables to the responses were identified. Bond force, USG power and bond time were found to be significant in the experiment. A set of optimised parameters that best meet the requirements was also found. Zero pad-inter-layer damage/peeling had been achieved by the 60-μm-BPP wire-bonding process for the device with SiO_2.

Squashed ball diameters of gold wires were measured as described in the previous section. Equivalent bulk wire hardness was then calculated using Eq. (1) and is summarised in Table 3. Type-3 wire has the highest bulk material hardness while type-2 wire has the lowest among the three wire types.

Table 4 summarises the parameter settings used in the DOE tests for devices with the low-k material or SiO_2. Results of the bonding responses are illustrated in Table 5. The bonding results of the low-k device showed that longer bond time was required for all three types of wires than the SiO_2 base-lined device. This was due to the low-k material being relatively more compliant than SiO_2. Hence, longer bond time was needed to overcome the loss of energy in order to achieve the same bonding quality for the SiO_2 material. In addition, type-1 and type-3 wires also required higher USG power to achieve equivalent response to the SiO_2 based device. They had higher bulk material hardness than type-2 wire. With higher bulk material hardness, higher USG energy was needed.

Next, to assess the pad structure, a cratering inspection test [36] was performed. The bonded devices were etched with KOH solution for 20 min. The solution dissolved aluminium pads allowing bonded balls to be removed without disturbing the dielectric layers. Four hundred and fifty bonded pads were checked for any damage using an optical microscope. The results are shown in the last column of Table 3. A graph was also plotted to relate bulk wire hardness to inter-layer damage, as shown in Fig. 3. The results revealed that type-2 wire caused negligible damage to the layer under the aluminium pad.

Fig. 4 illustrates an etched device bonded with type-2 wire. There were only light imprints on the etched surfaces, which indicated that the pads

Table 2
Results of FAB measurements

Run No.	1	2	3	4
Wire type	3	2	1	1
'FAB size' setting (μm)	41.9	41.9	41.9	34.3
Minimum (μm)	33.4	32.5	37.2	34.2
Maximum (μm)	35.5	34.9	39.3	35.7
Average (μm)	34.8	34.0	38.1	35.0
Standard deviation (μm)	0.5	0.6	0.4	0.4

Table 3
Bulk wire hardness and pad damage

Wire type	Smashed ball diameter (μm)	Hardness (MPa)	Relative hardness	Pad damage
1	39.3	97.902	88%	4.4%
2	40.5	88.298	79%	0.5%
3	36.0	111.821	Baseline	14.6%

Table 4
Summary of parameter settings used

Wire type/device type	Impact force (g)	USG setting (mA)	Bond time (ms)	Bond force (g)
Type 3/SiO_2	11.6	70	10	13
Types 1 and 3/low k	11.6	75	15	13
Type 2/low k	11.6	70	15	13

Table 5
Bonding responses

Wire type	Ball size (μm)	Ball height (μm)	Shear (g)	Shear/area (MPa)
1	41.0	10.0	12.77	94.89
3	44.2	10.0	14.10	90.15
2	41.5	10.0	12.62	91.53

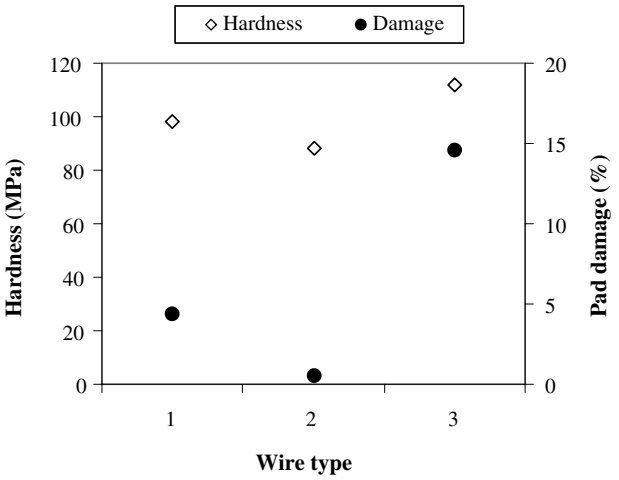

Fig. 3. Bulk hardness and pad damage in percentage.

had been bonded. No cracks or delamination of inter-layers were observed on the pads. Fig. 5 shows that there was peeling of inter-layers under the aluminium pad for samples bonded with type-1 wire. It was also noted that two layers of the material peeled off after KOH etching. Fig. 6 illustrates damage of inter-layers for a sample bonded with type-3 wire. Its failure mode was different from that observed in Fig. 5. Cracks were observed beneath the peeled material.

From these findings, pad damage on the low-*k* device was proportional to bulk material hardness of the wire used. According to a finite element analysis [36], stress concentration was found near the perimeters of bonded balls.

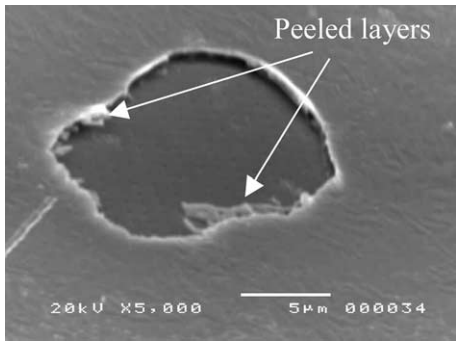

Fig. 5. Etched bond pads on the low-*k* device bonded with type-1 wire.

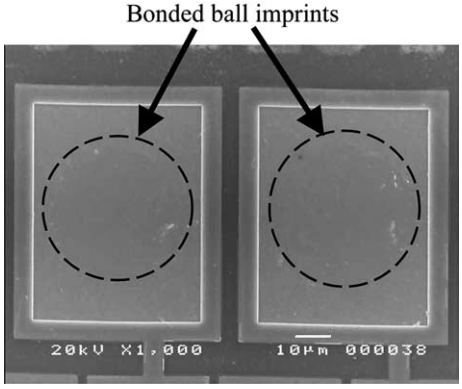

Fig. 4. Etched bond pads on the low-*k* device bonded with type-2 wire.

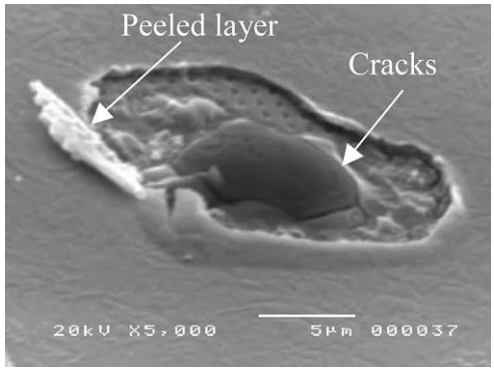

Fig. 6. Etched bond pads on the low-*k* device bonded with type-3 wire.

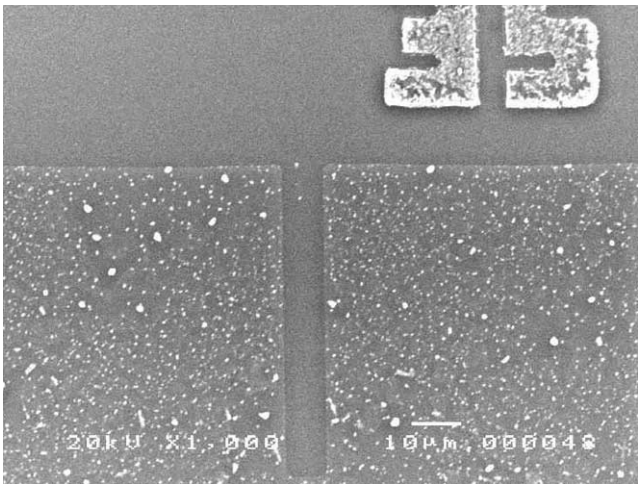

Fig. 7. Etched bond pads on the base-lined SiO_2 device bonded with type-3 wire.

Hence, the material failed at the area with the highest stress concentration.

A reference is shown in Fig. 7 with KOH solution etching of the base-lined SiO_2 device bonded with type-3 wire. It was observed that compared to the low-*k* device, the USG energy needed to achieve the required responses for the baseline SiO_2 material was also lower.

From the bonding results, it was found that the stiffer wires (types 1 and 3) needed higher USG power than type-2 wire to achieve equivalent responses. The higher energy needed was due to the higher bulk material hardness of the wires. Longer bond time was needed for the low-*k* material compared to the SiO_2 material. An increase in bond time was required to overcome the energy loss due to the compliance of the low-*k* material. Type-3 wire was the hardest among the three types of wires investigated, about 21% harder than type-2 wire, based on the equivalent bulk wire hardness calculation. Pad damage on the low-*k* device was proportional to bulk material hardness.

4. Conclusions

Bulk material hardness of the wires were characterised using an original set-up of a wire-bonding machine, the force applied and the diameters of squashed FABs. The challenge of measuring the FABs without measurement error was overcome by using cherry pit bonds. Bonding on low-*k* devices had been investigated with three types of gold wires with different mechanical properties. Type-3 wire was the hardest among the three types of wires, about 21% harder than type-2 wire based on the bulk wire hardness calculation.

It was found that the setting of the variable 'FAB size' for the 2N wire should be a lower value than the 4N wires due to its lower melting temperature. The FAB consistency for all three types of wires was within the specified range. Stiffer wires (types 1 and 3) needed higher USG power than a softer wire (type 2) to deform the ball after impact and achieve equivalent ball size and ball shear responses. Longer bond time was also needed for the low-*k* material compared to the SiO_2 material, to overcome the energy loss due to the compliance of the low-*k* material. Pad damage on the low-*k* device was proportional to bulk material hardness. The soft 4N (99.99% purity) wire required lower USG power to achieve the bonding specification, and was the most suitable wire to be used in the wire-bonding process for the low-*k* device.

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