Various Adhesives for Flip Chips

Z. W. Zhong
e-mail: mzwzhong@ntu.edu.sg
School of Mechanical and Production Engineering,
Nanyang Technological University,
50 Nanyang Avenue,
Singapore 639798,
Republic of Singapore

Flip chips using various adhesives were studied. The assembly yields using nonconductive adhesive and anisotropic conductive film investigated were 97% and 100%, respectively. A packaging process using anisotropic conductive paste with a 100% packaging yield was developed. All the packages passed various reliability tests such as burn in, artificial sweat and humidity tests, and temperature cycling tests. The reliability of the packages was 100% meeting the requirements for an industrial application. A stud bump bonding process with reduced process steps was proposed. Curing of conductive adhesive and underfill epoxy was not required, resulting in reduced packaging time.
[DOI: 10.1115/1.1846064]

1 Introduction

Many simple processes for flip chip assemblies at low costs have been developed [1–5]. There are many options to select from for a particular application of flip chip technology. These include lead-free solder, gold, polymer, etc., as the bump material to meet the requirements of applications. The substrate material can be glass, ceramics, FR-4, flex, etc. A solder alloy may be used to provide electrical interconnection and an underfill epoxy selected from many products available in the market to provide mechanical bonding of the flip chip to the substrate. An adhesive material can also be used as the electrical and/or mechanical bonding material, if gold bumps are selected to use. Electronics packaging engineers have an increasing selection of possible flip chip assembly processes, based primarily on cost, reliability and complexity.

Adhesive materials used in flip chip assemblies include anisotropic conductive adhesive (ACA), nonconductive adhesive (NCA) and isotropic conductive adhesive (ICA). ACA materials have two forms: film form (ACF) and paste form (ACP). Flip chip attachment with ACP, ACF or NCA has fewer process steps compared with other flip chip processes [6].

Flip chip attachment using gold bumps with adhesive is a solderless and low temperature flip-chip-mounting method. For many applications where high temperature is not desirable and reflow of a solder alloy is not allowed, flip chip using gold bumps with adhesive can be a solution. The demand for elimination of alpha emission, environmental requirements, requirements for gold bumps with fine pitch, applications of flip chip on glass (liquid crystal displays), etc. can be other reasons for choosing flip chip assembly processes using gold bumps with adhesive.

ICA can be used in the stud bump bonding (SBB) process that was invented as a solderless flip-chip-mounting method for high-density mounting of bare chips on glass epoxy or glass polyimide resin printed circuit boards. It was claimed that the process was inexpensive and reliable [1,7]. The gold bumps are formed with gold wire, using a modified wire bonding method. The stud bump has a two-stage construction, which helps transfer electrically conductive epoxy to the gold bump and is critical in preventing the spreading of the conductive epoxy. Cleaning is not required before the underfill is applied. The process is reworkable before curing of the underfill epoxy. If a defect is found before underfilling, the flip chip can be easily removed at room temperature and replaced with a new chip without the need to clean the terminals on the substrate [8].

This paper discusses flip chips on FR-4 and ceramics using NCA, ICA, ACF, or ACP. Several ACF and ACP materials with different types of adhesive resin and conductive particles and a few NCA and ICA materials were investigated. Design of experiments was carried out using the fractional factorial technique. Flip chips were assembled on test vehicles for various reliability tests. The reliability performance of the processes was compared.

The SBB process was evaluated for a flip chip in package application. A SBB packaging process having reduced process steps compared with the typical SBB process was proposed. Several issues affecting the assembly are also discussed in this paper.

2 Flip Chip on Board Using NCA

The reliability tests conducted for flip chips using NCA or ACF included temperature cycle test-1 ($-20°C/+60°C$) and test-2 ($-30°C/+100°C$), temperature humidity test [25°C/55°C, 95% relative humidity (RH)], artificial sweat test (38°C in an artificial sweat environment), drop test (from 170 cm height), and temperature behavior test ($-10°C/+70°C$). The test die used for the evaluation trials using NCA or ACF had a size of 3.5 mm $\times$6.0 mm, a minimum terminal pitch of 310 μm, and 33 gold bumps. The gold bump had a size of 100 μm$\times$100 μm. The substrate boards were multilayer rigid flex with gold pads.

A typical flip chip attachment using NCA is simple, and involves only two process steps: NCA placement, and integrated circuit (IC) placement and bonding. This process can give reasonable reliability and high assembly yield, when the parameters for epoxy placement (dispensing volume and pattern, shelf life of the epoxy) and bonding conditions (bonding force, temperature and time, cooling temperature) are optimized.

An L_{18} orthogonal array was selected for the DOE. Seven parameters (dispensing volume and pattern, shelf life of the epoxy, bonding force, temperature and time, cooling temperature) with three levels and one parameter (surface cleanliness) with two levels were investigated in the experiments. Eighteen experiments with four runs for each experiment were conducted, and the in-circuit voltage and functional tests were performed after the bonding experiments.

The analysis of variance (ANOVA) technique was used to establish the relative significance of the individual parameters. The ANOVA analysis revealed with 99% confidence that dispensing volume and pattern of the NCA, and bonding force and temperature, were the important parameters significantly affecting the assembly yield.

Based on the DOE results, the settings for five parameters were determined. However, the other three parameters needed further investigation. This was because the DOE was performed using the fractional factorial design technique, which could significantly reduce the number of experiments. One drawback of this technique was that some interactions of the factors investigated might not be distinguished completely from the effects of individual factors. Therefore, another DOE was carried out to focus on investigation of only three parameters whose settings could not be determined in the first DOE having eight parameters. After the two DOE analyses, the settings for all eight parameters were determined.

Manuscript received January 7, 2004; revision received July 27, 2004. Review conducted by: Y. C. Chan.

Table 1 Advantages and disadvantages of a flip chip process using adhesive compared to a typical flip chip process using solder with underfill epoxy

Advantages	Disadvantages
• Solderless process, without alpha emission and lead • Lower process temperature ($<200°C$) • Underfilling not required and fewer process steps (only 2 or 3) • Cleaning not required • ACF and ACP processes are reworkable	• Higher contact resistance • Lower current • Having no self-alignment effect • Special bonding machine needed to apply force, heat and accurate allighment • Gold bumps are more expensive than solder bumps

Confirmation and yield testing experiments were then conducted. The assembly yield was found to be over 97%. Failure analysis helped to further improve the assembly yield.

All of the samples tested passed the temperature cycle test-1, the temperature behavior test, the temperature humidity test and the drop test. Eighty percent of the tested samples passed the artificial sweat test; 95%, 90%, 85% and 70% of the samples passed 84 cycles (1 week), 168 cycles (2 weeks), 336 cycles (4 weeks) and 588 cycles (7 weeks) of the temperature cycle test-2, respectively.

Table 1 shows advantages and disadvantages of a flip chip process using gold bumps with NCA, ACF, or ACP compared to a typical flip chip process using eutectic solder bumps with underfill epoxy.

3 Flip Chip on Board Using ACF

Six ACF materials were evaluated. The ACFs have different types of conductive particles and densities. Preliminary studies were carried out to select ACF materials. Bonding tests, functional tests, temperature cycling tests and artificial sweat tests were conducted to evaluate the ACF materials and the process. The dies and substrate used were the same as those used for the NCA process.

To optimize the bonding parameter settings, DOE was performed. Three ACF materials were selected for the DOE runs because they did not produce any failures in the preliminary studies. Four factors were selected and three levels for each factor were determined. There were a total of nine experiments and four runs for each experiment in this DOE using an L_9 orthogonal array.

The attribute frequency for each level or each interaction was calculated based on the in-circuit voltage and functional test results. The best combination of parameter settings and material was determined. Confirmation and yield testing experiments were then conducted. The assembly yields were 100%.

All of the samples assembled during the yield runs passed temperature cycle test-1, the temperature behavior test, the temperature humidity test and the drop test. Ninty percent of the tested samples passed the artificial sweat test; 95% of the samples passed 336 cycles (four weeks) of temperature cycle test-2. The assembly yield and the reliability performance of the ACF process were better than those of the NCA process.

Although the assembly yield in this study with a sample size of a few hundreds was 100%, the yield for a mass production on a workshop floor may not be 100%. In the case that the cost for rework is lower than that of the product, reworkable mounting processes are desired.

An ACF process is reworkable. Rework using the method recommended by ACF manufacturers was evaluated first. The IC was heated at approximatly 180°C, twisted and removed. However, it was very difficult to completely remove the cured ACF. Cleaning with acetone was used as recommended, but this did not work. Therefore, after the IC was removed, another piece of the same ACF was added on the first cured ACF layer. Then, another cycle of pre-bonding and final bonding was carried out, as shown in Fig. 1. Studies revealed that the yield of this rework process was 100% and the first cured residual ACF did not affect the rework yield. Therefore, the steps to remove and clean the first cured ACF were not required.

4 Flip Chip in Package Using ACP

The test die used for the evaluation trials had a size of 3 mm $\times$4.6 mm, a minimum terminal pitch of 220 μm, and 22 gold bumps. The gold bump had a size of 100 μm$\times$100 μm. The substrate boards were multilayer ceramics with gold pads. The reliability tests conducted for flip chips using ACP included temperature cycle test-3 ($-30°C/+70°C$), temperature humidity test (25°C/55°C,95% RH), temperature cycle test-4 ($-40°C/+125°C$), artificial sweat test (38°C in an artificial sweat environment), and drop test (from 170 cm height).

DOE was conducted using the fractional factorial technique. A modified L_8 orthogonal array [9] was selected for the DOE. There were a total of eight experiments and five runs for each experiment in this DOE. Table 2 shows the details of the DOE.

The one factor with four levels was the adhesive material. Two ACP, one ACF and one NCA materials were the four levels. The important bonding parameters and laser marking were the other four factors. The differences of the two levels of bonding time ($t1$ and $t2$), temperature ($T1$ and $T2$) and force ($F1$ and $F2$) were 30 s, 10°C and 10 N, respectively.

Inspection tests were conducted after packaging experiments. Only one failure was produced using the condition of Experiment 1. The packaging yield using the conditions of Experiments 2–8 was 100%. This means that the flip chip attachment using any of the NCA, ACF and ACP materials investigated can produce 100% assembly yield.

A temperature cycling test ($-30°C/+60°C$) was conducted using all the samples that passed the inspection. A further temperature cycling test ($-40°C/+125°C$) was conducted using 24 samples (three samples from each DOE experiment) that passed the first temperature cycling test to further compare the reliability performance of the samples using the adhesives. There were three reasons for conducting these tests. First, after intensive research, it was not a problem anymore at that time to assemble flip chips using any of the materials to achieve 100% assembly yield. The target was to obtain 100% reliability. Second, flip chips using ACAs usually had reliability problems with temperature cycling and humidity tests [6]. Third, from our previous experience and a preliminary study for this industry application, if the packages could pass the temperature cycling tests, they could also pass

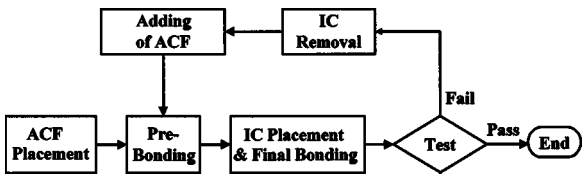

Fig. 1 The rework procedure developed for ACF processes

Table 2 Details of the DOE using a modified L_8 array

Experiment	Adhesive material	Bonding time	Bonding temperature	Bonding force	Laser marking
1	ACP 1	$t1$	$T1$	$F1$	With
2	ACP 1	$t2$	$T2$	$F2$	Without
3	ACP 2	$t2$	$T1$	$F1$	Without
4	ACP 2	$t1$	$T2$	$F2$	With
5	ACF 1	$t1$	$T2$	$F1$	Without
6	ACF 1	$t2$	$T1$	$F2$	With
7	NCA 1	$t2$	$T2$	$F1$	With
8	NCA 1	$t1$	$T1$	$F2$	Without

other reliability tests required for the application. This was because the encapsulation helped to protect the packages from moisture, etc.

Analysis of the DOE runs was performed to determine parameter settings and select the adhesive material. Pareto analysis [10] was carried out. The estimated attribute frequencies of failure and the estimated effects [11,12] of the five factors on the estimated failure frequencies were calculated. The results revealed that the most significant factor was the adhesive material selection and the most insignificant factor was laser marking.

After the analysis, ACP 2, $T2$, $F2$ and $t1$ were determined to be the adhesive material, bonding temperature, force and time, respectively. The final combination of the important factors was the same parameter setting of Experiment 4. Therefore, confirmation runs could be omitted in this study.

Yield runs were carried out using the parameter settings determined after the DOE analysis. The packaging yield of the process was 100%. The reliability tests required for the application were conducted. No failure occurred. The flip chip packages attained 100% reliability required for the application.

For research purposes (not for the industrial application requirements), extended temperature cycling test-4 ($-40°C/+125°C$) was conducted using the samples that already passed temperature cycling test-3 ($-30°C/+70°C$, 112 cycles). The reliability performance of the packages was quite satisfactory: 100% of the tested samples survived 836 cycles of temperature cycling test-4 (required cycles for the application were 30 cycles); 95%, 85% and 80% of the samples survived 1401, 2266 and 4329 cycles of the test, respectively.

An ACP process is also reworkable. A rework procedure for an ACP process, as shown in Fig. 2, was developed. After the IC was removed, more ACP material was added on the substrate site and another IC was assembled. Studies revealed that the yield of the rework process was 100%. And the residual first cured ACP volume did not affect the rework yield. Therefore, the steps to remove and clean the first cured ACP were not required.

5 SBB Processes

The test bare die used had a size of 3 mm×4.6 mm, a minimum terminal pitch of 220 μm, and 22 aluminum pads as terminals without bumps. The pad had a size of 76 μm×76 μm. The gold bumps were formed using a wire-bonding machine. The substrate used had 100 circuitry sites for mounting the bare dies. The substrate boards were multilayer ceramics with gold pads.

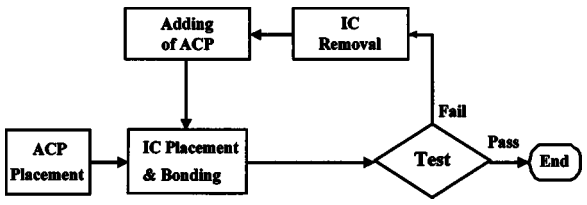

Fig. 2 The rework procedure developed for ACP processes

For this application of flip chip on ceramic substrates, the following standard SBB assembly steps were used for trials first:

1. stud bump leveling;
2. conductive adhesive dipping;
3. IC placement;
4. curing of conductive adhesive;
5. underfilling;
6. curing of underfill epoxy;
7. encapsulation;
8. curing of encapsulant; and
9. dicing.

The gold bumps were leveled by applying force. After dipping into a silver-filled conductive adhesive, the flip chips were placed onto ceramic substrates. Curing of the conductive adhesive was carried out at 120°C for 2 h in a curing oven. Underfill was applied by dispensing an epoxy on the sides of the chip. The substrate was kept at 60°C during underfilling. Curing of the underfill was then performed at 100°C for 2 h in the curing oven. An epoxy-based encapsulant was dispensed on the tops and sides of the flip chips. Curing of the encapsulant was also conducted at 100°C for 2 h in the curing oven. Dicing was carried out to obtain individual packages.

The standard SBB process works well for many applications, especially when the substrate is very flat, such as the glass substrate in flip chip on glass applications. However, it has more process steps compared with the flip chip mounting processes using ACF, ACP, NCA [6,13]. In the application of this study, the standard SBB process involved separately three process steps for curing of the conductive adhesive, underfill epoxy, and encapsulation epoxy, requiring in total 6 h for curing and more hours for cooling.

In addition, in the industrial application targeted, the pad surfaces on the multiple-layer substrate were not flat and had a lack of planarity at the initial development stage. It was found that many samples had open circuit interconnections after curing of the conductive adhesive. To solve the problem, one method was to improve the coplanarity of the pad surfaces on the multiple-layer substrate. This could be done by the substrate manufacturer. Another method was to develop an alternative SBB process that could work well even if the surfaces of the substrate pads were not flat.

For these two reasons, instead of the standard process, a modified process flow shown in Fig. 3 was used. The proposed assembly steps became:

1. epoxy placement;
2. stud bump leveling;
3. conductive adhesive dipping;
4. IC placement and bonding;
5. encapsulation;
6. curing of encapsulant; and
7. dicing.

A snap-cure-type epoxy was first dispensed onto the substrate. Next, the gold bumps were leveled and conductive adhesive dip-

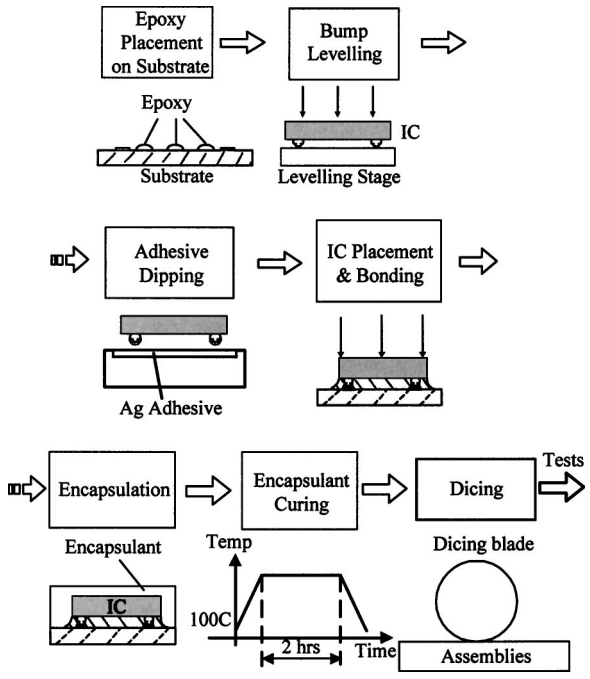

Fig. 3 A proposed SBB packaging process with reduced process steps

ping was performed. The IC with dipped conductive adhesive was placed onto the bonding site. Heat and pressure were then applied. The step of curing of underfill epoxy in a curing oven was not required. Furthermore, because an encapsulation curing process was conducted in the application, the separate curing step for the conductive adhesive could also be omitted.

This SBB process has fewer process steps compared with the typical SBB process. When the assemblies were put in the oven to cure the encapsulant, the epoxy dispensed before bump leveling and the conductive adhesive, which were incompletely cured during bonding, would also be further cured. The two separate steps of curing of the conductive adhesive and of the underfill epoxy, that in total needed 4 h for curing and more hours for cooling, were not required. This proposed process therefore resulted in shortened packaging time.

Furthermore, during bonding, each pair of gold bump and pad was slightly deformed to contact to each other more, due to the heat and pressure applied. After bonding, the snap-cure-type epoxy would hold the bumps in contact with the corresponding pads. Therefore, the proposed process also improved assembly yield although the pad surfaces on the multiple-layer substrate were not flat and had a lack of planarity at the initial development stage.

6 Conclusion

Flip chip on board using gold bumps with NCA or ACF was studied. The assembly yields of the NCA and ACF processes were 97% and 100%, respectively. A number of reliability tests were also carried out. The reliability performance of the ACF process was better than that of the NCA process.

A reliable flip chip packaging process using gold bumps and ACP was developed. The packaging yield was 100%. All of the packages assembled during the yield runs passed various reliability tests. The reliability of the packages was 100% meeting the requirements for an application.

An SBB packaging process with reduced process steps has been proposed. The two separate steps of curing of conductive adhesive and underfill epoxy, that in total needed 4 h for curing and more hours for cooling for the targeted application, were not required. This process therefore resulted in a reduced packaging time.

References

[1] Lau, J. H., 1995, *Flip Chip Technologies*, MacGraw–Hill, New York.
[2] Kloeser, J., Kutzner, K., and Gross, K. 1997, ''A New Production Line for Low Cost Flip Chip Assembly,'' *Proceedings of the Technical Program, Surface Mount International, San Jose*, CA, pp. 257–266.
[3] Zhong, Z., 2001, ''Development of a Reliable Packaging Process for Flip Chip on Ceramics,'' Microelectron. Int., **18**(1), pp. 19–22.
[4] Zhong, Z., 2001, ''Flip Chip Assemblies Using Gold Bumps and Adhesive,'' Microelectron. Int., **18**(3), pp. 15–19.
[5] Zhong, Z., 2001, ''Reliability of Flip Chips on FR-4 Assembled with Reduced Process Steps,'' Circuit World, **27**(3), pp. 26–30.
[6] Zhong, Z., 1999, ''Assembly and Reliability of Flip Chip on Boards Using ACAs or Eutectic Solder with Underfill,'' Microelectron. Int., **16**(3), pp. 6–14.
[7] Bessho, Y. et al., 1990, ''Chip-On-Glass Mounting Technology of LSIs for LCD Module,'' *IMC'90*, pp. 183–189.
[8] Potter, B., 1998, ''Flip Chip Bonding Primer,'' Circuits Assembly, September, pp. 72–75.
[9] Ross, P. J., 1988, *Taguchi Techniques for Quality Engineering*, McGraw–Hill, New York.
[10] Ott, E. R., 1990, *Process Quality Control*, McGraw–Hill, New York.
[11] Montgomery, D. C., 1991, *Design and Analysis of Experiments*, Wiley, New York.
[12] Cobb, G. W., 1998, *Introduction to Design and Analysis of Experiments*, Springer, New York.
[13] Zhong, Z., 2001, ''Stud Bump Bond Packaging with Reduced Process Steps,'' Soldering Surf. Mount Technol., **13**(2), pp. 35–38.