

## Overview of wire bonding using copper wire or insulated wire

Z.W. Zhong\*

School of MAE, Nanyang Technological University, 50 Nanyang Avenue, Singapore 639798, Republic of Singapore

### ARTICLE INFO

#### Article history:

Received 19 January 2010

Received in revised form 28 May 2010

Accepted 10 June 2010

Available online 6 July 2010

### ABSTRACT

Wire bonding using copper or insulated wire leads to many advantages and new challenges. Research is intensively performed worldwide, leading to many new findings and solutions. This article reviews recent advances in wire bonding using copper wire or insulated wire for advanced microelectronics packaging. Journal articles, conference articles and patents published or issued recently are reviewed. The benefits and problems/challenges related to wire bonding using copper wire or insulated wire such as wire open and short tail defects, poor bondability for stitch/wedge bonds, oxidation of Cu wire, and stiff wire on weak support structures, are briefly analyzed. A number of solutions to the problems and recent findings/developments related to wire bonding using copper wire or insulated wire are discussed. With the references provided, readers may explore more deeply by reading the original articles and patent documents.

© 2010 Elsevier Ltd. All rights reserved.

### 1. Introduction

Although wafer-level packaging [1], tape automated bonding [2] and flip chip [3–6] technologies are also increasingly used, wire bonding is the most widely employed IC (integrated circuit) packaging technology in the industry [7]. This is because ultimately cost rules. An engineer must consider costs, not only package performance. Because of its flexibility and being the lowest-cost IC packaging technology, wire bonding dominates more than 90% of the IC packaging market. It also has an established huge base of equipment, materials and manpower [8].

This article reviews recent advances in wire bonding using copper wire or insulated wire for advanced IC packaging. Journal articles, conference articles and patents published or issued recently are reviewed. The new challenges are briefly analyzed, and the solutions to the problems and recent findings/developments are discussed.

### 2. Wire bonding

The advances of IC fabrication technologies bring new challenges to wire bonding, such as increase in I/O numbers, reduction in cost, bond pad pitch (BPP) and wire size, emergence of alloyed gold wires and copper wires, and reliable wire bonding of ultra-fine-pitch low- $k$  devices [9–13].

Fig. 1 shows the wire bond pitch values plotted based on those for chip to next level interconnect potential solutions or chip to package substrate technology requirements published in the ITRS [14] reports. The values were timely updated when the reports were published. The trend has been clear: the bond pitch values become smaller with the year of production.

The industry requires wire bonding on increasingly finer pitch pads [15]. Ultra-fine-pitch wire bonding is needed for small and light packages [16]. Electronic devices with high circuitry integration of chips require high I/O numbers and reduced BPPs [17]. The demand for reducing manufacturing costs and improving performance is also driving low-cost packaging for fine pitch and high I/O devices [18].

Ultra-fine-pitch wire bonding leads to many challenges, as shown in Fig. 2 [17]. Capillaries must have very small tip diameters and holes. When the capillary tip diameter decreases, the stitch bond size decreases, resulting in reduced bondability [19]. The surface hardness and roughness of the substrate become important. Small wire sizes also must be used, causing problems such as reduced bonding strength, wire short and stitch bond problems [17]. Thinner wires have lower conductance, and are weaker, less stiff, and more difficult to handle [20]. After thermal aging, the ball bonds formed using thin gold wires have voids and intermetallic compound growth [21]. The main challenge for wire bonding on staggered pads is to consistently form low and high looping profiles without wire shorting, while the main challenge for fine-pitch wire bonding on in-line pads is to achieve ball bond strength stability with reduced ball sizes [22].

The permittivity of interconnection insulators must be reduced for good circuit performance [23]. The industry is replacing SiO<sub>2</sub>

\* Address: School of Mechanical and Aerospace Engineering, Nanyang Technological University, 50 Nanyang Avenue, Singapore 639798, Republic of Singapore. Tel.: +65 6790 5588; fax: +65 6791 1859.

E-mail address: [mzwzhong@ntu.edu.sg](mailto:mzwzhong@ntu.edu.sg).

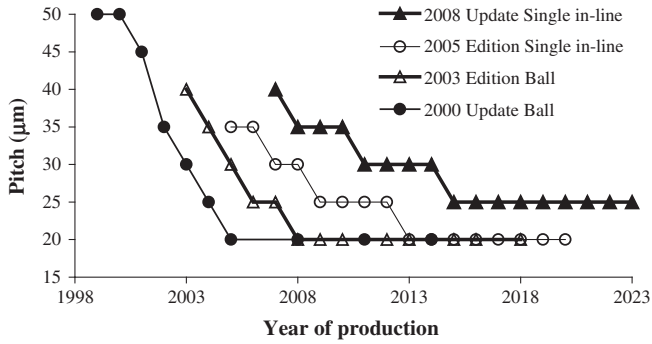


Fig. 1. Wire bond pitch values plotted based on those for chip to next level interconnect potential solutions or chip to package substrate technology requirements published in the ITRS [14] edition/update reports.

with a low-*k* dielectric and the Al conductor with Cu [24], because of many advantages [25–27]. An approach to obtain ultra-low-*k* dielectrics is to incorporate porosity into the existing low-*k* materials [27,28]. However, this introduces new challenges to the mechanical integrity of IC devices [29] and wire bonding [9,12,30–42]. Cu electromigration is a key issue, limiting the lifetime of advanced interconnection systems [43]. A critical challenge in the integration of porous low-*k* materials is their degradation during different processes [44]. Such materials have a low elastic modulus, low fracture toughness, and poor adhesion to capping and liner layers [45,46]. IC packaging interaction also becomes a critical reliability issue because of mechanically weak low-*k* materials [47]. A combination of a low-*k* material and a hard wire would introduce new challenges to wire bonding [48]. A low-*k* material requires longer wire bonding time to overcome the energy loss due to the compliance of the low-*k* material, compared to the SiO<sub>2</sub> material [49].

There are more challenges in wire bonding of “ultra-fine-pitch” low-*k* devices [13]. The bonding process is even more sensitive, during which relatively high reject rates due to metal pad peeling are often observed [17]. Obtaining reliable ball bonds becomes a major challenge, as higher parameter settings result in metal pad peeling while lower parameter settings lead to non-sticking. Small wire sizes must be used, leading to stitch bond problems: the tail bond may be detached away during the wire termination process, resulting in wire open or non-sticking on lead. The process window is narrow, and the capillary design becomes even more complex [50]. The combination of a low-*k* ILD with a fine pitch brings challenges to wire bonding in terms of process manufacturability and reliability [25,51,52].

Bare gold wires are the most widely used in wire bonding, but Al–Si wires [53], Cu wires and insulated wires are also employed

for chip packaging. In this article, the benefits and problems/challenges of wire bonding using copper or insulated wire, and the solutions and recent research findings are discussed.

### 3. Wire bonding using copper wire

#### 3.1. Benefits of wire bonding using copper wire

Wire bonding using copper wire offers many advantages over wire bonding using gold wire, which are summarized in Table 1.

Copper wires have better electrical and thermal properties than gold wires. Copper is ~25% more conductive than gold, accounting for increased power rating and better heat dissipation. Higher electrical conductivity results in a higher speed and less heat generation. This is an important factor to the development of high power, high performance and fine-pitch devices using small-diameter copper wire to accommodate small pad sizes [54–59].

Compared to gold wires, tempered and annealed copper wires have higher tensile strength and lower wire sag, and better loop stability is obtained during encapsulation [60]. Copper wires have excellent ball neck strength after the ball formation [55]. Compared to gold wires, the higher stiffness of copper wires is more suitable to fine pitch bonding [56,61], leading to better looping control and less wire sagging for ultra-fine-pitch wire bonding [62]. Using Cu wire can be a solution to the wire short problem caused by small wire sizes, besides other solutions such as using insulated wire [63] and having varying loop heights [7]. High stiffness and high loop stability of Cu wire lead to better wire sweep performance during encapsulation or molding for fine-pitch devices, and can help to achieve longer/lower loop profiles [54,55,57].

In addition, there is very little void formation in the Al–Cu system compared to the Al–Au system. The growing speed of the intermetallic compound (IMC) between Al and Cu is much lower than that between Al and Au, leading to lower electrical contact resistance, less heat generation, and better reliability and device performance, compared to Au/Al bonds [55–57,61]. The inter-diffusion between an Au bond and Al pad results in IMC growth and void formation, affecting the drain-to-source on-resistance in power MOSFET devices. Cu–Al bonds provide much more stable drain-to-source on-resistance because of the small inter-diffusion rate of Cu–Al phases, and do not have the Kirkendall void problem widely found in Au wire bonding. Cu wire is more suitable for bonding in MOSFET devices [60]. Copper wire can also be directly bonded on bare Cu lead-frames and BGA substrates, saving cost and time because of elimination of the plating process [62].

However, the primary driver for using copper wire is cost, without which copper wire bonding with many new challenges and problems discussed in the next section, would not have been considered. The price of gold has greatly increased, fueling the demand

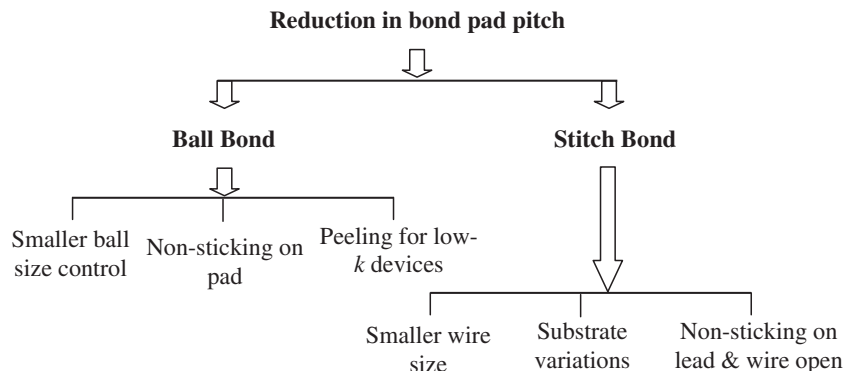


Fig. 2. Challenges resulted from the reduction in bond pad pitch [17].

**Table 1**  
Advantages of copper wires over gold wires and challenges of wire bonding with copper wires [30,54–57,60–62,65–69].

Advantages	Challenges
1. A solution to the wire short problem	1. A larger strain-hardening effect at a higher strain rate
2. Better thermal properties	2. Additional bonding parameters for using forming inert-gas
3. Better electrical properties	3. Easy to be oxidized in air
4. Can be bonded on bare Cu substrates	4. High pressure is put on pad structures, which can contain low- <i>k</i> materials having very low stiffness
5. Excellent ball neck strengths	5. Lower strengths of annealed wire resulting in breakage
6. Higher stiffness	6. Minimizing the Al squeeze of bond pads during bonding
7. High loop stability and better looping control	7. Needs more ultrasonic energy and a higher bonding force, which can damage the Si substrate, form die cratering and induce cracking and peeling of the bonding pad
8. Low growing speeds of IMC	8. Poor bondability for stitch/wedge bonds
9. Lower cost	9. Wire open and short tail defects
10. Small inter-diffusion rates of Cu–Al phases	
11. Very little void formation in the Al–Cu system	

for high-volume wire bonding using copper wire, which can significantly save cost because of the lower raw material cost [57]. The price of copper wire is 10–40% of that of gold wire [56,61], and copper is not subject to sudden price fluctuations in the market [55]. Copper wire now is much cheaper than gold wire. Currently, a 500-m spool of 20- $\mu\text{m}$  gold wire costs \$200, about 1000% of the cost of comparable Cu wire [64].

### 3.2. Challenges in wire bonding using copper wire

Despite its many benefits discussed in the previous section, copper wire has not yet been widely used like gold wire, as copper wire bonding also introduces many new challenges summarized in Table 1.

One challenge is to minimize the Al squeeze of bond pads during bonding, demanding the Cu ball to have a lower yield stress. Impurities in pure copper resist slip, increase the flow strength and the FAB (free air ball) hardness, and demand more energy to deform the Cu ball, leading to more Al squeeze. There is conflicting demands for a softer FAB but higher wire strengths and stiffness [65].

Because copper wires are harder and stiffer than gold wires, copper wire bonding needs higher bonding force and more ultrasonic energy, which may damage the Si substrate, form die cratering [61], and cause cracking and peeling of the bonding pad [56]. A stage temperature of 150–200 °C is also needed for copper wire bonding [55]. To improve stitch bondability, higher parameter settings must be used, leading to heavy cap marks and potential short tails or wire open. Therefore, copper wire bonding often has poor process control, wire open and short tail defects, and low stitch pull readings [62]. Because Cu exhibits a larger strain-hardening effect at a higher strain rate [66], the effects of the process parameters on the hardness of Cu FABs need to be investigated [67]. As-drawn copper wire has higher hardness and strengths, but its lower ductility reduces the reliability of bonding. The lower strength of the annealed wire leads to breakage [68].

Copper can be easily oxidized in air, and thus copper wire bonders must have additional tools to prevent copper oxidation [61]. Additional cost of forming inert-gas must be considered [62] and additional bonding parameters for using forming gas have to be optimized [55]. A forming gas mixture of 95%  $\text{N}_2$ /5%  $\text{H}_2$  has been shown to be the best choice [57]. Oxidation of Cu wire also results in poor bondability for stitch bonds [69], which can lead to increased non-sticking rates. Thick oxide can prevent a good wedge bond when a spool of Cu wire is on the bonding machine for a long time, because the longer copper wire has been removed from its package, the thicker the oxide becomes [57]. Two failure modes often occur in wedge bonding of copper wire: lifting-off of the wedge bond and uncontrolled wire breakage during tail formation [56].

Copper wire bonding of ultra-fine-pitch low-*k* devices may lead to many benefits, but this combination also brings most of the discussed challenges together, due to the individual effects of “ultra-fine-pitch”, “low-*k*” and “copper wire” on wire bonding and their interactions. Compared to the wire bonding using gold wire on conventional non-ultra-fine-pitch pads, a harder thin copper wire must be deformed on a mechanically weaker pad structure with a smaller pad size using a capillary with a smaller tip diameter and a possibly weakened bottleneck. This deformation must be properly controlled to consistently obtain desired bonded ball diameters and heights with very tight tolerances and obtain reliable ball shear and wire pull readings without such defects as bond lift, non-sticking on pad, wire open and metal pad peeling. Furthermore, the stitch bond problems in copper wire bonding must also be solved. To meet all of these stringent requirements in a mass production environment is very challenging.

### 3.3. Recent findings and solutions for copper wire bonding

Research on copper wire bonding is extensively performed worldwide [70] to deal with the challenges and solve the problems so as to fully benefit from its many advantages, leading to many new findings and solutions to the problems, which are summarized in Table 2.

After annealing, single-crystal Cu wires were bonded [55] on Au (1–2  $\mu\text{m}$  thick) and Al (2  $\mu\text{m}$  thick) surfaces without gas protection, and  $\text{CuAl}_2$  was found at the Cu/Al interface while AuCu and  $\text{Cu}_3\text{Au}$  IMCs were found at the Cu/Au interface. After thermal aging, Kirkendall voids were discovered at the Cu/Au interface. Annealed Cu wires exhibited tensile strength and elongation characteristics comparable to those of Au wires.

Investigations of the Cu-to-Si diffusion behavior and the IMC growth in wire bonds reveal that Au–Al IMC grows much faster than Cu–Al IMC [71,72]. Cu-to-Si diffusion is faster than Au-to-Si diffusion under the same annealing condition. With a TiW barrier layer adopted, Cu or Au diffusion to Si is decreased. Cu–Al IMC is thinner than Au–Al IMC at the bonding interface, which leads to better bond strengths and smaller electrical resistance.

Aging at 250 °C of Cu ball bonds [73] reveals that Cu/Al IMCs are mainly  $\text{Cu}_9\text{Al}_4$  and  $\text{CuAl}_2$ , with CuAl present in smaller amounts. Cu/Al IMCs form at the bond periphery and extend toward the bond center. Cavities grow from the ball periphery toward the bond center, and finally form a complete fracture between the ball bottom surface and the upper IMC layer. The IMC growth rate decreases gradually with the aging time and stops when the fracture completes. In another study [74], discontinuous  $\text{CuAl}_2$  IMCs were detected at the ball bond center and periphery. The IMCs were adjacent to smaller copper grains in regions subjected to higher stresses, indicating that localized stresses incorporated into the

**Table 2**  
Solutions and findings for reliable wire bonding with copper wire.

Findings and solutions	References
• Annealed Cu wires exhibited tensile strengths and elongation characteristics comparable to those of Au wires	[55]
• Higher bonding power and force are needed for the second bond than the first bond to have strong pull force readings	[56,75]
• Increasing the temperature can enlarge the bondability window and less bonding force can be used	[57]
• Lower bonding force and ultrasonic power can help minimize pad cratering	
• Slip was the major mechanism involved in the overall deformation of polycrystalline copper	[61]
• A new capillary with a new surface morphology results in satisfactory results in stitch pull and ball shear tests	[62]
• Higher purity copper wires have reduced grain numbers in FABs and have smaller flow stresses, requiring a smaller force to deform the ball and leading to less Al squeeze during bonding	[65]
• Having shorter firing time during FAB formation, providing sufficient inert-gas coverage and using a lower contact velocity are recommended to achieve a softer FAB and minimal stresses induced during the ball bond impact	[67]
• Use high EFO current with short firing time	[77,79]
• The initial temperature of the chip can improve the atomic reaction	[82]
• Decreased strengths and hardness of the HAZ resulted in breakage sites of the wires to be in the HAZ near Cu balls	[68,86]
• A secondary EFO method can be adopted to reduce the hardness of the Cu FAB to improve its bondability and reliability	[87,88]
• Pd-plated Cu wire demonstrated excellent bondability and reliability	[69,76]
• Higher forces are needed to form a Cu bond, resulting in higher stresses in the pad structure	[30,116]
• With a TiW barrier layer adopted, Cu or Au diffusion to Si is decreased	[71,72]
• Cu–Al IMC is thinner than Au–Al IMC at the bonding interface, leading to better bond strengths and smaller electrical resistance	
• Cu/Al IMCs are mainly $\text{Cu}_9\text{Al}_4$ and $\text{CuAl}_2$ , with CuAl present in smaller amounts	[73]
• Discontinuous $\text{CuAl}_2$ IMCs were detected at the ball bond center and periphery, adjacent to smaller copper grains in regions subjected to higher stresses	[74]
• Plasma cleaning of lead-frames before bonding significantly increases the tail breaking stability	[19]
• One method to reduce the stresses is to select a softer Cu wire type	[83–85]
• Another method is to decrease the ultrasound level	
• The asperity deformation is the most significant factor for good bonding	[89]
• Ultrasonic energy breaks the oxide film and deforms asperities, while the bonding force increases the asperity proximity	
• The Cu wire tail picks up Ag from the lead-frame during tail formation	[90]
• Preferable remnant Al after bonding should be more than half of the thickness of the Al bond pad	[91]
• The bonding position significantly affects the local stress near the bond, and the wire should be bonded at the pad center	[117]
• The stress is large if the pad size is close to the wire ball size	

Cu–Al interfacial region during bonding catalyze the IMC formation.

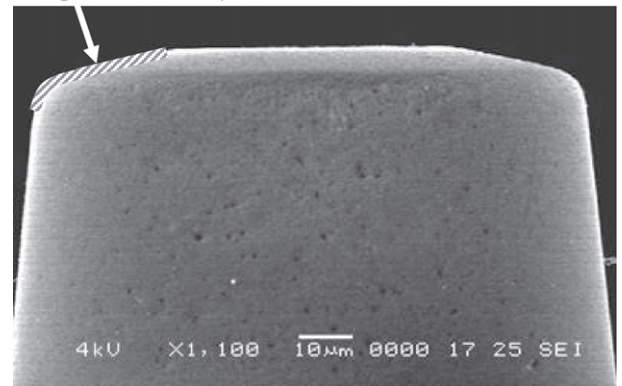
Investigation of copper wire ball bonding on an Al-metallized silicon substrate revealed that slip was the major mechanism involved in the overall deformation of polycrystalline copper, although twinning was also found in very limited bonds [61]. The shear force of the ball bonds did not degenerate after 1500 h at 200 °C, and had some extension of increasing, because of the interface diffusion of the bonds.

Cross section analyses after ultrasonic wedge bonding using Cu wire at ambient temperature on Au/Ni/Cu metallization of a PCB reveal a continuous interconnection between Cu wire and Au/Ni/Cu metallization [56]. Three common failure modes found are bond lifting-off from the metallization surface, bond break when the bond is deformed excessively, and wire break at the bond neck, which is the preferred mode indicating good bonding. Strong Cu wire wedge bonds on an Au/Ni plated Cu substrate are obtained by ultrasonic bonding at room temperature, achieved by the wear action induced by ultrasonic vibrations [75]. The ultrasonic power enhances deformation of the Cu wire because of the ultrasonic softening effect followed by the strain hardening of the Cu bond. Higher bonding power and force are needed for the second bond than the first bond to have strong pull force readings.

Bond integrity testing revealed that increasing the temperature could enlarge the bondability window and less bonding force could be used [57]. Lower bonding force and ultrasonic power could help minimize pad cratering. Cu ball bonds performed better than their Au counterparts in ball shear and wire pull tests.

As a solution to the poor stitch bondability due to surface oxidation, a new capillary has been developed with a new surface morphology. As shown by a curved line in Fig. 3 [62], the critical portion of a capillary tip has a direct impact on the stitch formation. To achieve good stitch bondability, the coupling effect between the capillary and the wire must be improved, by enhancing the morphology or texture of the capillary tip surface.

This portion shown by a curved line is critical.



**Fig. 3.** The critical portion of a capillary tip shown by a curved line has a direct impact on the stitch formation [62].

Bonding experiments with the new capillary were performed using 70- $\mu\text{m}$  and 100- $\mu\text{m}$  pitch BGA devices and 25- $\mu\text{m}$  copper wire, and satisfactory results were confirmed by stitch pull and ball shear tests. Fig. 4 [62] shows SEM pictures of the copper stitch bonds before and after the stitch pull test.

As another solution, electroplating of an oxidation-resistant metal on Cu wire was conceived to prevent surface oxidation [69,76]. Experiments revealed that electroplating of 0.1- $\mu\text{m}$ -thick Ni, Pd Ag or Au on Cu wire increased bond strengths, but produced problematic ball shapes except the Pd-plated Cu wire, which could produce the same ball shape as that of Au wire. Temperature humidity bias, temperature cycling and pressure cooker tests confirmed that the Pd-plated Cu wire demonstrated excellent bondability and reliability.

A study about the effect of wire purity on copper wire bonding reveals that higher purity copper wires have reduced grain num-

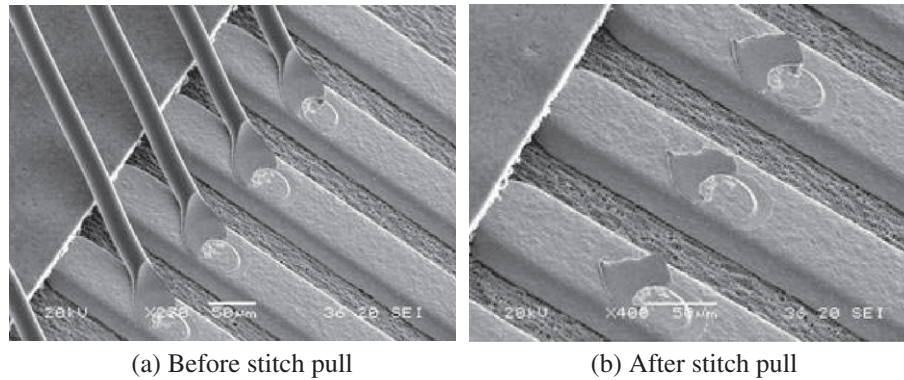


Fig. 4. SEM pictures of copper stitch bonds before and after a stitch pull test [62].

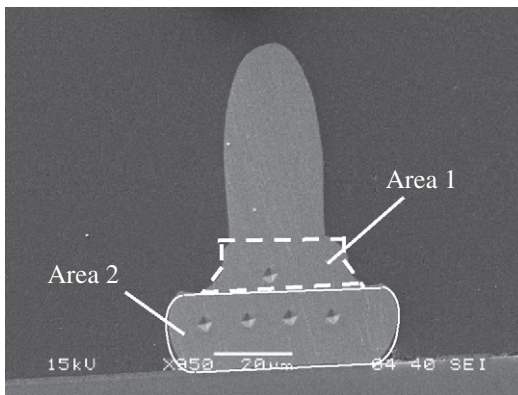


Fig. 5. Indentation locations for microhardness tests [67].

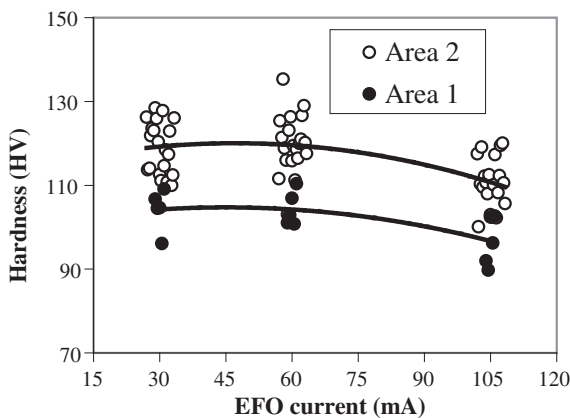


Fig. 6. Vickers hardness numbers (HV) of the ball bonds obtained using ultrasonic generator current = 90 mA, and contact velocity = 11.43  $\mu\text{m}/\text{ms}$  [67].

bers in FABs and smaller flow stresses, requiring a smaller force to deform the ball and leading to less Al squeeze during bonding. Al squeeze is caused by the shear stress during the ball deformation and the ultrasonic softening of the Al layer [65].

Hardness tests were performed to study the effects of EFO (electric flame-off) current levels on the microhardness of the Cu ball bonds. Fig. 5 shows an example of the indentations performed, and Fig. 6 illustrates the Vickers hardness numbers (HV) of the ball bonds [67]. The investigation reveals that the microhardness of the bonded balls depends on the EFO parameters, with FABs obtained using higher EFO current being softer. The lower hardness is attributed to the higher maximum temperature during the FAB melting.

Higher EFO current leads to a higher maximum temperature of the Cu FAB. Having shorter firing time during the FAB formation, providing sufficient inert-gas coverage and using a lower contact velocity are recommended to achieve a softer FAB and minimal stresses which are induced during the ball bond impact.

It is also recommended by another group of researchers to use high EFO current with short firing time for Cu wire bonding, because this reduces the risk of under-pad damage and benefits low loop heights. Significant softening of deformed Cu balls can be obtained, leading to 8% less force needed for the deformation of the same amount and an 8% reduction in under-pad stress. Higher EFO current strengthens the heat-affected zone (HAZ) and reduces its length [77], because of a higher recrystallization temperature [78]. If lower EFO current is used, the work hardening effect on FABs is stronger [79].

Copper wires become harder during the ball formation and bonding process [80]. Ball hardness depends on the location, the capillary geometry influences the flow pattern when the forces act on the grains relative to the slip plane, and different local strain rates, strain/strain rate gradients and grain orientations affect the ball hardening [81].

Copper oxidation can be prevented by providing sufficient shielding gas during the FAB formation. The bondability is determined by the slip area at the bonding interface, and the transfer from the slip area to entire slip is controlled by the levels of the bonding force and ultrasonic power. The initial temperature of the preheated chip can improve the atomic reaction [82].

Compared to Au ball bonds, Cu ball bonds have higher shear strengths, but the ultrasound level required for Cu bonding is higher, leading to higher stresses on bond pads and increased risks of under-pad damage [83,84]. One method to reduce the stresses is to select a softer Cu wire type. Another method is to decrease the ultrasound level by 10%, leading to a 15% reduction of shear strengths and a 9% reduction of the ultrasonic force. This decreases the extra stress with Cu wire by 42% compared to that with Au wire [83]. Using a lower bond force and a reduced ultrasound level can reduce the pad stress by 30% [85].

Investigations of the copper wire annealing effect on its mechanical properties found that with temperatures  $>200$  °C, copper wire had a fully annealed structure, its tensile strength and hardness decreased, and its elongation was significantly raised [68,86]. After EFO, the FAB microstructures of the wire were column-like grains, which grew from the HAZ to the Cu ball. Decreased strengths and hardness of the HAZs resulted in breakage sites of the wires to be in the HAZs near Cu balls.

A secondary EFO method [87] can be adopted to reduce the yield strength of Cu wire with the kink height of HAZ remained and to reduce the hardness of the Cu FAB. The bondability and reliability of Cu wire bonding can be improved [88].

During melting of a copper wire tip in air to form an FAB, oxidation of the wire occurs, leading to voids, flaws and asymmetric ball formation, while copper FABs formed in a forming gas atmosphere have a uniform, symmetric shape without flaws. The HAZ length of copper wires melted in a forming gas atmosphere is shorter than that melted in air. A shorter HAZ is associated with higher mechanical stability of copper ball bonds [74].

A weak tail bond can result in non-uniform tail lengths and FAB formation. The bonder stops before flaming off the tail, reducing the production throughput, if the tail bond is weak enough to loose before the clamps can close, resulting in the wire being blown out from the capillary. The cleanliness of bonding pads is important for using Cu wire. Plasma cleaning of the lead-frame before bonding significantly increases the tail breaking stability, and an average Cu tail breaking force >50 mN is obtained, comparable to that obtained using Au wire [19]. The standard deviation of the Cu tail breaking force is about two times that obtained using Au wire.

Studies of Cu wire bonding on metallized and plated materials such as Cu, Ag, Al, Au and Pd find that the asperity deformation is the most significant factor for good bonding [89]. Ultrasonic energy breaks the oxide film and deforms asperities, while the bonding force increases the asperity proximity. Soft Al with a lower asperity deformation is easier to be wire bonded than harder surfaces. Good adhesion can be achieved on bare and plated surfaces with surface roughness ( $R_a$ ) of 0.01–0.15  $\mu\text{m}$  and 0.02–0.6  $\mu\text{m}$ , respectively.

A study of silver pick-up during the tail formation has revealed that the Cu wire tail picks up Ag from the lead-frame. Ag is found on the FAB surface with the highest concentration on the grain boundaries. The Ag pick-up reduces the hardness of the Cu FAB by ~3% but does not significantly change the FAB diameter [90].

Cu wires of 3N and 5N were bonded on 1  $\mu\text{m}$ -thick Al bond pads, and the less-purity wire showed larger IMC coverage and ball shear values. After baking of 300 h, both types of bonded Cu wires consumed the remnant Al (~0.4  $\mu\text{m}$ ). For good reliability, the preferable remnant Al after wire bonding should be more than half of the thickness of the Al bond pad, so that Al would not be completely consumed [91].

Many factors affect the quality of wire bonds. Experimental and numerical approaches are often adopted to investigate wire bonding using copper wire. As discussed above in this section, bonding and testing experiments [92–98] are typically conducted to evaluate the performance of wire-bonded devices. On the other hand, numerical investigations are also widely performed because this approach can save time, cost and manpower for time-consuming experiments and tests [99]. Finite element analysis (FEA) is a useful method to investigate processes and discover facts [100–104]. There is an increasing research trend in applying FEA to wire-bonded packages [10,11,31,105–115], although articles reporting FEA of Cu-wire-bonded packages are still scarce.

As discussed in Section 2, the traditional configuration with  $\text{SiO}_2$  dielectric and Al interconnection layers is replaced with

low- $k$  dielectrics and Cu interconnection layers [116]. Numerical studies reveal that the yield stress of the wire bond determines the pressure on the pad structure [30]. Higher forces are needed to form a Cu bond, resulting in higher stresses in the pad structure. A stiffer capping redistributes the deformation over a larger area, leading to a smaller local deformation in the metal layer at the bond edge, and thus the stress peak decreases.

FEA of a Cu-to-Cu wire-bond forming process finds that the bonding position significantly affects the local stress near the bond, and the wire should be bonded at the pad center [117]. The stress is large if the pad size is close to the wire ball size. The bonding temperature also largely affects the stress.

#### 4. Wire bonding using insulated wire

##### 4.1. Benefits of wire bonding using insulated wire

As discussed in Section 2, small wire sizes have to be used for wire bonding because the bond pad pitches (BPPs) are being reduced. However, a problem with wire bonding using small wire sizes is that a wire may short to another conductive structure because of sweep, which may occur during encapsulation when the liquid encapsulant moves the soft wire toward the conductive structure [118]. Smaller size wires tend to have higher wire sweep and shorting rejects [119]. Using insulated wire can be one solution to this problem, besides using copper wire.

Insulated wires are traditionally and currently used in many applications such as coils used in electronics circuits, motors and transformers incorporated into a large variety of electrical devices, machines and cars [120]. Wire bonding using insulated wire was developed over 10 years ago, but was not popular because of the high processing cost and lack of sufficient market demands [17]. As IC packages become more complicated, wire bonding using insulated wire has market demands today and in the future, because wire sweep becomes a new problem due to the further reduction in BPPs and wire sizes.

Insulated wire was identified on the 2006 ITRS Roadmap as a potential solution to enable 25- $\mu\text{m}$  pitch wire bonding [121]. It is a cost-effective solution to enable complex package designs, enhance package performance, and improve the yield of high-density packaging [8]. It allows long wires, and wire sweep, touching and crossing, that were previously prohibited. Insulated wires can use existing platforms and wire bonding infrastructure, and should meet industry standard test specifications.

The benefits of wire bonding using insulated wire have been well known for many years, which are summarized in Table 3. Insulated-wire bonding can use the lowest-cost packaging infrastructure and reduce wire shorting rejects. With its area array capability using closely packed and crossed insulated wires, it can overcome the previous limitation of wire bonding that the interconnections are confined to the chip perimeter. It can directly

**Table 3**  
Benefits and challenges of wire bonding with insulated wire [8,16,119,122–126].

Benefits	Challenges
1. Allows use of the Z dimension and wasted space created by parallelism of bare wires	1. Damaged wire with a hole burned in the insulation layer
2. Allows wire sway, lower loops, sagging wires, wire sweep and longer wires	2. Frequent machine stoppages
3. Enables complex package designs and improves the yield of high-density packaging	3. Insulation layer pushed out to one side of the wire during molding
4. Enables flexible routing, simplified substrate and packaging of small dies	4. 'Kissing effect' after temperature cycling
5. Enables wire bonding with insulated fine gold or copper wire and low- $k$ pad structures	5. Low stitch pull readings
6. Is suitable for multi-row, ultra-fine-pitch and area array wire bonding	6. Non-sticking on lead
7. Is suitable for system in package, stacked dies and side-by-side chip-to-chip bonding	7. Weak tail bonds causing bonder stoppage
8. Prevents wire shorts and enables cross bonding	
9. Uses existing platforms and lowest-cost packaging infrastructure	

connect stack dies, and allow flexible routing without requiring a fan-out area. Wire bonding using insulated fine copper or gold wire on low- $k$  pad structures is also possible [8,16,119,122,123], and wire sway, low loops, sagging wires, wire sweep and long wires are not the limitations to production anymore [124].

#### 4.2. Challenges in wire bonding using insulated wire

In spite of many benefits of insulated-wire bonding, there were challenges and problems that had to be dealt with and solved before insulated wires could be widely used in wire bonding for advanced IC packaging. The challenges of wire bonding using insulated wire are summarized in Table 3.

Insulated wires cannot be bonded in the usual way for bonding bare wires. The electricity can jump to the ground through the insulation layer if a ground is not properly provided, burning a hole in the insulation layer and leading to damaged wire [125,126].

There is no concern with ball bonds, because the firing of the EFO to form a FAB melts the insulation layer on the wire ball [17], but the rest of the insulation layer is not melted and remains on the wire as the melting temperature of the insulation layer is higher than that of the wire [118]. It is to obtain reliable stitch bonds between the substrate leads and the insulated wire that poses a large challenge. Non-sticking on lead is a common problem with the stitch bonds [17,119]. Stitch bonds are often weak due to the insulation layer partially existing between the lead and the wire, preventing good adhesion. Insulated ultra-fine wire usually results in very low wire peel strengths [123]. Standard bond parameters used for bonding bare wires are not sufficient for bonding insulated wires with the equivalent pull strengths. Weak tail bonds can result in non-uniform tail lengths and non-uniform FAB formation [124]. There are frequent machine stoppages if non-sticking on lead happens [16] or if the tail bond is weak enough to become loose and the wire is blown out from the capillary [124].

Thicker insulation has a bondability issue in tearing off the insulation layer, while thinner insulation results in better bonding but leads to a so-called 'kissing effect' [16] after about 100 temperature cycling. Lower coating temperatures are good for wire bonding but may also cause the exposure problem. A lower insulation melting temperature results in the insulation layer pushed out to one side of the wire during molding with the bare wire exposed, potential to wire short.

#### 4.3. Solutions and recent findings for reliable insulated-wire bonding

Efforts made in the past to meet the challenges in insulated-wire bonding had limited success [122]. Recently, several articles and approved patents have been published, reporting new findings and good solutions for reliable wire bonding using insulated wire. They are briefly summarized in Table 4.

Insulated wire needs lower EFO current and a shorter EFO gap compared to bare wire to achieve optimal FAB quality. One development focus is to provide a coating material that easily cracks only at the stitch bond with available bonding parameters. Such a bonding method involves applying a high initial bonding force with low ultrasonic energy, applying a high initial impact during touch-down, and providing slight scrubbing motions to promote the coating removal. A smaller capillary outside radius is preferred, which can maximize the capillary area contacting the stitch bond. The capillary tip finish is a matte, compared to a polished surface for bonding bare wire. A smaller capillary hole is also preferred, which does not scrape the coating during looping [8]. The coating thickness must be thin enough so that insulated wires do not require increased capillary hole diameters [122].

The HAZ lengths of bare and insulated wires depend on the base wire type. Some types of bare and insulated wires have no significant difference in HAZ length. Compared with its corresponding bare wire, some type of insulated wire has the HAZ length 4–12% longer, and the insulation slows down the FAB cooling after EFO or increases the plasma temperature during EFO, resulting in slightly increased recrystallized-grains [127].

A method is invented to bond insulated wire by moving the capillary tip with the wire over the stitch bond pad such that the wire is rubbed between the pad and capillary tip, tearing the insulation layer so that a portion of the metal core contacts the pad before the wire is bonded to the pad. The outer surface of the capillary tip is roughened to enhance the tearing of the wire insulation. This can lead to increased wire-peel/wire-pull strengths and near elimination of part rejection due to non-sticking on lead [119].

Another method is invented to form a bump on the second wire bond. The bump is offset by a distance of about one half of the bump diameter, which depends on the wire diameter used. For example, the bump may have a diameter of about 40–50  $\mu\text{m}$  for a  $\phi 25\text{-}\mu\text{m}$  wire used. This can enhance the bondability of insulated wire with increased wire-peel/wire-pull strengths [123,128].

A special capillary movement is provided to enable a mechanical thermal compression of the wire to the lead at the stitch bond,

**Table 4**  
Solutions and findings for reliable wire bonding with insulated wire.

Solutions and findings	References
<ul style="list-style-type: none"> <li>• Use lower EFO current and a shorter EFO gap compared to bare wire to achieve optimal FAB quality</li> <li>• Provide a coating material that easily cracks only at the stitch bond with available bonding parameters</li> </ul>	[81,22]
<ul style="list-style-type: none"> <li>• Apply a high initial bonding force with low ultrasonic energy, apply a high initial impact during touch-down, and provide slight scrub motions to promote coating removal</li> <li>• Use a smaller capillary outside radius, which maximizes the capillary area contacting the stitch bond, and a matte capillary tip</li> <li>• Use a smaller capillary hole, which does not scrape the coating during looping</li> </ul>	[127]
<ul style="list-style-type: none"> <li>• The HAZ lengths of bare and insulated wires depend on the base wire type</li> <li>• Some types of bare and insulated wires have no significant differences in HAZ length</li> <li>• Compared with bare wire, some type of insulated wire has a longer HAZ length</li> </ul>	[119]
<ul style="list-style-type: none"> <li>• Move the capillary tip with the wire over the stitch bond pad</li> <li>• Roughen the outer surface of the capillary tip</li> <li>• Form a bump on the second wire bond, offset by a distance of about one half of the bump diameter</li> <li>• Provide a special capillary movement to achieve mechanical abrasion</li> <li>• Use a special surface-treated capillary for effective tearing of the insulation layer</li> </ul>	[123,128] [16]
<ul style="list-style-type: none"> <li>• Choose a proper combination of insulation thickness, coating and melting temperatures, wire bonding and capillary parameters</li> <li>• Use a modified bonding process with a shift motion toward to the ball direction before bonding to improve the insulation layer removal</li> </ul>	[124]
<ul style="list-style-type: none"> <li>• Provide a ground adjacent to the free end of the insulated wire with a conducting capillary</li> <li>• Add a ground at the spool end of the wire at the far side of the insulated wire path from the free end</li> <li>• Have a scratching motion in combination with ultrasound to remove the insulation layer before bonding</li> </ul>	[125,126] [129]

using a special surface-treated capillary for effective tearing of the insulation layer. As a result, the peel strength is increased by 150%. Choosing a proper combination of insulation thickness, coating and melting temperatures, wire bonding and capillary parameters can result in good reliability results of insulated-wire bonding, comparable with those of bare gold-wire bonding [16].

A ground is properly provided to prevent the insulation layer on the wire, far from the free end, from being damaged. One method is providing a ground adjacent to the free end of the insulated wire with a conducting capillary instead of using a dielectric capillary. Another method is adding a ground at the spool end of the wire at the far side of the insulated wire path from the free end [125,126].

Modified bonding processes for insulated-wire bonding are developed. For example, compared to an original bonding process, a larger impact force is applied to produce a larger deformation of the stitch bond and a larger interfacial contact area. A shift motion toward to the ball direction with a shift distance of 20  $\mu\text{m}$  is then introduced to improve the insulation layer removal, with the bonding force reduced by 50% to facilitate this motion. This is followed by the bonding of the stitch with the original parameters. As a result, the average pull force of the insulated wire stitch bonds is comparable with that obtained with bare Au wire [124]. By having a scratching motion in combination with ultrasound to remove the insulation layer before bonding, the pull force of the stitch bonds obtained using insulated wire can even be larger than that obtained using bare Au wire [129].

## 5. Conclusions

Wire bonding using copper wire offers many benefits, but also poses many new challenges in wire bonding. To meet the challenges and solve the problems so as to fully benefit from its many advantages, research on wire bonding using copper wire is extensively performed worldwide, leading to many new findings and solutions to the problems. Insulated wire has market demands today and in the future, because wire sweep becomes a new challenge due to the continuous reduction in bond pad pitches and wire sizes. There were problems, which had to be solved before insulated wires could be widely used in wire bonding. Non-sticking on lead was a common problem. Several solutions to the problems have been proposed by several groups of researchers and engineers. Articles reporting numerical investigations including FEA of Cu wire bonds are still scarce, and more such reports are expected in the future. Although recently published journal articles reporting insulated-wire bonding are also scarce, more articles reporting new solutions, lower costs, better results and innovative applications are expected with more advanced devices packaged by wire bonding using insulated wires.

## References

- [1] Oberhammer J, Stemme G. *J Microelectromech Syst* 2005;14(2):419–25.
- [2] Kassamakov IV, Seppanen HO, Oinonen MJ, Haeggstrom EO, Osterberg JM, Aaltonen JP, et al. *Microelectron Eng* 2007;84(1):114–23.
- [3] Zhong ZW, Goh KS. *J Electron Manuf* 2000;10(2):89–96.
- [4] Jang C, Han S, Kim H, Kang S. *Microelectron Reliab* 2006;46(2–4):487–95.
- [5] Arulvanan P, Zhong ZW, Shi XQ. *Microelectron Reliab* 2006;46(2–4):432–9.
- [6] Lee S, Yim MJ, Master RN, Wong CP, Baldwin DF. *IEEE Trans Electron Packag Manuf* 2008;31(4):297–305.
- [7] Zhong ZW, Tee TY, Luan J-E. *Microelectronics International* 2007;24(3):18–26.
- [8] Lyn R, Crockett W. In: SEMI technology symposium – S2 advanced packaging technologies, SEMICON Singapore 2007, Singapore; 2007. p. 33–9.
- [9] Viswanath AGK, Fang W, Zhang X, Ganesh VP, Lim LA. In: Proceedings of the 7th electronics packaging technology conference, EPTC 2005; 2005. p. 215–20.
- [10] Viswanath AGK, Zhang X, Ganesh VP, Chun L. *IEEE Trans Adv Packag* 2007;30(3):448–56.
- [11] Fiori V, Beng LT, Downey S, Gallois-Garreignot S, Orain S. In: Proceedings of the electronic components and technology conference; 2007. p. 256–63.
- [12] Kim YJ, Kim JS, Chung JY, Na SH, Kim JY, Kim SB. In: Proceedings of the electronic components and technology conference; 2006. p. 1616–22.
- [13] Zhong ZW. *Microelectron Int* 2008;25(3):19–25.
- [14] ITRS (The international technology roadmap for semiconductors); 2009 <<http://www.itrs.net/reports.html>>.
- [15] Singh I, Levine L, Brunner J. In: Proceedings of the IEEE/CPMT international electronics manufacturing technology (IEMT) symposium; 2003. p. 39–43.
- [16] Ibrahim MR, Bee ATK. In: Proceedings of the 7th electronics packaging technology conference. EPTC 2005; 2005. p. 283–6.
- [17] Goh KS, Zhong ZW. *Microelectron Eng* 2007;84(2):362–7.
- [18] Shah A, Mayer M, Zhou Y, Hong SJ, Moon JT. In: 58th Electronic components and technology conference (ECTC 2008); 2008. p. 2123–30.
- [19] Lee J, Mayer M, Zhou Y, Hong SJ. *Microelectron J* 2007;38(8–9):842–7.
- [20] Levine L, Osborne M, Keller F. In: Proceedings of the IEEE/CPMT international electronics manufacturing technology (IEMT) symposium; 2004. p. 174–6.
- [21] Murali S, Srikanth N, Vath Iii CJ. *Microelectron Reliab* 2006;46(2–4):467–75.
- [22] Ruston M, Tran TA, Yong L, Youngblood A, Ravenscraft D, Harun F, Mui KW. In: Proceedings of the electronic components and technology conference; 2003. p. 1334–43.
- [23] Vitiello J, Ducote V, Farcy A, Gosset LG, Le-Fric Y, Chapelon LL, et al. *Microelectron Eng* 2006;83(11–12):2130–5.
- [24] Hoofman RJO, Verheijden GJAM, Michelon J, Iacopi F, Travaly Y, Baklanov MR, et al. *Microelectron Eng* 2005;80:337–44.
- [25] Wang Z, Du C, Han MC. In: 2005 Conference on high density microsystem design and packaging and component failure analysis. HDP'05, art. no. 4017420; 2005. p. 1–6.
- [26] Yazdani F. *IEEE Trans Adv Packag* 2006;29(2):359–63.
- [27] Hsia CC. *Microelectron Eng* 2006;83(11–12):2055–8.
- [28] Iacopi F, Brongersma SH, Vandeveld B, O'Toole M, Degryse D, Travaly Y, et al. *Microelectron Eng* 2004;75(1):54–62.
- [29] Zhao JH. *Eng Fract Mech* 2005;72(9):1361–82.
- [30] Degryse D, Vandeveld B, Beyne E. In: Proceedings of the 6th international conference on thermal, mechanical and multi-physics simulation and experiments in micro-electronics and micro-systems; 2005. p. 41–8.
- [31] van Driel WD. *Microelectron Reliab* 2007;47(12):1969–74.
- [32] Tagami M, Ohtake H, Abe M, Ito F, Takeuchi T, Ohto K, Usami T, Suzuki M, Suzuki T, Sashida N, Hayashi Y. In: Proceedings of the IEEE 2005 international interconnect technology conference, IITC; 2005. p. 12–4.
- [33] Inoue N, Tagami M, Itoh F, Yamamoto H, Takeuchi T, Saito S, Furutake N, Ueki M, Tada M, Suzuki T, Hayashi Y. In: Proceedings of the IEEE 2007 international interconnect technology conference – digest of technical papers; 2007. p. 181–3.
- [34] Yeh CL, Lai YS, Kao CL. *IEEE Trans Adv Packag* 2006;29(3):631–8.
- [35] Huang TC, Peng CT, Yao CH, Huang CH, Li SY, Liang MS, Wang YC, Wan WK, Lin KC, Hsia CC, Liang M-S. In: 2006 International interconnect technology conference, Burlingame, CA, 2006. p. 92–4.
- [36] Fiori V, Beng LT, Downey S, Gallois-Garreignot S, Orain S. In: International conference on thermal, mechanical and multi-physics simulation experiments in microelectronics and micro-systems, London, UK; 2007. p. 1–9.
- [37] van der Sluis O, van Silfhout RBR, Engelen RAB, van Driel WD, Zhang GQ. In: International conference on thermal, mechanical and multi-physics simulation experiments in microelectronics and micro-systems, London, UK; 2007. p. 1–6.
- [38] Van Der Sluis O, Van Silfhout RBR, Engelen RAB, Van Driel WD, Zhang GQ, Ernst LJ. In: Proceedings of the electronic components and technology conference; 2007. p. 235–41.
- [39] Kregting R, Van Silfhout RBR, Van Der Sluis O, Engelen RAB, Van Driel WD, Zhang GQ. In: 2006 7th International conference on electronics packaging technology, ICEPT '06, art. no. 4198954, Shanghai; 2007. p. 1–6.
- [40] van Gils MAJ, van der Sluis O, Zhang GQ, Janssen JHJ, Voncken RMJ. *Microelectron Reliab* 2007;47(2–3):179–86.
- [41] van Hal BAE, Peerlings RHJ, Geers MGD, van der Sluis O. *Microelectron Reliab* 2007;47(8):1251–61.
- [42] Srikanth N, Tiong LC, Vath Iii CJ. *Microelectron Eng* 2008;85(2):440–3.
- [43] Chhun S, Gosset LG, Michelon J, Girault V, Vitiello J, Hopstaken M, et al. *Microelectron Eng* 2006;83(11–12):2094–100.
- [44] Baklanov MR, Mogilnikov KP, Le QT. *Microelectron Eng* 2006;83(11–12):2287–91.
- [45] Leduc P, Farjot T, Savoye M, Demas A-C, Maitrejean S, Passemard G. *Microelectron Eng* 2006;83(11–12):2072–6.
- [46] Gottfried K, Schubert I, Schulz SE, Gessner T. *Microelectron Eng* 2006;83(11–12):2218–24.
- [47] Dang B, Bakir MS, Patel CS, Thacker HD, Meindl JD. *J Microelectromech Syst* 2006;15(3):523–30.
- [48] Han MC, Yan BY. In: 2009 International conference on electronic packaging technology and high density packaging, ICEPT-HDP 2009; 2009. p. 737–41.
- [49] Tan J, Zhong ZW, Ho HM. *Microelectron Eng* 2005;81(1):75–82.
- [50] Goh KS, Zhong ZW. *Microelectron Eng* 2006;83(10):2009–14.
- [51] Han M-C, Yan B-Y, Yao JZ, Tran TA, Lee S, Li J. In: 9th Electronics packaging technology conference; 2007. p. 613–7.
- [52] Han MC, Yan BY, Zhang HY, Yao JZ, Li J. In: 10th Electronics packaging technology conference, EPTC 2008; 2008. p. 457–62.



- [53] Qin W, Doyle R, Scharr T, Shah M, Kottke M, Chen G, et al. *Microelectron Eng* 2004;75(1):111–6.
- [54] Ratchev P, Stoukatch S, Swinnen B. *Microelectron Reliab* 2006;46(8):1315–25.
- [55] Chen H, Lee SWR, Ding Y. In: 2005 Conference on high density microsystem design and packaging and component failure analysis, HDP'05; 2006.
- [56] Tian YH, Lum I, Won SJ, Park SH, Jung JP, Mayer M, Zhou Y. In: 2005 6th International conference on electronics packaging technology; 2005.
- [57] England L, Jiang T. In: Proceedings – electronic components and technology conference; 2007. p. 1604–13.
- [58] Thomas S, Reynoso D. In: Proceedings of the electronic packaging technology conference, EPTC; 2009. p. 363–8.
- [59] Kung HK, Chen HS. In: Proceedings of the electronic packaging technology conference, EPTC; 2009. p. 21–6.
- [60] Yeoh LS. In: The electronic packaging technology conference; 2007. p. 731–6.
- [61] Hong S, Hang C, Wang C. In: 2005 6th International conference on electronics packaging technology; 2005.
- [62] Goh KS, Zhong ZW. *Microelectron Eng* 2007;84(1):173–9.
- [63] Zhong ZW. *Microelectron Int* 2008;25(2):9–14.
- [64] Qin I, Shah A, Huynh C, Meyer M, Mayer M, Zhou Y. *Microelectron Reliab* 2011;51:60–6.
- [65] Srikanth N, Premkumar J, Sivakumar M, Wong YM, Vath III CJ. In: The electronic packaging technology conference; 2007. p. 755–9.
- [66] Bhattacharyya A, Rittel D, Ravichandran G. *Scripta Mater* 2005;52(7):657–61.
- [67] Zhong ZW, Ho HM, Tan YC, Tan WC, Goh HM, Toh BH, et al. *Microelectron Eng* 2007;84(2):368–74.
- [68] Hung FY, Wang YT, Chen LH, Lui TS. *Mater Trans* 2006;47(7):1776–81.
- [69] Kaimori S, Nonaka T, Mizoguchi A. *IEEE Trans. Adv Packag* 2006;29(2):227–31.
- [70] Zhong ZW. *Microelectron Int* 2009;26(1):10–6.
- [71] Zhang S, Chen C, Lee R, Lau AKM, Tsang PPH, Mohamed L, Chan CY, Dirkwager M. In: Proceedings of the electronic components and technology conference; 2006. p. 1821–6.
- [72] Zhang S, Chen C, Lee R, Lau AKM, Tsang PPH, Mohamed L, Chan CY, Dirkwager M. In: Proceedings of the international symposium and exhibition on advanced packaging materials processes, properties and interfaces; 2007. p. 189–95.
- [73] Hang CJ, Wang CQ, Mayer M, Tian YH, Zhou Y, Wang HH. *Microelectron Reliab* 2008;48(3):416–24.
- [74] Drozdov M, Gur G, Atzmon Z, Kaplan WD. *J Mater Sci* 2008;43(18):6029–37.
- [75] Tian Y, Wang C, Lum I, Mayer M, Jung JP, Zhou Y. *J Mater Process Technol* 2008;208(1–3):179–86.
- [76] Kaimori S, Nonaka T, Mizoguchi A. *SEI Techn Rev* 2006;63:14–8.
- [77] Hang CJ, Song WH, Lum I, Mayer M, Zhou Y, Wang CQ, et al. *Microelectron Eng* 2009;86(10):2094–103.
- [78] Sun LN, Liu YT, Liu YJ. *Trans Nonferr Metal Soc China* 2009;19.
- [79] Pequegnat A, Hang CJ, Mayer M, Zhou Y, Moon JT, Persic J. *J Mater Sci – Mater Electron* 2009;20(11):1144–9.
- [80] Fan X, Qian K, Wang T, Cong Y, Zhao M, Zhang B, Wang J. In: 2009 International conference on electronic packaging technology and high density packaging, ICEPT-HDP 2009; 2009. p. 790–4.
- [81] Breach CD, Wulff FW. *Microelectron Reliab* 2010;50(1):1–20.
- [82] Xu H, Liu C, Silberschmidt VV, Wang H. In: Proceedings – electronic components and technology conference; 2008. p. 1424–30.
- [83] Shah A, Mayer M, Zhou YN, Hong SJ, Moon JT. *IEEE Trans Electron Packag Manuf* 2009;32(3):176–84.
- [84] Qin I, Shah A, Huynh C, Meyer M, Mayer M, Zhou Y. In: Proceedings of the electronic packaging technology conference, EPTC; 2009. p. 573–8.
- [85] Shah A, Mayer M, Zhou Y, Persic J, Moon JT. In: Proceedings of the electronic packaging technology conference, EPTC; 2009. p. 10–5.
- [86] Hung FY, Lui TS, Chen LH, Lin YC. *IEEE Trans Adv Packag* 2010;33(1):58–63.
- [87] Chang WY, Hsu HC, Fu SL, Yeh CL, Lai YS. In: 10th Electronics packaging technology conference, EPTC 2008; 2008. p. 419–23.
- [88] Chang WY, Hsu HC, Fu SL, Lai YS, Yeh CL. In: 2008 3rd International microsystems, packaging, assembly and circuits technology conference, IMPACT 2008; 2008. p. 287–90.
- [89] Murali S, Srikanth N, Wong YM, Vath Iii CJ. *J Mater Sci* 2007;42(2):615–23.
- [90] Lee J, Mayer M, Zhou Y, Hong SJ, Moon JT. In: Proceedings of the electronic components and technology conference; 2008. p. 2024–9.
- [91] Premkumar J, Kumar BS, Madhu M, Sivakumar M, Song KY, Wong YM. In: 10th Electronics packaging technology conference, EPTC 2008; 2008. p. 971–5.
- [92] Hung FY, Lui TS, Chen LH, Lin YC. *Mater Trans* 2009;50(2):293–8.
- [93] Jacob P, Rutsch M. In: Conference proceedings from the international symposium for testing and failure analysis; 2008. p. 49–52.
- [94] Lum I, Hang CJ, Mayer M, Zhou Y. *J Elec Mater* 2009;38(5):647–54.
- [95] Lee J, Mayer M, Zhou Y, Hong SJ, Moon JT. *IEEE Trans Electron Packag Manuf* 2009;32(3):157–63.
- [96] Ding Y, Hu L, Hu Y, Cao WH. *Tezhong Zhuzao Ji Youse Hejin/Special Cast Nonferr Alloys* 2009;29(6):0582–4 [+VIII].
- [97] Ding Y, Cao J, Hu Y, Kou S, Xu G. *Jixie Gongcheng Xuebao/J Mech Eng* 2009;45(4):83–8.
- [98] Sibalija TV, Majstorovic VD. *Int J Adv Manuf Technol* 2009;42(3–4):363–71.
- [99] Zhong ZW, Tee TY. *Proc IEEE* 2009;97(1):175–83.
- [100] Sun J, Zhong ZW. *Sens Actuators A – Phys* 2002;100(2–3):257–63.
- [101] MacKerle J. *Modell Simul Mater Sci Eng* 2005;13(6):935–79.
- [102] Tee TY, Zhong Z. *Microelectron Reliab* 2004;44(12):1957–65.
- [103] Zhong Z, Yip PK. *Solder Surf Mount Technol* 2003;15(1):21–5.
- [104] Tee TY, Ng HS, Yap D, Zhong ZW. *Microelectron Reliab* 2003;43(8):1329–38.
- [105] He J, Guo Y, Lin Z. *Microelectron Reliab* 2008;48(4):594–601.
- [106] Saiki H, Marumo Y, Nishitake H, Uemura T, Yotsumoto T. *J Mater Process Technol* 2006;177(1–3):709–12.
- [107] Ishiko M, Usui M, Ohuchi T, Shirai M. *Microelectron J* 2006;37(3):262–8.
- [108] Chen KM, Wu BC, Tang KH, Cheng FY, Kao NH, Lai JY. *Microelectron Reliab* 2006;46(2–4):335–42.
- [109] Chen KM, Tang KH, Liu JS. *Microelectron Reliab* 2008;48(3):408–15.
- [110] Gao J, Kelly R, Yang Z, Chen X. In: 2008 International conference on electronic packaging technology & high density packaging, vols. 1 and 2; 2008. p. 788–93.
- [111] He J, Guo YJ, Lin ZQ. In: Icept: 2007 8th international conference on electronics packaging technology, proceedings vol. 60; 2007. p. 1–12.
- [112] He J, Zhu P. In: Proceedings of the electronic packaging technology conference, EPTC; 2007.
- [113] Zhai Y, Zhao W, Jun C, Hw T. In: 2009 International conference on electronic packaging technology and high density packaging, ICEPT-HDP 2009; 2009. p. 742–8.
- [114] Huang W. In: 2009 International conference on electronic packaging technology and high density packaging, ICEPT-HDP 2009; 2009. p. 344–52.
- [115] Tee TY, Ng HS, Zhong ZW. *Microelectron Reliab* 2006;46(12):2131–8.
- [116] Degryse D, Vandeveld B, Beyne E. *IEEE Trans Compon Packag Technol* 2004;27(4):643–50.
- [117] Chen J, Degryse D, Ratchev P, De Wolf I. *IEEE Trans Compon Packag Technol* 2004;27(3):539–45.
- [118] Downey SH, Harper PR. United States Patent 7138,328, US; 2006.
- [119] Harun F, Chan CM, Tan LC, Beng LT, Tiu KB, Yong SS. United States Patent 7261230, US; 2007.
- [120] Mesaki M, Tatamatsu Y. United States Patent 6734,361, US; 2004.
- [121] ITRS (The international technology roadmap for semiconductors; 2006) <<http://www.itrs.net/Links/2006ITRS/Home2006.htm>>.
- [122] Lyn RJ, Persic JI, Song YK. In: 39th International symposium on microelectronics (IMAPS), San Diego, CA, USA; 2006.
- [123] Harun F, Tiu KB. United States Patent 6854,637, US; 2005.
- [124] Lee J, Mayer M, Zhou Y, Persic J. In: The electronic packaging technology conference; 2007. p. 725–30.
- [125] Lyn RJ, Persic JI, Song Y-K. United States Patent 6896170, US; 2005.
- [126] Lyn RJ, Persic JI, Song Y-K. European Patent EP1448335 European; 2004.
- [127] Song WH, Hang C, Pequegnat A, Mayer M, Zhou NY, Song YK, Persic J. *J Elec Mater* 2009;38(6):834–42.
- [128] Harun F, Tiu KB. European Patent EP1617967, European; 2006.
- [129] Lee J, Mayer M, Zhou N, Persic J. *Mater Trans* 2008;49(10):2347–53.