

# Finite element analysis of a three-dimensional package

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## Keywords

Flip chip, Fatigue, Solder joints, Finite element analysis

## Abstract

A three-dimensional (3D) package consisting of a stack of three silicon chips was conceptually designed. A finite element simulation of this 3D package was conducted in order to compare the fatigue lives of the solder joints with those in a typical single flip chip package when subjected to a cyclic thermal loading. It was found that the proposed design of the 3D package was feasible in terms of its mechanical deformation response to the thermal cycle.

## Introduction

Most future electronics applications will require increased reliability and performance as well as lower cost. In order to meet this general demand, many new three-dimensional (3D) packaging technologies are now emerging where multiple ICs are stacked within a single package. The advantages of 3D packaging are an increase in the silicon packing efficiency and, through a reduction in the parasitic impedances, an increase in the bandwidth, reduction of signal time delay and reduction of system power consumption, allowing an increase in the system speed and clock rate (Ginsberg and Schnorr, 1994). However, they are limitations to the use of 3D packaging in terms of thermal management, design complexity and design software.

A conceptual design of a 3D package was attempted in this study. In order to investigate the feasibility of this design in terms of the reliability of the interconnecting solder joints between the stacked chips and the substrate, a computer modelling approach was used to simulate a thermal cycling load. A comparison of the fatigue life with that of a conventional flip chip package was performed in order to investigate the effect of the multi-layer chips on the fatigue life.

## Conceptual design

The chip thickness was chosen to be 300  $\mu\text{m}$ , although the technology is available to allow a wafer to be thinned to 100  $\mu\text{m}$ . During the micro-lithography of the chip circuit, special routing of the circuit is required to route the connections from the circuit to the edges of the chip instead of standard bond pads.

One of the silicon chips has a special backside interconnection layer. This layer contains the pathways, pads and bumps, which would be used to interconnect the IC stack to the package substrate. The configuration of the pads and bumps can be either a peripheral array or an area array (only a peripheral array is shown in Figure 1).

The next stage is to stack the chips using an adhesive, after which the vertical interconnects on the edges of the stack are produced using conventional micro-lithography techniques. These interconnects can be either a single layer or multi-layer. If the vertical interconnects are multi-layered, then the insulating material could be silicon dioxide, which can be deposited using chemical vapour deposition etc. with the aluminium interconnects being deposited alternately with the dielectric layers using the normal built-up process.

The final stage is to attach the chips to a substrate using a flip-chip mounting method. The solder bumps are reflowed and underfilling is conducted to complete the packaging process (Figure 2).

## Finite element analysis modelling

The 3D package and a conventional 2D package were modelled using the ANSYS<sup>TM</sup> finite element analysis (FEA) software. The interconnection method considered was flip chip attachment onto an FR-4 substrate using eutectic tin-lead solder. Investigation of the 3D package's reliability in terms of stresses of the solder joints induced by the coefficient of thermal expansion (CTE) mismatch between the chips and the FR-4 substrate was carried out.

A direct consequence of the CTE mismatch is the development of stresses and strains in the system, including the solder joints sandwiched between the chip and the substrate during temperature changes. If the temperature fluctuates, the strain and stress will also fluctuate, eventually leading to fatigue failure of the solder joints (Frear, 1991).

Since fatigue failure of solder joints is one of the major failure mechanisms for a flip chip assembly, it is desirable to predict the reliability of the design before the production stage. This is a difficult task due to the lack of experimental data, the limited understanding of the physics of solder fatigue and fatigue in general, and the extremely time-consuming reliability testing process (Lu *et al.*, 1999). The difficulty in predicting the reliability of the solder joints can be significantly reduced with the help of computer modelling which, combined with empirical methods, has made it possible to analyse these thermal stresses and strains.

## Model geometry and material properties

Three-dimensional diagonal slices (Darveaux, 2000; Lam, 2000; Lau and Pao, 1997) of the packages were used for the simulation (Figure 3). Table I lists the geometric parameters and Table II lists the material properties used in the simulation. The property values are referenced at 25°C.

Both models had full area array interconnects with a pitch of 225  $\mu\text{m}$  and 144 I/Os in a quadrant. The pads on the chip and the substrate were represented only by nickel and copper, respectively. The solder was assumed to wet the pads on both sides. The 3D package model had three stacked silicon chips, each with a thickness of 300  $\mu\text{m}$ . The 2D package model had only one chip having a thickness of 500  $\mu\text{m}$ .

Since diagonal slices of the two package types were simulated, the following boundary conditions were applied to the models:  $U_x = 0$  for all of the nodes in the  $x$ -symmetrical plane,  $U_y = 0$  for the package centre, and  $U_z = 0$  for all of the nodes in the  $z$ -symmetrical plane.

## Anand viscoplastic model

When used in electronic devices eutectic Sn-Pb solder usually works at high homologous temperatures because of

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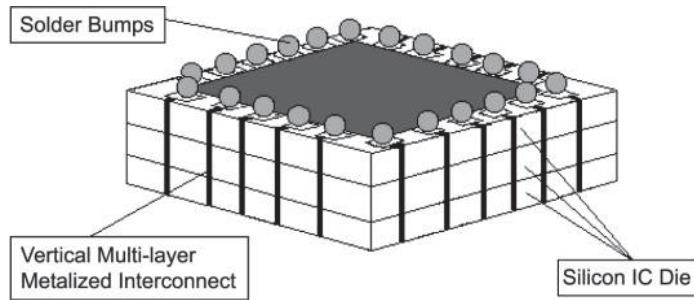
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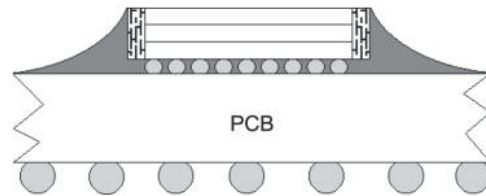


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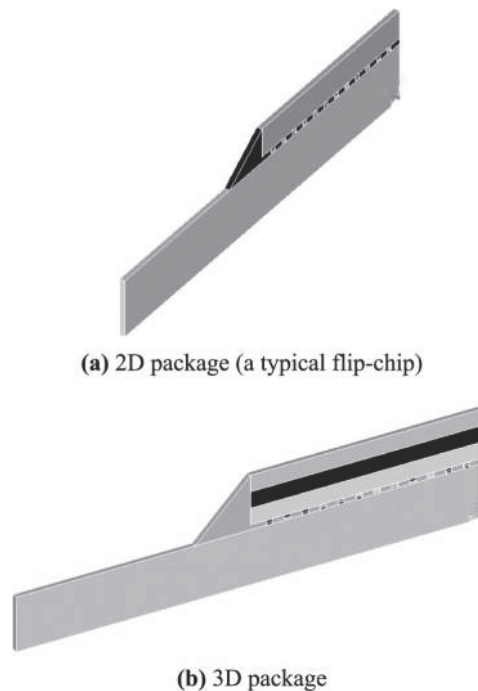
**Figure 1**  
 Schematic drawing of stacked dies



**Figure 2**  
 Schematic drawing of the 3D package



**Figure 3**  
 Diagonal slice models of the packages.



**Table I**  
 Geometric properties of the package models

	3D package	2D package
Die dimensions (mm <sup>3</sup> )	6.0 × 6.0 × (0.3 × 3)	6.0 × 6.0 × 0.5
Solder bump diameter (μm)	120	120
Standoff height (μm)	95	95
Substrate thickness (μm)	1,000	1,000
Pad diameter (μm)	90	90
Copper pad thickness (μm)	40	40
Nickel pad thickness (μm)	5	5

**Table II**  
 Material properties used in the package models

	CTE 10 <sup>-6</sup> /°C	E (GPa)	ν
FR-4	α <sub>x</sub> : 18	E <sub>x</sub> : 22	ν <sub>xy</sub> : 0.28
	α <sub>y</sub> : 70	E <sub>y</sub> : 10	ν <sub>yz</sub> : 0.11
	α <sub>z</sub> : 18	E <sub>z</sub> : 22	ν <sub>xz</sub> : 0.28
Copper	17	121	0.35
63Sn-37Pb solder	21	10	0.4
Nickel	13.4	200	0.31
Silicon	2.8	131	0.3
Underfill	30	6	0.35

the solder's low melting point. High homologous temperatures experienced by the solder and the thermally activated strains imposed on it due to the CTE mismatch among the materials in a package cause a complex deformation behaviour. This deformation behaviour is associated with the irreversible, temperature and rate (or time) dependent inelastic characteristics. This deformation behaviour is known to be viscoplastic, with general relations such as creep and stress relaxation phenomena in materials working in the high homologous temperature regime. A unified framework was used in this study for viscoplastic behaviour of solder materials, in which plasticity and creep were unified and described by the same set of flow and evolutionary equations proposed by Anand (1985) and Brown *et al.* (1989).

ANSYS has viscoplastic elements available as standard. The use of these elements is convenient because the source code does not need any modification. Anand's model is broken down into a flow equation and three evolution equations (Darveaux, 2000). In their article, Darveaux *et al.* (1995) made an approximate fit to solder deformation data using only the flow equation. In another paper, Darveaux (1997) used the flow equation and the evolution equations.

In this study, the following functional form for the flow equation of the Anand model was selected to accommodate the strain rate dependence on the stress (Lam, 2000).

$$\frac{d\epsilon}{dt} = C_{7l} [\sinh(\alpha_{2l}\sigma)]^n \exp\left(\frac{-Q_a}{kT}\right) \quad (1)$$

where,  $d\epsilon/dt$  is the equivalent creep strain rate;  $\sigma$  is the equivalent Von-Mises stress;  $\alpha_{2l}$  is a constant related to power law break down stress;  $Q_a$  is the activation energy;  $n$  is 3.3; and  $C_{7l}$  is a characteristic constant of the material. In the ANSYS FEA system used, this equation can be implemented by using element type VISCO 107 with the ANAND option (Lam, 2000). The input constants required for eutectic Sn-Pb solder are listed in Table III.

### Non-linear element analysis method

Three-dimensional non-linear element modelling was used to calculate strain energy density accumulation in the solder joints during thermal cycling. The solder material was

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**Table III**

The constants for the Anand viscoplastic formulation for eutectic tin-lead solder (Lam, 2000)

TBDATA constant	Parameter	Meaning	Unit	Value
1	$s_0$	Initial value of deformation resistance	Stress, Pa	$12.412 \times 10^6$
2	$Q/R$	$Q$ = Activation energy $R$ = Universal gas constant	1/K	9,400
3	$A$	Pre-exponential factor	1/s	$4 \times 10^6$
4	$\xi$	Multiplier of stress	Dimensionless	1.5
5	$m$	Strain rate sensitivity of stress	Dimensionless	0.303
6	$h_0$	Hardening/softening constant	Stress, Pa	$13.792 \times 10^8$
7	$s$ (hat)	Coefficient for deformation resistance saturation value	Stress, Pa	$13.792 \times 10^6$
8	$N$	Strain rate sensitivity of saturation (deformation resistance) value	Dimensionless	0.07
9	$a$	Strain rate sensitivity of hardening or softening	Dimensionless	1.3

modelled as a viscoplastic solid, and the other materials were modelled as linearly elastic solids in order to simplify the simulation.

The objective of the simulation was to calculate the plastic work density per unit volume or viscoplastic strain energy density, which is referred to as *plwk* in ANSYS. Three complete thermal cycles (1 h/cycle), as shown in Figure 4, were simulated in order to establish a stable stress-strain hysteresis loop. The initial stress-free temperature was 25°C, the dwell times at  $-25^\circ\text{C}$  and  $+125^\circ\text{C}$  were 15 min, and the ramp rates were  $\pm 10^\circ\text{C}/\text{min}$ . The difference in the plastic work density between the ends of the second and third cycles was taken to be the plastic work expended per cycle.

The calculated strain energy density has been found to increase as the element size in the solder joint is decreased (Darveaux *et al.*, 1995). Hence, a volume averaging technique (Darveaux, 2000) was used to reduce this sensitivity to the mesh density. The strain energy value of each element can be normalized by the volume of the element.

$$\Delta W_{\text{ave}} = \frac{\sum(\Delta WV)}{\sum V} \quad (2)$$

where  $\Delta W_{\text{ave}}$  is the average viscoplastic strain energy density accumulated per cycle for the solder elements,  $\Delta W$  is the viscoplastic strain energy density accumulated per cycle of each element, and  $V$  is the volume of each element.

Once the value of  $\Delta W_{\text{ave}}$  was obtained, the following equations (Darveaux, 2000; Lam, 2000) were used to predict the fatigue life of the solder joints in the models.

Crack initiation (no. of cycles):

$$N_0 = K_1 \Delta W_{\text{ave}}^{K_2} \quad (3)$$

Crack growth (m/cycle):

$$\frac{da}{dN} = K_3 \Delta W_{\text{ave}}^{K_4} \quad (4)$$

Cycles to fracture (no. of cycles):

$$N_f = N_0 + \frac{a}{da/dN} \quad (5)$$

where  $K_1 = 6.37 \times 10^8$  cycles/(Pa) $^{K_2}$ ,  $K_2 = -1.44$ ,  $K_3 = 1.88 \times 10^{-13}$  m/cycles/(Pa) $^{K_4}$ ,  $K_4 = 1.15$ , and  $a$  = diameter of solder bump.

Because finite element prediction is element-size sensitive, the constants above only apply to elements with a thickness greater than  $15 \mu\text{m}$ . Additional constants for element sizes that differ from what was used in this study can be found in Darveaux's (2000) article.

## Results and discussion

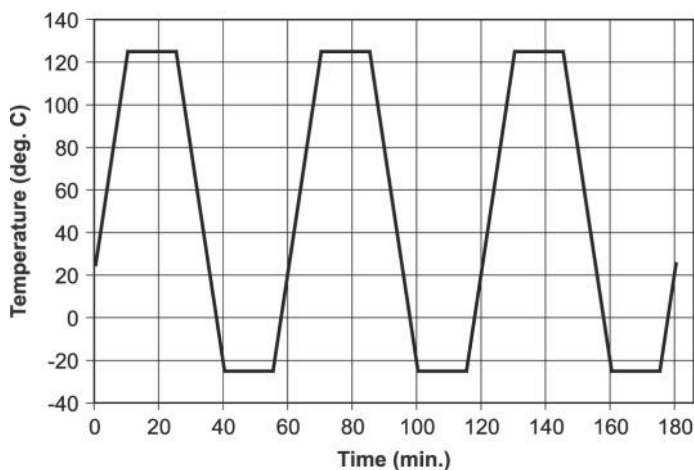
Figure 5 demonstrates the effect of CTE mismatch between the silicon chip and the FR-4 substrate causing the package's deformation when subjected to uniform thermal loading of temperature  $125^\circ\text{C}$  and  $-25^\circ\text{C}$ . The broken lines represent the undeformed shape of the package. When the model is subjected to a thermal loading of  $125^\circ\text{C}$ , the package bends upwards, as shown in Figure 5(a). This is because the higher CTE of the FR-4 substrate causes the substrate to expand more than the silicon chip, which has a lower CTE. Conversely, as shown in Figure 5(b), when the package is cooled to  $-25^\circ\text{C}$ , the package bends downwards as the higher CTE of FR-4 causes it to contract more than the silicon chip.

The outermost bump had the highest plastic work density compared to the rest of the solder bumps. As such, the life prediction calculation of the simulated models was based on the plastic work density of the outermost solder bump as it was the most likely site for first failure. Figure 6 shows the plastic work density (averaged) contour plot of the outermost solder joints at the end of the three cycles for the 2D package and the 3D package models. Table IV shows the results of the fatigue life calculation.

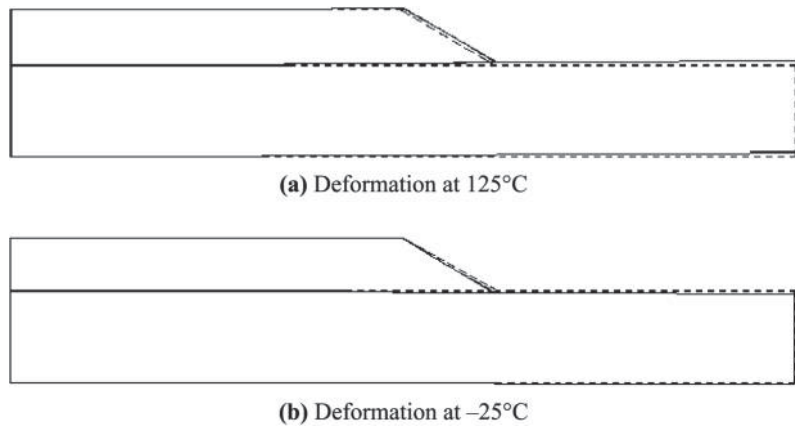
The results show that the values of the plastic strain, Von Mises stress and plastic work density for the 2D package are lower than those for the 3D package. The calculated  $\Delta W_{\text{ave}}$  for the 2D package is also lower than that of the 3D package, causing the fatigue life of the 2D package to be longer than that of the 3D package by 45 per cent. This can be attributed to the thicker stacked silicon chip layers that increase the effect of the CTE mismatch between the silicon chips and the FR-4 substrate.

**Figure 4**

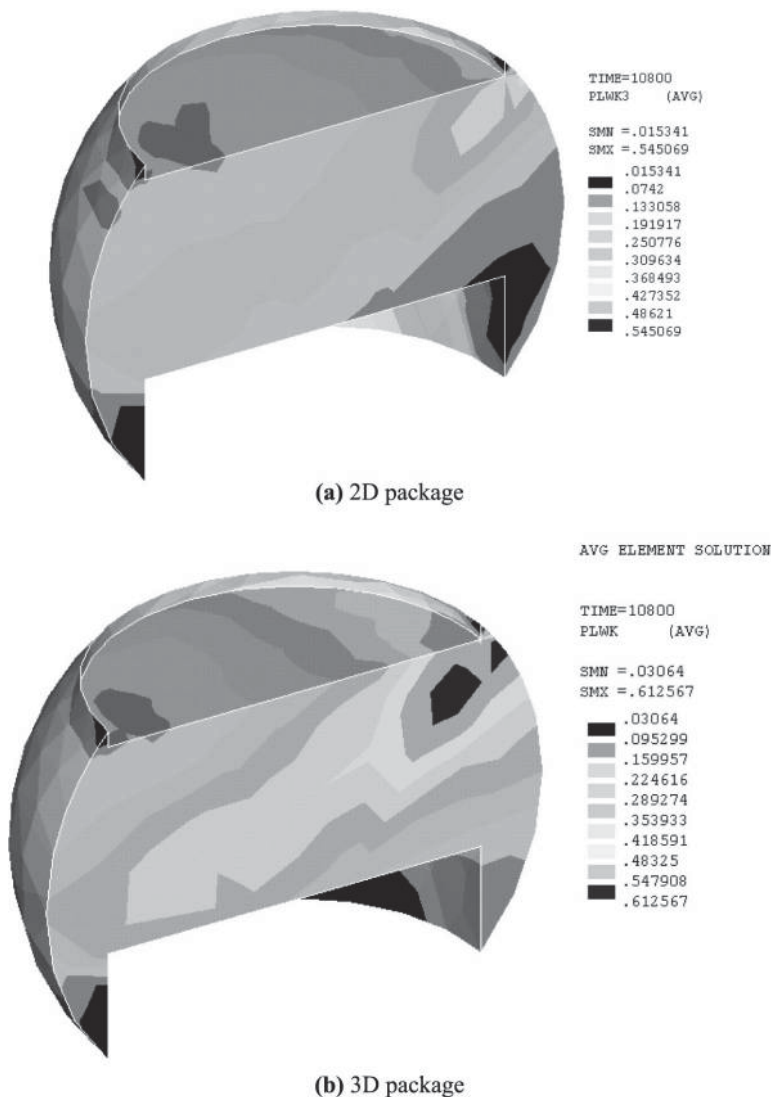
The time/temperature profile used



**Figure 5**  
 Package deformation due to thermal loading. The broken lines represent the undeformed shape of the package



**Figure 6**  
 Averaged plastic work density ( $N/mm^2$ ) contour plot of the outermost solder joints of the 2D and 3D packages (Time=180 min)



**Table IV**  
 Fatigue life prediction results

	2D package	3D package
$\Delta W_{ave}$ (Pa)	61,220	98,689
$N_0$ (cycle)	1,155	581
$da/dN$ (m/cycle)	$0.06007 \times 10^{-6}$	$0.1040 \times 10^{-6}$
$a$ (m)	$120 \times 10^{-6}$	$120 \times 10^{-6}$
$a/(da/dN)$ (cycle)	1,998	1,154
$N_f$ (cycle)	3,153	1,735
Percentage difference, $N_f$	100 per cent	55 per cent

The distribution of the plastic work density for both models (Figure 6) shows that viscoplastic strains are highly localized at the upper corner of the solder joint near the interface with the nickel pad on the silicon chip. Crack failure may initiate in this critical region during thermal cycling. Cheng *et al.* (2000) reported a metallographic cross-section with a thermal-fatigue-induced crack in a solder joint. The crack occurred near the fillet corner and propagated in the solder joint close to the upper interface between the solder and the chip passivation. The modelling results presented here are in good agreement with their experimental results.

The fatigue life of the 3D package,  $N_f$  is predicted to be 1,735 cycles, which is 55 per cent of that of the 2D package. The utilization of an inexpensive FR-4 substrate material reduces the production cost and also improves the compatibility with current manufacturing techniques. However, if a ceramic substrate were to be used, it is expected that the effect of the reduced CTE mismatch would be an improved life.

The fatigue life may be improved when thinner chips are used. Currently silicon wafers can be produced as thin as  $100 \mu m$ . This can also allow more chips to be stacked before the thermal-mechanical deformation due to CTE mismatch reduces the fatigue life to a degree where it is no longer practical. Another way to increase the fatigue life is to increase the standoff height between the bottom layer chip and the substrate, by using bigger solder bumps. However, the increased solder bump size also means that the solder pitch will not be as fine, thus leading to a reduction in the possible maximum I/O count.

## Summary

Comparison of the predicted fatigue lives of the 3D package and a 2D package using the finite element method shows that the 3D package life is 45 per cent lower ( $N_{f2D} = 3,153$

cycles vs  $N_{f3D} = 1,735$  cycles). This shows that although the silicon chips are stacked, making the overall height of the 3D package higher, the fatigue life is still within an acceptable limit, i.e. greater than 1,000 cycles ( $N_f > 1,000$ ). The design of the 3D package is therefore considered to be feasible in terms of thermo-mechanical deformation.

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