VLSI TECHNOLOGY AND CIRCUITS COMMITTEE
JUNE 1999 ADCOM REPORT

TO: IEEE EDS ADCOM

FROM: H.-S. PHILIP WONG

SUBJECT: ACTIVITIES OF THE VLSI TECHNOLOGY AND CIRCUITS COMMITTEE, JAN 99 TO DEC 99

DATE: 11/30/99

CC: JAMES T. CLEMENS, ATSUSHI HORI, JACK LAU, JOHN K. LOWELL, ERIC M. MAIR, KEVIN J. O'CONNOR, DENNIS L. POLLA, WERNER WEBER

OVERVIEW

The objective of the VLSI Circuits and Technology Committee is to identify new/hot areas of interest to the Electron Device and Solid-State Circuits communities. Based on the nature of the areas, we will recommend any or all of the following.

1. Initiate topical workshops of current interest (attached to existing conferences or start new ones)

2. Special Issues for major publications (e.g. T-ED)

3. Panel session topics for major conferences

4. Special Sessions for major conferences

As a result of our first face-to-face meeting on Dec. 5, 1998, there is a consensus that this committee would be most effective on items 1 and 2 above. Therefore, this year, we will concentrate on items 1 & 2; but if we have good ideas for 3 & 4, we will help establish the connection to the conferences.

This committee continues to operate entirely by email. Two workshops wer successfully organized by our committee members in February, 1999, and in October, 1999. One Trans. Electron Devices special issue is accepted as a result of our committee's proposal. Another T-ED special issue proposal is in the works. A workshop on memory technologies is being conceived.

MEMBERSHIP

In the Dec. 5, 1998, meeting, everyone expressed a desire to have members come from Europe and Japan in addition to the North American and Asian members in the first year. We are thankful that Atsushi Hori (Matsushita) and Werner Weber (Siemens) have agreed to join us.

We expect to limit the membership of the committee to three years so that new ideas can be incorporated. John Lowell expects to resign from the committee next year due to other engagement.

All other present committee members are invited to serve another year. In 2001, both the present Chair and all the members (except the two new members added in 1999) will leave this committee. In 2000, we are looking to add enough members for the committee to function in 2001.

WORKSHOP ORGANIZATION

1. IEEE SOLID STATE CIRCUITS TECHNOLOGY WORKSHOP ON RF PASSIVE COMPONENTS
   (Jack Lau)

This workshop was quite a success, with over 75 registered attendees (filled to capacity). The talks ranged from measurement, CAD, integration, to micromechanical structures. There were a number of good interactions during the workshop. Although there were not a lot of advance advertisement, the attendance was good, an indication of the timeliness of the topic and the quality of the speakers. The fact that it is held in conjunction with a large conference clearly helped in many aspects. The agenda of the workshop is listed below:

- Discrete Passive Components for RF-IC Applications – An Introduction (Lukas Leyten, Philips)
- Modeling of RF Inductors (Simon Wong, Stanford)
- Integration of RF Inductors (Joachim Burghartz, Delft University)
- RF and High-Speed Circuit Design using On-Chip Inductors and Transformers (John Long, Toronto)
- Introduction to High Frequency Electromagnetic Analysis (Jim Rautio, Sonnet)
- Integrated Varactors for RFIC's (Jack Lau, HKUST)
- Micromechanical Resonators for Miniaturized Low-Power Communications (Clark Nguyen, U. Michigan)

2. 300 MM MANUFACTURING TUTORIAL WORKSHOP
   (John Lowell)

In conjunction with the IEEE International Symposium on Semiconductor Manufacturing (Oct. 11-13, 1999, Santa Clara), a one day (Oct. 10, 1999, noon – 6 pm) tutorial workshop on 300 mm manufacturing was held at the Santa Clara Marriott. This workshop is sponsored jointly by the Electron Devices (EDS) Technical Committees on VLSI Circuits & Technology and Semiconductor Manufacturing. About 200 attended a standing-room only workshop. It was a success by all accounts. The ISSM is considering another such workshop in 2 years when the ISSM returns to the U.S.

The scope of this workshop is to present and discuss many of the major issues facing the EDS community as it transitions into 300mm wafer manufacturing and the ULSI device realm within the next few years. As we move into the 300 mm realm, we will face several new trends that will impact

our entire industry such as the merging of R&D facilities with manufacturing, the increased role of equipment vendors in process integration as well as new equipment design, major increases in costs of materials and equipment, the need for new methods of device metrology, the emergence of new device architectures, and new defect detection, defect reduction, and yield enhancement techniques.

The format of the workshop includes two keynotes talks by I300I and SLET representatives, invited tutorial lectures on critical topics and panel discussion. The program can be found in the URL: http://www.issm.com/workshop%20agenda.html.

The workshop invites participants for this workshop from equipment suppliers, semiconductor manufacturers including the R&D and manufacturing sectors, silicon suppliers, metrology and test equipment vendors, and the university research community who are involved with the area of 300mm manufacturing and the advanced device concepts they will embrace.

Workshop Chairs:

- Rajendra Singh, Holcombe Department of Electrical and Computer Engineering,Clemson University (E-mail: raj.singh@ces.clemson.edu)
- John Lowell, Oracle Corp. (Email: jklowell@us.oracle.com)
- Kamal Rajkanan, KLA-Tencor Corporation (Email: kamal.rajkanan@kla-tencor.com)

The full report on the workshop will be presented by Arlene Santos at the December 1999 AdCom meeting.

3. WORKSHOP ON EMERGING MEMORY AND STORAGE TECHNOLOGIES
(Werner Weber, Philip Wong)

This workshop is in the proposal stage and we are still looking for the suitable organizers. The concept of the workshop is to bring together researchers and developers to exchange information on new and emerging memory technologies. Technologies such as FeRAM, MagRAM, quantum dot memory, single-electron memory, multi-level FLASH and DRAM, etc. are examples.

Many "new" storage ideas start with a materials and device innovation. But in order to make that a real technology, the architecture issues need to be addressed also. For example, the MagRAM and MRAM has a different architecture, and quantum dot memories has interesting tradeoff's in read/write speed and retention/endurance. The purpose of the workshop is to bring together people with experience in these emerging storage principles and discuss device/architecture issues. There are several possible venues, among them the most painless would be to attach the workshop to existing large conferences such as the Symp. VLSI Technology (June, 2000), and the ISSCC (Feb, 2000).

Stan Schuster of the Solid State Circuits Council has already agreed to allow this workshop to be attached to the ISSCC in 2000. At this point, we are in need of an organizer for the conference. Any suggestions of organizers will be welcome.

IEEE TRANSACTION OF ELECTRON DEVICES SPECIAL ISSUES

Two special-issue topics were proposed to the Editor-in-chief of the IEEE Transaction of Electron Devices. The proposal on TCAD and Computational Electronics has already been accepted and the announcement of the special issue has appeared in the June issue of the IEEE Transaction of Electron Devices (deadline for paper submission: November, 1999, publication date: October, 2000). The proposal on Interconnect Systems was forwarded to the Editor-in-chief and is now on-hold since T-ED special issues has already been booked through 2001.

1. SPECIAL ISSUE ON COMPUTATIONAL ELECTRONICS: NEW CHALLENGES AND DIRECTIONS
   (Philip Wong)

This issue will provide a forum for new approaches in computational electronics and their application to critical challenges in semiconductor technology. Areas of interest include but are not restricted to: technology computer aided design (TCAD) and issues for next-decade TCAD, the device physics of electronic and optoelectronic devices, the role of quantum scale effects in devices, the treatment of reliability, contacts, and tunneling currents by simulations, and exploration of novel devices and device architectures by simulation. Papers on software approaches and numerical methods that are relevant to these issues and accessible to non-specialists are also solicited. Guest Editors: Mark Lundstrom (Purdue University), Bob Dutton (Stanford University), Karl Hess (University of Illinois), David Ferry (University of Arizona).

2. SPECIAL ON INTERCONNECT SYSTEMS
   (Atsushi Hori, Eric Mair)

Since interconnect delay becomes a main factor of LSI performance due to the scaling of the device dimensions, it is important to consider whole LSI performance for scheming the interconnect design strategy. On the other hand, new materials such as low resistance (Cu) and low-k dielectrics have been developed to overcome the limit of the LSI scaling merit. The interconnect systems include materials (low resistance, low-k dielectrics), hierarchal structure, and circuit performance such as gate delay and crosstalk. In this special issue, following items will be discussed.

- Low resistance and low-k materials and their impact on LSI performance
- Design strategy of interconnect such as hierarchal structure and novel structure.
- Novel simulation method to predict performance such as delay time and crosstalk.
- Fabrication and technology integration

This committee supplied a list of potential guest editors and their biographies to the T-ED editor-in-chief for the editor's consideration.

ARTICLE IN THE ELECTRON DEVICES SOCIETY NEWSLETTER

A short article describing the objectives and activities of this committee was written by Philip Wong and published in the October issue of the Electron Devices Society Newsletter.

REVIEW FOR THE IEEE PRESS

Kwok Ng, EDS Liaison to the IEEE Press, requested our committee to review two book proposals to the IEEE Press. Both proposals are within our committee's technical area. We polled the members and provide reviews and suggested possible reviewers to the IEEE Press. The two book proposals were:

- "Flash memory technologies", by Joe E. Brewer and Manzur Gill.
- "CMOS Technology Definition and Benchmarking" by Alfred Hesener