Course Outline

Module 1 ● ***TCAD: Process Simulation***

Week 1
- ❑ Introduction to Physical Simulation and TCAD
- ❑ Semiconductor Fabrication Processes

Week 2
- ❑ CMOS Process Flow and Device Design
- ❑ TSUPREM-4: Process Simulation

Week 3
- ❑ TMA WorkBench: Virtual IC Factory

Week 4–7
- ❑ Design 1: Virtual Wafer Fabrication (VWF)

Module 2 ● ***TCAD: Device Simulation***

Week 8
- ❑ Device Simulation and Characterization
- ❑ MEDICI: Device Simulation
- ❑ AURORA: Parameter Extraction
- ❑ SPICE: Circuit Simulation

Week 9–11
- ❑ Design 2: Virtual Device Characterization (VDC)

Week 12–13
- ❑ Design 3: Virtual Process Integration (VPI)

Course Objectives

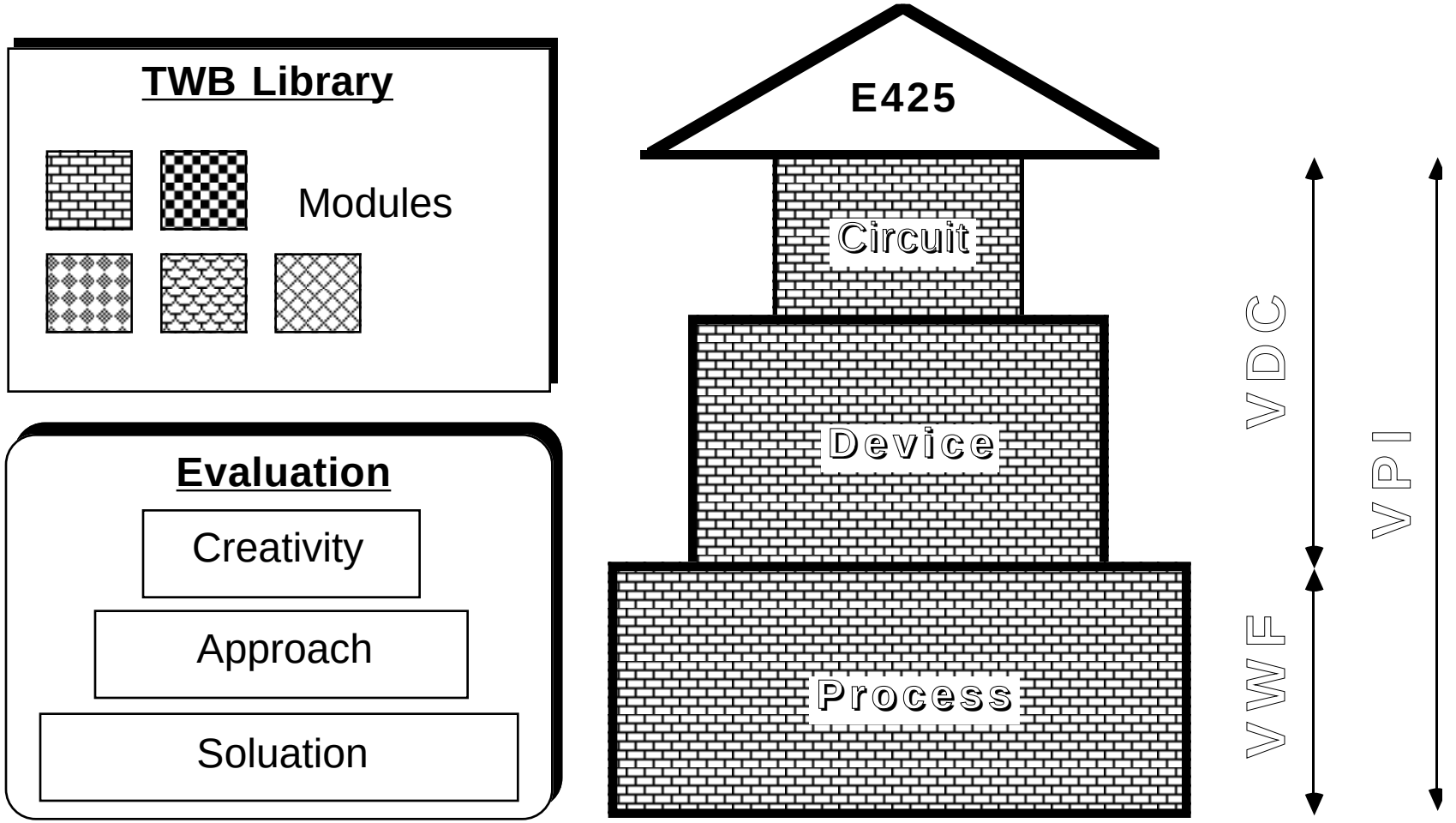
❑ ***General***

- To understand and appreciate the underlying physics and principles involved in silicon processing and device characterization
- To relate theory on semiconductor processing and device physics to practical technology development and device design considerations
- To get familiarized with the use of TCAD tools as a design aid in process and device simulation

❑ ***Specific***

- To analyze, design, and simulate a 2–μm CMOS process and transistor electrical characteristics
- To implement the design under the TMA WorkBench environment, integrating process, device, and circuit parameter extraction
- To visualize physical quantities and parameters at various stages of the design
- To study the influence of process variables on the device performance

Engineering Design V



TCAD: Emulating Wafer Fabrication and Device Characterization

- **VWF: Virtual Wafer Fabrication** — creating device structures and impurity distributions through process-dependent numerical simulation
  - Basic fabrication process steps and modules
  - Process variables and targets, and their dependencies
- **VDC: Virtual Device Characterization** — characterizing device electrical performance by solving coupled partial differential equations
  - Single-device 2D/3D numerical simulation
  - Circuit model parameter extraction and optimization
  - Circuit simulation
- **VPI: Virtual Process Integration** — integrating silicon process steps to create and optimize silicon devices
  - Structural variation: layer thickness, depletion width, etc.
  - Process variation: impurity profile, junction depth, etc.
  - Mask variation: lateral diffusion, design rule and scaling rule, etc.