VLSI TECHNOLOGY AND CIRCUITS COMMITTEE
DECEMBER, 2001 ADCOM REPORT

FROM: WERNER WEBER

SUBJECT: ACTIVITIES OF THE VLSI TECHNOLOGY AND CIRCUITS COMMITTEE, JAN 2001 TO DEC 2001

DATE: DECEMBER 8, 2001.

TO: ATSUSHI HORI, LALITA MANCHANDA, KEN-ICHI GOTO, S.C. SUN, WILLY SANSEN, PIERRE WOERLEE, TSU-JAE KING, XING ZHOU, MARK LAW, JEFF WELSER, ILESNMI ADESIDA, JIM HUTCHBY, AKIRA TORIUMI, KWYRO LEE

OVERVIEW

The objective of the VLSI Circuits and Technology Committee is to identify new/hot areas of interest to the Electron Device and Solid-State Circuits communities. Based on the nature of the areas, we will recommend any or all of the following.

1. Initiate topical workshops of current interest
(attached to existing conferences or start new ones)

2. Special Issues for major publications (e.g. T-ED)

3. Panel session topics for major conferences

4. Special Sessions for major conferences

During this year, much effort was spent on organizing an Emerging Technology Session and Evening Panel Discussion within the IEDM. A list of topics for new special issues was proposed. Furthermore, a workshop on compact modeling was initiated. The membership in the committee was put onto a broader basis to account better for the special needs of EDS members worldwide. Details will be described in a later section.

This committee continues to operate entirely by email.

MEMBERSHIP

In our previous report (Dec. 2000 report), we indicated that we will add enough members for the committee to function in 2001.

In choosing new members this year, we continue to execute on our desire to encompass members from Europe, Asia, as well as North America. We made an effort to include members with representations from different technical areas (technology and circuit) and different geographic location, as well as nature of the business (industry vs. academia). The slate of new members for 2001 includes elements of the above criteria. The new committee has 6 members from the US, 3 from South East Asia, 3 from Japan, and 3 from Europe. 8 are from industry and 8 from academia and government institutions.

During the meeting on December 5, 2001 the committee decided to limit the membership to two years, once renewable. In this way the total membership term is limited to a maximum of 4 years. This rule applies also to the chairman. The reason for the change is that it better fits the two-years term of the Adcom than the previous three-years term. It applies to all members whose term does not expire at the end of 2001.
The reason for limitation of the membership term is to make sure that new ideas can be incorporated. Atsushi Hori and Werner Weber will step down at the end of the year since their terms expire. Savvas Chamberlain, Tsu-Jae King, and Pierre Woerlee step down due to other engagement. All other committee members from 2000 were invited to serve for another year. In addition new members should be appointed to replace those who resigned. Jim Hutchby has been appointed the new chairman.
The present members are listed below:

Term started 1999	Term started 2000	Term started 2001
Werner Weber Infineon (Chair, stepping down)	**Lalita Manchanda**, Agere	**Mark Law**, U. Florida
Atsushi Hori, Matsushita (stepping down)	**Ken-ichi Goto**, Fujitsu	**Jeff Welser**, IBM Technology Group
	Savvas Chamberlain, DALSA (stepping down)	**Ilesanmi Adesida**, U. Illinois
	S.C. Sun, ProMos	**Jim Hutchby**, SRC
	Willy Sansen, K.U. Leuven	**Akira Toriumi**, U Tokyo
	Pierre Woerlee, Philips, (stepping down)	**Kwyro Lee**, KAIST
	Tsu-Jae King, UC Berkeley, (stepping down)	
	Xing Zhou, Nanyang Technological University	

IEDM EMERGING TECHNOLOGY SESSION AND PANEL

During the past year an emerging technology session was (again) established at IEDM. The needs of the community to obtain better information on alternative and side topics that may become mainstream in the future have fostered the success of this initiative. This year both the emerging technology session and the evening panel discussion were organized by members of the EDS Technology and Circuits committee in cooperation with the IEDM executive committee. Jeff Welser who is also a member of the IEDM organizing committee organized the session and Jim Hutchby took care of the panel discussion. The topic of both was "interconnects". This topic was selected from numerous proposals worked out in the EDS T&D committee in cooperation with the IEDM organizing committee.

The description below summarizes this year's session:

Background of the Emerging Technology session on "Interconnecting Devices":
The session is entitled "Interconnecting Devices," and consists entirely of invited talks from experts in the field. This year's chosen subject is of critical importance today, due to the increasing need for very high bandwidth operation by high-speed computing, networking, and internet applications. The talks cover a broad range of emerging technologies, including optical and wireless interconnects and novel three-dimensional chip and wiring structures, all aimed to address the challenges of high-speed communication both across a chip and between chips. In addition to giving the IEDM attendees a good overview of future technologies, the session also serves as a launching pad for a lively debate on the topic in the evening panel session to which it is linked: "Interconnecting Devices for the Terabit Era."

Speakers/Topics:

James Meindl	(Georgia Tech)	Future Interconnect/Architecture Challenges
Frank Chang	(UCLA)	Wireless Interconnects
Eric Beyne	(IMEC)	Thin-film Multilayer Wiring / 3D Stack Chips
Sadik Esener	(UCSD)	Optical Interconnects
Sam Purushothaman	(IBM)	K<2 Dielectrics

The Emerging Technology evening panel session at IEDM is entitled "Interconnecting Devices for the Terabit Era: Myths, Rumors, and Heresies, Panel Moderator – Jim Hutchby, SRC

Panel Topic:

Much has been said and written about the looming (arguably, current) problem of global interconnect (intra- and inter-chip), particularly related to intra-chip global clock/signal distribution. Views range from having to replace current Cu/Low-k global interconnect technology with an alternate solution by the 65-nm node in 2007 – to the notion that this "incrementally worsening" problem can be managed via new systems architectures and Cu/Low-k global interconnect modifications. Eventually, however, accelerating clock frequencies (10's of GHz) will drive Cu/Low-k global interconnects to their limit performance. Alternate solutions for global interconnect include optical and RF interconnects (guided wave and free space) and a variety of heterogeneous and monolithic 3D integration approaches. Regarding optical approaches, many diverse views abound. Some speculate that optical interconnect will be used for local or semi-global intra-chip interconnects, while others are skeptical about application of optical approaches even for inter-chip interconnects within multi-chip packages. Others propose new RF communications technologies (CDMA and FDMA) for global interconnect while others are exploiting new markets for heterogeneous 3D integration of mixed functions and technologies. In this "interconnect soup" of

controversial problem definition and myriad technological approaches, the following questions are addressed:

- Is the "Global Interconnect Problem" a "Red Brick Wall" show stopper, or is it a soft limit that eventually will require an alternate solutions?
- What are the issues defining the limits of Cu/Low-k from systems and microprocessor points of view?
- Is optical interconnect a viable technology approach for inter-chip applications. Will it ever be applicable to intra-chip applications? Will the power dissipation be a limiting factor?
- Will RF interconnect provide sufficient number of channels within an achievable bandwidth to be useful? Again, will the power dissipation in RF interconnects be a limiting factor?
- Will 3D integration have significant impact on the global interconnect issue, or will it be more opportunity driven to integrate dissimilar functions and materials? Again, what about the power dissipation and thermal management issues?

PANEL MEMBERS

Frank Chang	UCLA (RF)
Karl Ebeling	Infineon (Optical)
Sadik Esener	UCSD (Optical)
Bob Markunas	Ziptronix (3D Integration)
Jim Meindl	Georgia Institute of Technology (Interconnect Systems Issues)
Shinichi Ogawa	SELETE (Cu/Low-k Technologies)
Ian Young	Intel (Microprocessor Architectural Approaches)
Tom Theis	IBM (Interconnect Systems Issues)

TRANS. ELECTRON DEVICES SPECIAL ISSUE

A list of new proposals for topics of special issues was worked out for the Transactions on Electron Devices and handed over to Doug Verret. As a result invited review articles on SiGe technology, reliability of ultra-thin gate oxides and technology for low power applications were initiated. Furthermore, guest editors were invited to submit proposals on Nanoelectronic Devices, Imaging Technology, Organic Technology and RF, Mixed Signal SOC Technology.

Furthermore, there is an ongoing discussion about a Special Issue on Interconnects for T-ED. This special issue was fermented by a proposal from the VLSI Technology and Circuits Committee in 2000.

WORKSHOP ON COMPACT MODELING

A workshop on compact modeling is organized at the 2002 International Conference on Modeling and Simulation of Microsystems. Workshop organizer is Xing Zhou.

The objective is to create a truly open forum for discussion among experts in the field as well as feedback from technology developers and circuit designers. It consists of *a 2-day Invited Speaker Session*, an *Evening Panel Session*, and a *Tutorial Session*. The topics are centered at bulk-Si and SOI MOSFET compact models for circuit simulation to address the following issues:

- Physics-based I-V model formulations
- Scalable AC/RF/noise models
- Predictive models with process correlation
- Statistical modeling with compact models
- Compact model with higher-order (atomic level) effects
- Parameter extraction
- Global vs local optimization
- Equivalent circuit generation from numerical simulation
- Compact solution from surface-potential-based models
- Benchmark tests and model comparisons
- Role of CM in bridging technology development, TCAD, and circuit design
- Trend and needs in compact models in the VDSM era

INVITED SPEAKER SESSION

There are invited presentations from all over the world (9 countries) to present their work and their views on compact modeling. A selection is listed below, with tentative titles (or areas) of the talk:

- A practical comparison of three modern compact MOS DC models
  Peter Bendix, LSI Logic, USA
- Accounting for ultra-deep submicron aspects in a design oriented MOSFET model
  Matthias Bucher, National Tech. Univ. Greece
- Recent development of the BSIM4 model
  Mansun Chan, Hong Kong Univ. of Science and Tech., Hong Kong
- RF MOS noise parameter extraction and modeling
  Jamal Deen, Mc Master Univ., Canada
- TCAD and ECAD: Is there a connection
  Michael Duane, Applied Materials, USA
- Recent Advances in the EPFL-EKVMOS transistor compact model
  Christian Enz, Swiss Center for Electronics and Microtechnology, Switzerland
- A unified process-based compact model for scaled PD/SOI and bulk-Si MOSFETs
  Jerry Fossum, Univ. Florida, USA
- Gm/Id-based modeling and analog design
  Daniel Foty, Gilgamesh Associates, USA
- Advanced surface-potential-based model (SP)
  Gennady Gildenblat, PennState Univ., USA

- Experimental determination of the electron and hole low field mobility in FD/SOI in the single or double gate operation
  Marco Mastrapasqua, Agere Systems, USA
- How to build an SOI MOSFET compact model without violating the laws of physics
  Josef Watts, IBM, USA
- Xsim: A compact model for bridging technology develpopers and circuit designers
  Xing Zhou, Nanyang Technological Univ., Singapore

EVENING PANEL SESSION

An evening panel session on Trends and needs in compact models in the Very-deep-submicron era is organized. The topic is on the trends and needs of compact models from the perspective of the model developers, device physicists, technoloy developers, CAD vendors, and circuit designers

Moderator: Narain Arora, Simplex Solutions, USA

Panelists:

- *Peter Bendix, LSI Logic, USA*
- *Mansun Chan, Hong Kong University of Science and Technology, Hong Kong*
- *Christian Enz, Swiss Center for Electronics and Microtechnology, Switzerland*
- *Daniel Foty, Gilgamesh Associates, USA*
- *Gennady Gildenblat, Pennsylvania State University, USA*
- *Mitiko Miura-Mattausch, Hiroshima University, Japan*

TUTORIAL SESSION:

Several tutorials are offered by the invitees on special topics, which will be arranged in series with the Invited-Speaker Session (in parallel with other MSM2002 sessions) for the general audience:

- The basic formulation of the BSIM4 model
  Mansun Chan, Hong Kong University of Science and Technology, Hong Kong
- MOS transistor RF modeling for RF IC design
  Christian Enz, Swiss Center for Electronics and Microtechnology, Switzerland
- Implications of modeling (good or bad) on circuit design
  Daniel Foty, Gilgamesh Associates, USA
- Automatic generation of compact RF models directly from device simulation
  Serge Luryi, State Universtiy of New York at Stony Brook, USA
  Andrea Pacelli, State Universtiy of New York at Stony Brook, USA
- MOSFET model HiSIM
  Mitiko Miura-Mattausch, Hiroshima University, Japan

EDS WEBSITE

Xing Zhou created and is updating the website for this committee. This website was transferred to Chris Salicco at IEEE past summer to facilitate continuity in times when Xing will no longer be a member of the committee. He has another year in the committee. It will be the task of next year's committee to find an individual to replace Xing as the person responsible for updating the website.

The website describes our committee's activities and should be a good forum to disseminate information to EDS members. The URL link can be found in the EDS homepage under EDS Technical Committees and Other Technically Related Groups, URL: http://www.ieee.org/organizations/society/eds/groups.html, and EDS Roster http://www.ieee.org/organizations/society/eds/roster.html