Design & Modeling of Nanodevices – Design Exercise

❑ Objectives

- Design and model short-channel MOSFETs through (simple) analytic compact model equations.
- Understand basic transistor (linear/saturation/subthreshold) equations and their derivations, as well as major related effects (such as pinned surface potential, bulk-charge linearization, velocity saturation, vertical-field mobility degradation, etc.) and major assumptions (such as gradual-channel approximation, charge-sheet model, drift-diffusion, etc.).
- Understand major short-channel effects (SCEs), such as threshold voltage "roll-off" and "drain-induced barrier lowering" (DIBL), and their simple models ("triangle" & "trapezoidal" charge-sharing model, and "halo" for revers SCE).
- Relate basic transistor parameters (such as threshold voltage, drive/leakage currents, etc.) with fundamental physical parameters, such as gate oxide thickness (T_{ox}), source/drain junction depth (X_j), body/halo doping (N_A/N_{pile}), etc.
- Experience model parameter extraction and its role in compact modeling.
- Study the effects of physical parameter variations on transistor behaviors through compact modeling**,** and understand design trade-offs in submicron device performance optimization.
- Learn and appreciate model development and data analysis for multi-target optimization in multi-variable design space.

❑ Tasks

- Review and understand the basic MOS transistor equations: linear, saturation, and subthreshold currents, and threshold voltages including (simple) charge-sharing and "halo" models (see lecture notes).
- Code basic compact model equations using any available programming language (Matlab, C, or any spread-sheet).
- Extract model parameters using relevant numerical data from NM6604 Design Exercise for a given 0.25-μm process.
- Define transistor performance parameters (such as I_{on}, I_{off}, V_{t0}, V_{ts}, etc.; see lecture notes) and evaluate (calculate) their behaviors with respect to physical-parameter variations, e.g.,

- V_t vs. N_A at various T_{ox};
- V_t vs. T_{ox} at various N_A
- V_t vs. V_{sb} at various N_A and T_{ox}
- V_{t0} and V_{ts} vs. L_g at various N_A, T_{ox}, X_j as well as "halo" (κ, β)
- log(I_{dlin}) and log(I_{dsat}) vs. V_{gs}, and label I_{on} and I_{off}
- I_{on} and I_{off} vs. L_g at various N_A, T_{ox}, X_j as well as "halo" (κ, β)
- I_{off} vs. I_{on} at various L_g and given N_A, T_{ox}, X_j, and "halo" (κ, β)

- *Obtain "contour plots" for device targets versus a pair of physical variables for performance optimization and "parameter windows", e.g.,
  - V_{t0}, V_{ts}, I_{on}, I_{off} contours with respect to N_A and T_{ox}

➢ ***Exercise***: Through transistor compact modeling, observe and optimize the transistor performance through physical parameter variation. By tuning V_t "roll-off" and "roll-up" of the ***V_t* vs. *L_g*** characteristics for a given short-channel transistor (e.g., L_g = 0.25 μm), obtain improved "on/off" current trade-off (***I_{off}* vs. *I_{on}*** at various L_g) for logic-circuit applications. The following are suggested:

- Vary gate oxide thickness (T_{ox}) together with body doping (N_A), and/or additionally with junction depth (X_j) for improved I_{off} and I_{on}.
- Introduce "halo" with various N_{pile} (κ) and I_β (β) values, combined with T_{ox} and/or N_A variations for improved I_{off} and I_{on}.
- Propose and define new device performance parameters, e.g., transconductance (g_m) and drain conductance (g_d) as well as intrinsic voltage gain (g_m/g_d), and evaluate from the compact models.
- *Propose different *approaches* and *guidelines* to transistor performance optimization.

❑ **Continuous assessment and report submission**

- ***Submit an individual written report summarizing your approach and understanding***, **including your new proposals for open-ended questions*. Attach your codes in an Appendix***.*
- ***Due***: **Friday, 10 November 2023**. Softcopy of the report, together with the programming code (as an appendix), submit through email: exzhou@ntu.edu.sg; or Hardcopy submit to my Office (S1-B1c-95, 6790-4532).

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