Virtual Process Integration (VPI) – Design Exercise

❑ Syllabus

- Wafer-split experiment. Device-target vs. process-variable relations. Transistor performance optimization/trade-offs through process variation. Technology development and optimization.
- Design of Experiment (DOE): Implement a computer experiment to study the scaling characteristics (varying gate length) of the given sub-micron technology. Study the influence of process variations on device performance parameters.

❑ Objectives

- Design and simulate the processing and characteristics of nMOS transistors for a given 0.25-μm (2.5-V) CMOS logic process.
- Observe layer structures and profiles at various stages of the process.
- Visualize transistor operation in terms of terminal *I*–*V* characteristics as well as internal doping, potential, field, carrier, current distributions.
- Observe and relate device performance parameters to process variations.
- Understand design trade-offs in submicron device performance optimization.
- Learn data analysis and graphical prediction from numerical data.

❑ Tasks

- Review and understand the basic definitions of MOS transistor performance parameters: linear and saturation threshold voltages (V_{t0} and V_{ts}), on-state saturation current (I_{dsat} or I_{on}), off-state leakage current (I_{off}), transconductance (g_m), and subthreshold swing (S_t).

Linear threshold voltage:	$V_{t0} \equiv V_{gs} \mid I_{ds} = 0$ @ g_{m0}=max (V_{ds} = 0.05 V)
Critical current:	$I_{crit} = I_{ds}$ @ $V_{gs} = V_{t0}$ (V_{ds} = 0.05 V)
Saturation threshold voltage:	$V_{ts} \equiv V_{gs} \mid I_{ds} = I_{crit}$ (V_{ds} = 2.5 V)
On-state saturation current:	$I_{on} \equiv I_{ds} \mid V_{gs} = V_{ds}$ = 2.5 V
Off-state leakage current:	$I_{off} \equiv I_{ds} \mid V_{gs} = 0$, V_{ds} = 2.5 V
Transconductance:	$g_{ms} \equiv dI_{ds}/dV_{gs}$ ($V_{gs} = V_{ds}$ = 2.5 V)
Subthreshold swing:	$S_{ts} \equiv \Delta V_{gs}/\Delta\log(I_{ds})$=1dec (mV/dec) ($V_{ds}$ = 2.5 V)

All the above are at zero body bias: V_{sb} = 0. For body effect, threshold voltage is defined as: $V_t(V_{sb}) \equiv V_{gs} \mid I_{ds} = I_{crit}$ (V_{ds} = 0.05 V, V_{sb} = 2.5 V)

- With reference to the given CMOS process recipe, implement the process to simulate only the nMOS transistor of the 0.25-μm CMOS process. The resulting structures of your design of experiment (DOE) will be used to investigate the device scaling characteristics and performance optimization with process variations.

  - View device structures and doping profiles at the end of various major processing steps.

  - Create transistors with different gate lengths, obtain various device *I*–*V* characteristics, such as I_{ds}–V_{gs}, log(I_{ds})–V_{gs}, and I_{ds}–V_{ds}, and extract device parameters (V_{t0}, V_{ts}, g_{ms}, S_{ts}, I_{on}, I_{off}) into the RunTable.

- Study the *transistor scaling characteristics*: performance parameters (V_t, I_{on}, I_{off} as well as g_m and S_t) as a function of decreasing gate length, L_g.

  - Obtain MEDICI device structures of different gate lengths using structure truncation/reflection (Recommended: L_g = 10, 1, 0.5, 0.35, 0.25, 0.2, 0.18, 0.15 μm).

  - Obtain ***technology optimization*** curves, e.g., V_{t0}–log(L_g), V_{ts}–log(L_g), g_m–log(L_g), S_t–log(L_g), I_{on}–log(L_g), log(I_{off})–log(L_g), and log(I_{off})–I_{on}. Understand different aspects of and concerns for short-channel effects.

➢ ***Exercise***: Through DOE, split wafer with selected process variations. Observe and optimize the device performance through target–variable relationship. Determine new process variables for improved "on/off" current trade-off for logic-circuit applications. Specifically, by tuning the given process such that for the ***designed*** $\boldsymbol{L_g}$ **= 0.25 μm device**, "on/off" current performance can be improved (i.e., I_{on} increased and I_{off} decreased), with the *guide* that the linear threshold voltage at L_g = 0.25 μm is relatively unchanged. The following experiments are suggested:

  - Tune the gate oxide thickness (t_{ox}) in the gate oxidation step (e.g., vary gate-oxidation *time t*) together with tuning the channel average doping (N_A) in the V_t-adjustment implant step (e.g., vary the V_t-implant *dose* Φ and/or the "halo" implant dose/energy/tilt) such that the $\boldsymbol{L_g}$ **= 0.25 μm** device I_{on} and I_{off} can both be improved.

  - Compare technology optimization curves of your "new" wafer with the "original" (given) wafer, and understand why your new process is better than the original given process.

❑ **Continuous assessment and report submission**

- ***Submit an individual written report summarizing your approach and understanding. Due***: **Friday, 13 October 2023**. Softcopy of the report submit through email: exzhou@ntu.edu.sg; or Hardcopy submit to my office (S1-B1c-95, 6790-4532).