

EE4613 Course Schedule (Device/Integration Modules)

EE4613

CMOS Process and Device Simulation

No.	Week of	Subject	Monday (F61)	Friday (F62)
			1:30–4:30 pm	1:30–4:30 pm
5	11 Sep	Introduction: TCAD and Device Modeling	11/9	15/9
6	18 Sep	VisualFab: VWF / DOE	18/9	22/9
7	25 Sep	VDS: Device Characterization	25/9	29/9
<i>B</i>	2 Oct	<i>Make-up</i> for Deepavali/Overseas - VPI: Process Integration	2/10	6/10
8	9 Oct	VPI: Process Integration	9/10	13/10
9	16 Oct	VPI: Design Exercise	16/10	20/10
10	23 Oct	VPI: Design Exercise (F61)	23/10	27/10 [no class]
11	30 Oct	VPI: Design Exercise / Quiz-2 (45min, start at 3:30pm)	30/10	3/11
12	6 Nov	Summary (F61) / VPI: Design Exercise (F62)	6/11	10/11
13	13 Nov	Summary (F62)	13/11 [no class]	17/11

❑ **Venue: Device Fabrication Simulation Lab (S2-B5a-01)**

❑ **Continuous assessment:**

- **Quiz-2** (MCQ, open-book – tests the knowledge of basic MOSFET device theory & operations (~45min, start at 3:30pm): **30 Oct / 3 Nov 2023** for F61/F62, respectively.
- **Design Exercise report** (individual). See *Notes* in the Design Exercise.
Due: Latest by **9/20 Nov 2023** for F61/F62, respectively. Softcopy submit by email (exzhou@ntu.edu.sg); hardcopy (if any hand-written) submit to my office (S1-B1c-95). Marked reports to be sent back by email before the exam.
- **Individual performance** (based on lab participation and activities, including Q&A and approach to problem solving).

❑ **Final examination:** Two hours. Open book, open notes, open mind. Covers the full contents (3 Modules).