DIP: Project Proposal

Title: **Virtual Transistor Fabrication and Characterization**
Group: E036
Lab: Nanoelectronics Design Lab (S2-B5a-01)
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In order to have good returns on investments on the real fabrication process of transistors and IC chips, "virtual transistors" based on process/device simulations are needed to enhance design predictability, increase design productivity, and boost chip performance.

According to the recently issued O-S-D Report, "since the early 1990s, power transistor applications have steadily expanded in automotive electronics, personal computers, cell phones, industrial equipment, home appliances, consumer electronics, and many battery-operated portable products. From 1990 to 2010, the power transistor market is expected to increase at a cumulative average growth rate (CAGR) of 8% per year to $10.5 billion in 2010, based on IC Insights' forecast. During this 21-year time span, the entire discrete semiconductor market will increase at a CAGR of 5%."

The real fabrication process of transistors is fabricated onto a silicon wafer. This process is irreversible. Optimizations of the transistors are done together with the fabrication. Trials-and-errors through wafer-split experiments are carried out to find the optimized parameters. This trial-and-error is costly if a design of experiment (DOE) is not properly designed. Some design targets may not be observable at certain individual steps and, therefore, it is difficult to determine the exact parameters. Moreover, the fabrication is affected by the inevitable statistical process fluctuations.

Furthermore, it costs more than $3 million a day to pay off the $5 billion investment of a fab over a five-year schedule. In order to generate that much money, high utilization of the fabrication equipment has to be maintained. Experimental wafers utilize the machine time for production and, hence, increase the cost. Errors and testing of wafers in the real fabrication process will contribute to the amount of wastage which, in turn, will increase the costs. To reduce the number of experimental wafers, virtual transistor fabrication is widely used in all fabs. The virtual fabrication process is simulated according to a given real process recipe. In virtual fabrication, a step-by-step process can be followed and physical parameters can be observed.

With the aforementioned background and incentive, our group's DIP aims to demonstrate the idea of virtual transistor fabrication and characterization via technology computer-aided design (TCAD). A particular example for optimizing transistor drive current (Ion) and minimizing leakage current (Ioff) is carried out, which has been achieved through process variations of the threshold-adjustment implant and gate-oxidation process steps.

Our group has run simulated fabrication and characterization of the virtual transistors. We are able to observe the graphical and numerical results at every major process step of a given CMOS recipe. To emulate a wafer-split experiment, necessary changes to the selected input variables can be varied to achieve the target results. We show that the idea of virtual fabrication can be extended to a generic multi-target optimization in a multi-variable design space, and to generate process windows for trading-off performance parameters.

With the help of virtual transistor fabrication, it is possible to take design for manufacturability (DFM) into consideration even before fabricating silicon wafers. This enables the fabs to maximize their return on investment through cost reduction, cycle time reduction, and yield maximization.