Call for Papers

IEEE International Workshop on

Compact Thin-Film Transistor Modeling for Circuit Simulation

Date: September 11 - 12, 2008

Location: The Møller Centre, Cambridge, UK

Organized by:

IEEE EDS Compact Modeling Technical Committee

In collaboration with:

London Center for Nanotechnology, University College of London, UK

Electrical Engineering Division, Engineering Department, Cambridge University, UK

IEEE UK-RI (AP/ED/LEO/MTT) joint Chapter

In recent years, the increasing use of active matrix flat-panel displays and bio-medical imagers in commercial electronic products has drawn significant attention to “thin-film transistors (TFT)” and integration technologies. TFTs on amorphous- and poly-silicon as well as newly emerging organic and transparent metal oxide semiconductor technologies are becoming increasingly common. For example, flat panel displays are finding widespread use in many products such as cellular phones, personal digital assistants (PDAs), camcorders, laptop personal computers (PCs), to name a few. The active matrix display is composed of a grid or matrix of picture elements called "pixels". Thousands or millions of these pixels together create an image, in which the TFT acts as a switch to individually turn on and off each pixel. More increasingly these devices are starting to be used as analog circuit elements for rudimentary signal conditioning. Therefore, physically-based compact modeling of TFTs for circuit simulation is crucial to accurately and reliably predict TFT behavior in the active matrix and concentrated R&D efforts along these lines for TFTs in emerging thin-film technologies are currently underway world-wide. Thus, this workshop will provide a forum for discussions and current practices on compact TFT modeling. A partial listing of the **areas of interest includes:**

- **Physics of TFTs and operating principles**
- **Compact TFT device models for circuit simulation**
- **Model implementation and circuit analysis techniques**
- **Model parameter extraction techniques**
- **Applications of compact TFT models in emerging products**
- **Compact models for interconnects in active matrix flat panels**

ABSTRACT SUBMISSION DEADLINE: July 15, 2008

Submission of Final PowerPoint presentation: August 15, 2008

Prospective authors should submit a 500-word abstract to *any one* of the following email addresses:

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