Call for Papers for Special Issue of IEEE TRANSACTIONS ON ELECTRON DEVICES on

Compact Interconnect Models for Giga Scale Integration

The special issue is devoted to the research and development activities on emerging compact interconnection models for advanced circuit simulation using 65-nm silicon technology and below. The continuous scaling of CMOS devices to sub-90 nm regime has resulted in higher device density, faster circuit speed, and lower power dissipation. As VLSI technology shrinks below 90-nm geometries with Cu/low-k interconnects, the parasitics due to interconnections are becoming a limiting factor in determining the circuit performance. Therefore, accurate modeling of interconnection parasitic resistance (R), capacitance (C), and inductance (L) is essential in determining various on-chip interconnect-related issues such as delay, cross-talk, IR drop, and power dissipation. Thus, accurate compact interconnection models are crucial for the design and optimization of advanced VLSI circuits for 65-nm CMOS technology and below. In addition, with the emerging technologies based on Carbon Nano-Tubes (CNTs) and Graphene Nano-Ribbons (GNR), etc., compact interconnection models suitable for these technologies are crucial for advanced circuit design.

The presently available interconnection models based-on field-solvers provide high accuracy. However, they are inadequate for an accurate and meaningful analysis of today's chip with millions of devices. Therefore, advanced compact interconnection models are urgently needed for accurate simulation of on-chip global interconnections and speed-power optimization using advanced interconnection technologies. The ongoing R&D efforts indicate that the emerging compact interconnection models based on analytical equations and compatible with circuit simulation tools show an excellent promise for full-chip analysis of advanced interconnection technologies of sub-90-nm nodes. Therefore, the objective of this special issue is to bring together a diversity of R&D activities and advancement in compact models for the passive components integrated in an advanced silicon technology. A partial list of the **areas of interest is:**

- **Compact RLCK Interconnect Models**
- **Compact Models for Cu/low-k Technologies**
- **2D/3D Compact Interconnect Models**
- **Carbon Nanotube Interconnect Models**
- **Graphene Nano-Ribbon Interconnect Models**
- **RF and Microwave Modeling**
- **Interconnect Modeling for SoC Design**
- **Interconnect Variability and Statistical Modeling**

Submission deadline: January 16, 2009

In preparing the manuscript please follow the guidelines for authors on the inside back cover of the transactions. Indicate that the manuscript is for this special issue. Direct all manuscripts, correspondence, and communications to:

Jo Ann Marsh
IEEE/EDS Publications Office
445 Hoes Lane, P.O. Box 1331
Piscataway, NJ 08854-1331, USA
Phone: +1 732 562 6855, Fax: +1 732 562 6831
E-mail: j.marsh@ieee.org

Guest Editors

Dr. Samar K. Saha
Silterra USA, Inc.
1740 Technology Drive, Suite 530
San Jose, CA 95110, USA
E-mail: samar@ieee.org

Prof. M. Jamal Deen,
McMaster University, ECE Dept., CRL 226
1280 Main Street West
Hamilton, ON L8S 4K1 CANADA
E-mail: jamal@mcmaster.ca

Dr. Hiroo Masuda
Renesas Technology
5-20-1, Josuihon-Cho, Kodaira-shi,
Tokyo, Japan – 187-8588
E-Mail: masuda.hiroo@renesas.com

Scheduled publication: September 2009