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EDUCATION

- Ph.D., Electrical Engineering, University of Rochester, Rochester, New York, U.S.A., October 1990.
- M.S., Electrical Engineering, University of Rochester, Rochester, New York, U.S.A., May 1987.
- B.E., Electrical Engineering, Tsinghua University, Beijing, P.R.C., July 1983.

EMPLOYMENT

- Since 1/2000 *Associate Professor*, School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore.
- 1/1999 — 12/1999 *Assistant Professor*, School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore.
- 3/1995 — 12/1998 *Lecturer*, School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore.
- 3/1992 — 3/1995 *Research Fellow*, School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore.
- 9/1991 — 2/1992 *Senior Scientist*, ANAmation, Inc., U.S.A.
- 9/1990 — 8/1991 *Research Associate*, Department of Electrical Engineering, University of Rochester, U.S.A.
- 9/1987 — 8/1990 *Graduate Research Fellow*, Department of Electrical Engineering, University of Rochester, U.S.A.
- 9/1985 — 8/1987 *Graduate Research Assistant*, Department of Electrical Engineering, University of Rochester, U.S.A.

MEMBERSHIPS

- Since 2002 Member, Circuits and Systems Society, IEEE.
- Since 1999 Senior Member, IEEE.
- Since 1994 Member, Electron Devices Society, IEEE.
- 1991 — 1999 Member, IEEE.
- 1988 — 1990 Student Member, IEEE.

AWARDS AND HONORS

- Visiting Professor, Ultra-Scaled Device Laboratory, Hiroshima University, Japan, Jan. 2003.
- Visiting Fellow, LSI Logic Corp. and Center for Integrated Systems, Stanford University (under *Overseas Attachment Program* awarded by Nanyang Technological University), Feb.–Mar. 2001.

- Listed in *Who's Who in the World* since 1998 (15th edition) and *Who's Who in Science and Engineering* since 2000 (5th edition).
- Visiting Fellow, Center for Integrated Systems, Stanford University (under *Tan Chin Tuan Exchange Fellowship* awarded by Nanyang Technological University), Nov.–Dec. 1997.
- Scholarship for the degree Master of Science in U.S.A., Ministry of Education, P.R.C., 1985 (selected among 20 students from top 5 universities nationwide).

PROFESSIONAL ACTIVITIES

- Member of the *IEEE Singapore Section REL/CPMT/ED Chapter Committee*, since 2002.
- Member of the *IEEE EDS Regions/Chapters Committee*, since 2002.
- Member of the *IEEE EDS Compact Modeling Technical Committee*, since 2001.
- Member of the *IEEE EDS VLSI Technology and Circuits Technical Committee*, since 2000.
- Lecturer of the *IEEE EDS Distinguished Lecturer Program*, since 2000.
- Member of the Editorial Advisory Board, *Journal of Modeling and Simulation of Microsystems (JMSM)*, Applied Computational Research Society, Cambridge, MA, since 2000.
- Member of the Program Committee, *the 7th International Conference on Modeling and Simulation of Microsystems (MSM2004)*, the 2004 NanoTech Conference and Trade Show (NanoTech2004), Boston, MA, Mar. 7–11, 2004.
- Organizer for the *Workshop on Compact Modeling at the 2003 International Conference on Modeling and Simulation of Microsystems (WCM-MSM2003)*, San Francisco, CA, Feb. 25–27, 2003.
- Member of the Program Committee, *the 6th International Conference on Modeling and Simulation of Microsystems (MSM2003)*, the 2003 NanoTech Conference and Trade Show (NanoTech2003), San Francisco, CA, Feb. 23–27, 2003.
- Co-chairman of the MOS-AK special session at *the 9th International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES2002)*, Wroclaw, Poland, June 20–22, 2002.
- Organizer for the *Workshop on Compact Modeling at the 2002 International Conference on Modeling and Simulation of Microsystems (WCM-MSM2002)*, San Juan, Puerto Rico, April 23–25, 2002.
- Member of the Program Committee, *the 5th International Conference on Modeling and Simulation of Microsystems (MSM2002)*, San Juan, Puerto Rico, April 22–25, 2002.
- Member of the Organizing Committee and Publicity Chair, *the 2nd International Symposium on Photonics and Applications (ISPA2001)*, co-sponsored by SPIE, Singapore, Nov. 26–30, 2001.
- Member of the Program Committee and Session Chair, *the 4th International Conference on Modeling and Simulation of Microsystems (MSM2001)*, Hilton Head Island, SC, Mar. 19–21, 2001.
- Member of the Organizing Committee and Publicity Chair, *the 2nd International Symposium on Microelectronics and Assembly (ISMA2000)*, co-sponsored by SPIE, Singapore, Nov. 27–30, 2000.

- Member of the Program Committee and Special Session Organizer, *the 3rd International Conference on Modeling and Simulation of Microsystems (MSM2000)*, San Diego, CA, Mar. 27–29, 2000.
- Sessions Chair for *the 8th International Symposium on IC Technology, Systems & Applications (ISIC-99)*, Singapore, Sept. 8–10, 1999.
- Member of the Technical Program Committee and Sessions Chair, *the 7th International Symposium on IC Technology, Systems & Applications (ISIC-97)*, Singapore, Sept. 10–12, 1997.
- Reviewer for *IEEE Transactions on Electron Devices*, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, *Solid-State Electronics*, and *International Journal of Electronics*.

CONSULTING

- 1996 National Supercomputing Research Center, Singapore.
- 1991 — 1992 ANAmation, Inc., Rochester, New York, U.S.A.

TEACHING

- E202/E316: Analog Electronics
- E6605: Sub-Micron Semiconductor Process and Device Simulation
- E422/E411: Integrated Circuits: Process, Device & Circuit Design.
- E425: TCAD: Process and Device Simulation.
- G265: Mathematics 2B.
- E272: Series Resonance and Transient Response of RLC Networks.
- E227: Design of a Linear Power Supply.
- E222: Design Study of an Audio Power Amplifier.
- E322: Design of a Semi-Custom IC.
- Supervised 2 post-doctoral fellows, 2 Ph.D., 4 masters, and 24 B.E. students.

RESEARCH

Projects

- Computational Investigation of Novel Device Structures and Concepts (P.I.)
- Multi-Level Modeling of ULSI Systems in the Very-Deep-Submicron Technology Era (P.I.).
- Project DOUST: Design and Optimization of Ultra-Small Transistors (P.I.).
- Design, Modeling, and Characterization of Submicron MOSFETs (P.I.).
- Predictive Technology Modeling for Deep-Submicron MOSFET Design (P.I.).
- TCAD-Synthesis Approach to Deep-Submicron MOS Technology Development (P.I.)
- Circuit Modeling and Parameter Extraction for MMIC Applications (P.I.).
- Device Modeling and Characterization with TCAD for MMIC Applications (P.I.).
- Mixed-Mode Analog–Digital Circuit Simulation (P.I.).

- Strategic Research Program on Nanoscience Initiative - Modelling and Self Assembly of Molecular Semiconductors for Nanoscale Electronic Integration (Collaborator).
- Core Capabilities Development in III-V Compound Semiconductor for Wireless Communication Devices and MMICs (Collaborator).
- Development of Power MMICs (Collaborator).
- Establishment of Teaching and Research Facilities for Semiconductor Wafer Fabrication Technology (MicroFabrication Laboratory, MFL) (Group Member).

University Collaborations

- Prof. Mitiko Miura-Mattausch, Hiroshima University, Japan
  Compact modeling for circuit simulation.
- Assoc. Prof. Mahesh B. Patil, Indian Institute of Technology, Bombay, India
  DOUST/SEQUEL: MOSFET Compact Modeling (CM) and Look-Up Table (LUT) Circuit Simulation.

Industry Interactions

- Chartered Semiconductor Manufacturing Ltd., Singapore.
- LSI Logic Corp., USA.

Major Achievements

- Developed a unique one-region scalable compact I_{ds} model for deep-submicron MOSFET's with a small number of fitting parameters using one-iteration parameter extraction and minimum measurement data, with correlation to process variables.
- Developed a simple method for direct measurement and modeling of electrical effective channel length for submicron MOSFET's, with correlation to LDD lateral diffusion and critical-dimension (CD) correction.
- Proposed a novel hetero-material gate MOSFET, which demonstrates the potential for breaking the barrier of MOSFET scaling beyond 0.1-μm technologies.
- Established the theory on the mechanism of subpicosecond electrical pulse generation by nonuniform illumination of MSM transmission-line gaps based on Monte Carlo and numerical techniques.
- Developed a unique dynamic-delay model, which includes the effects of nonlinear loading, input transition time, and multiple-input triggering, and implemented in a single-engine mixed-circuit/gate level simulator.

PUBLICATIONS

Referred International Journal

1. **X. Zhou**, "The Missing Link to Seamless Simulation," (*Invited Feature Article*), *IEEE Circuits Devices Mag.*, vol. 19, no. 3, pp. 9–17, May 2003.
2. K. Y. Lim and **X. Zhou**, "An analytical effective channel-length modulation model for velocity overshoot in submicron MOSFETs based on energy-balance formulation," *Microelectronics Reliability*, vol. 42, no. 12, pp. 1857–1864, Dec. 2002.
3. **X. Zhou** and K. Y. Lim, "De-embedding Length-Dependent Edge-Leakage Current in Shallow Trench Isolation Submicron MOSFETs," *Solid-State Electron*., vol. 46, no. 5, pp. 769–772, May 2002.

4. K. Y. Lim and **X. Zhou**, "MOSFET Subthreshold Compact Modeling with Effective Gate Overdrive," *IEEE Trans. Electron Devices*, vol. 49, no. 1, pp. 196–199, Jan. 2002.
5. K. Y. Lim, **X. Zhou**, and Y. Wang, "Physics-Based Threshold Voltage Modeling with Reverse Short Channel Effect," *J. Modeling Simulation Microsystems (JMSM)*, vol. 2, no. 1, pp. 51–55, 2001.
6. **X. Zhou** and K. Y. Lim, "Unified MOSFET Compact *I–V* Model Formulation through Physics-Based Effective Transformation," *IEEE Trans. Electron Devices*, vol. 48, no. 5, pp. 887–896, May 2001.
7. **X. Zhou**, K. Y. Lim, and W. Qian, "Threshold Voltage Definition and Extraction for Deep-Submicron MOSFETs," *Solid-State Electron*., vol. 45, no. 3, pp. 507–510, Apr. 2001.
8. K. Y. Lim and **X. Zhou**, "A Physically-Based Semi-Empirical Effective Mobility Model for MOSFET Compact *I–V* Modeling," *Solid-State Electron*., vol. 45, no. 1, pp. 193–197, Jan. 2001.
9. K. Y. Lim and **X. Zhou**, "A Physically-Based Semi-Empirical Series Resistance Model for Deep-Submicron MOSFET *I–V* Modeling," *IEEE Trans. Electron Devices*, vol. 47, no. 6, pp. 1300–1302, June 2000.
10. **X. Zhou**, "Exploring the Novel Characteristics of Hetero-Material Gate Field-Effect Transistors (HMGFET's) with Gate-Material Engineering," *IEEE Trans. Electron Devices*, vol. 47, no. 1, pp. 113–120, Jan. 2000.
11. **X. Zhou**, K. Y. Lim, and D. Lim, "A General Approach to Compact Threshold Voltage Formulation Based on 2-D Numerical Simulation and Experimental Correlation for Deep-Submicron ULSI Technology Development," *IEEE Trans. Electron Devices*, vol. 47, no. 1, pp. 214–221, Jan. 2000.
12. T. Tang and **X. Zhou**, "Multi-Level Digital/Mixed-Signal Simulation with Automatic Circuit Partition and Dynamic Delay Calculation," *J. Modeling Simulation Microsystems (JMSM)*, vol. 1, no. 2, pp. 83–89, Dec. 1999.
13. **X. Zhou**, K. Y. Lim, and D. Lim, "A New 'Critical-Current at Linear-Threshold' Method for Direct Extraction of Deep-Submicron MOSFET Effective Channel Length," *IEEE Trans. Electron Devices*, vol. 46, no. 7, pp. 1492–1494, July 1999.
14. **X. Zhou**, K. Y. Lim, and D. Lim, "A Simple and Unambiguous Definition of Threshold Voltage and Its Implications in Deep-Submicron MOS Device Modeling," *IEEE Trans. Electron Devices*, vol. 46, no. 4, pp. 807–809, Apr. 1999.
15. **X. Zhou** and W. Long, "A Novel Hetero-Material Gate (HMG) MOSFET for Deep-Submicron ULSI Technology," *IEEE Trans. Electron Devices*, vol. 45, no. 12, pp. 2546–2548, Dec. 1998.
16. **X. Zhou**, T. Tang, L. S. Seah, C. J. Yap, and S. C. Choo, "Numerical Investigation of Subpicosecond Electrical Pulse Generation by Edge Illumination of Silicon Transmission-Line Gaps," *IEEE J. Quantum Electron.*, vol. 34, no. 1, pp. 171–178, Jan. 1998.
17. **X. Zhou**, "Numerical Physics of Subpicosecond Electrical Pulse Generation by Nonuniform Gap Illumination," *IEEE J. Quantum Electron.*, vol. 32, no. 9, pp. 1672–1679, Sept. 1996.
18. **X. Zhou**, "On the Physics of Femto-second Electrical Pulse Generation by Nonuniform Gap Illumination," *OPTOELECTRONICS—Devices and Technologies*, vol. 10, no. 4, pp. 491–504, Dec. 1995.

19. **X. Zhou** and H. S. Tan, "Monte Carlo Formulation of Field-Dependent Mobility for $Al_xGa_{1-x}As$," *Solid-State Electron.*, vol. 38, no. 6, pp. 1264–1266, June 1995.
20. **X. Zhou**, S. Alexandrou, and T. Y. Hsiang, "Monte Carlo investigation of the intrinsic mechanism of subpicosecond pulse generation by nonuniform gap illumination," *J. Appl. Phys.*, vol. 77, no. 2, pp. 706–711, Jan. 1995.
21. **X. Zhou**, "Electron Transport in Graded-Band Devices: Interplay of Field, Composition and Length Dependencies," *Solid-State Electron.*, vol. 37, no. 11, pp. 1888–1890, Nov. 1994.
22. **X. Zhou** and H. S. Tan, "Monte Carlo formulation of velocity–field characteristics and expressions for $Al_xGa_{1-x}As$," *Int. J. Electron.*, vol. 76, no. 6, pp. 1049–1062, June 1994.
23. **X. Zhou**, "Regional Monte Carlo Modeling of Electron Transport and Transit-Time Estimation in Graded-Base HBT's," *IEEE Trans. Electron Devices*, vol. 41, no. 4, pp. 484–490, Apr. 1994.
24. **X. Zhou** and T. Y. Hsiang, "Monte Carlo determination of femtosecond dynamics of hot-carrier relaxation and scattering processes in bulk GaAs," *J. Appl. Phys.*, vol. 67, no. 12, pp. 7399–7403, June 1990.
25. **X. Zhou**, T. Y. Hsiang, and R. J. Dwayne Miller, "Monte Carlo study of photogenerated carrier transport in GaAs surface space-charge fields," *J. Appl. Phys.*, vol. 66, no. 7, pp. 3066–3073, Oct. 1989.

International Conference

1. **X. Zhou**, S. B. Chiah, and K. Y. Lim, "A Technology-Based Compact Model for Predictive Deep-Submicron MOSFET Modeling and Characterization," (*Invited Paper*), *Proc. of the 6th International Conference on Modeling and Simulation of Microsystems (WCM-MSM2003)*, San Francisco, CA, Feb. 23–27, 2003, vol. 2, pp. 266–269.
2. S. B. Chiah, **X. Zhou**, and K. Y. Lim, "Unified Length-/Width-Dependent Threshold Voltage Model with Reverse Short-Channel and Inverse Narrow-Width Effects," *Proc. of the 6th International Conference on Modeling and Simulation of Microsystems (WCM-MSM2003)*, San Francisco, CA, Feb. 23–27, 2003, vol. 2, pp. 338–341.
3. S. B. Chiah, **X. Zhou**, and K. Y. Lim, "Unified Length-/Width-Dependent Drain Current Model for Deep-Submicron MOSFETs," *Proc. of the 6th International Conference on Modeling and Simulation of Microsystems (WCM-MSM2003)*, San Francisco, CA, Feb. 23–27, 2003, vol. 2, pp. 342–345.
4. **X. Zhou**, "Mixed-Signal Multi-Level Circuit Simulation: An Implicit Mixed-Mode Solution," (*Invited Plenary Paper*), *Proc. of the 9th International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES2002)*, Wroclaw, Poland, June 2002, pp. 27–31.
5. **X. Zhou**, "Multi-Level Modeling of Deep-Submicron MOSFETs and ULSI Circuits," (*Invited Paper*), *Proc. of the 9th International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES2002)*, Wroclaw, Poland, June 2002, pp. 39–44.
6. **X. Zhou**, "Xsim: A Compact Model for Bridging Technology Developers and Circuit Designers," (*Invited Paper*), *Proc. of the 5th International Conference on Modeling and Simulation of Microsystems (WCM-MSM2002)*, San Juan, Puerto Rico, Apr. 2002, pp. 710–714.
7. S. B. Chiah, **X. Zhou**, K. Y. Lim, A. See, and L. Chan, "Physically-Based Approach to Deep-Submicron MOSFET Compact Model Parameter Extraction," *Proc. of the 5th International*

Conference on Modeling and Simulation of Microsystems (WCM-MSM2002), San Juan, Puerto Rico, Apr. 2002, pp. 750–753.

8. K. Y. Lim and **X. Zhou**, "Compact Model for Manufacturing Design and Fluctuation Study," *Proc. of the 5th International Conference on Modeling and Simulation of Microsystems (WCM-MSM2002)*, San Juan, Puerto Rico, Apr. 2002, pp. 746–749.
9. **X. Zhou**, S. B. Chiah, and K. Y. Lim, "A Compact Deep-Submicron MOSFET g_{ds} Model Including Hot-Electron and Thermoelectric Effects," *Proc. of the 2001 International Semiconductor Device Research Symposium (ISDRS-01)*, Washington, DC, Dec. 2001, pp. 653–656.
10. **X. Zhou**, S. B. Chiah, K. Y. Lim, Y. Wang, X. Yu, S. Chwa, A. See, and L. Chan, "Technology-Dependent Modeling of Deep-Submicron MOSFET's and ULSI Circuits," (*Invited Paper*), *Proc. of the 6th International Conference on Solid-State and Integrated-Circuit Technology (ICSICT-2001)*, Shanghai, Oct. 2001, vol. 2, pp. 855–860.
11. **X. Zhou** and K. Y. Lim, "Experimental Determination of Electrical, Metallurgical, and Physical Gate Lengths of Submicron MOSFET's," *Proc. of the 4th International Conference on Modeling and Simulation of Microsystems (MSM2001)*, Hilton Head Island, SC, Mar. 2001, pp. 44–47.
12. S. B. Chiah, **X. Zhou**, K. Y. Lim, Y. Wang, A. See, and L. Chan, "Semi-Empirical Approach to Modeling Reverse Short-Channel Effect in Submicron MOSFET's," *Proc. of the 4th International Conference on Modeling and Simulation of Microsystems (MSM2001)*, Hilton Head Island, SC, Mar. 2001, pp. 486–489.
13. **X. Zhou** and K. Y. Lim, "A Novel Approach to Compact *I–V* Modeling for Deep-Submicron MOSFET's Technology Development with Process Correlation," *Proc. of the 3rd International Conference on Modeling and Simulation of Microsystems (MSM2000)*, San Diego, CA, Mar. 2000, pp. 333–336.
14. K. Y. Lim, **X. Zhou**, and Y. Wang, "Modeling of Threshold Voltage with Reverse Short Channel Effect," *Proc. of the 3rd International Conference on Modeling and Simulation of Microsystems (MSM2000)*, San Diego, CA, Mar. 2000, pp. 317–320.
15. W. Qian, **X. Zhou**, Y. Wang, and K. Y. Lim, "A Velocity-Overshoot Subthreshold Current Model for Deep-Submicrometer MOSFET Devices," *Proc. of the 3rd International Conference on Modeling and Simulation of Microsystems (MSM2000)*, San Diego, CA, Mar. 2000, pp. 396–399.
16. **X. Zhou** and K. Y. Lim, "A Compact MOSFET I_{ds} Model for Channel-Length Modulation Including Velocity Overshoot," *Proc. of the 1999 International Semiconductor Device Research Symposium (ISDRS-99)*, Charlottesville, VA, Dec. 1999, pp. 423–426.
17. K. Y. Lim, **X. Zhou**, and D. Lim, "A Predictive Length-Dependent Saturation Current Model Based on Accurate Threshold Voltage Modeling," *Proc. of the 2nd International Conference on Modeling and Simulation of Microsystems (MSM99)*, San Juan, Puerto Rico, Apr. 1999, pp. 423–426.
18. K. Y. Lim and **X. Zhou**, "Modelling of Threshold Voltage with Non-uniform Substrate Doping," *Proc. of the 1998 IEEE International Conference on Semiconductor Electronics (ICSE'98)*, Malaysia, Nov. 1998, pp. 27–31.
19. K. Y. Lim, **X. Zhou**, D. Lim, Y. Zu, H. M. Ho, K. Loiko, C. K. Lau, M. S. Tse, and S. C. Choo, "A Predictive Semi-Analytical Threshold Voltage Model for Deep-Submicrometer MOSFET's," *Proc. of the 1998 IEEE Hong Kong Electron Devices Meeting (HKEDM98)*, Hong Kong, Aug. 1998, pp. 114–117.

20. S. S. Rofail, K. S. Yeo, K. W. Chew, **X. Zhou**, and T. Tang, "An Experimentally-Based DC Model for the Bi-MOS Structure and Its Adaptation to a Circuit Simulation Environment," *Proc. of the IEEE Canadian Conference on Electrical and Computer Engineering (CCECE98)*, Waterloo, Canada, May 1998, vol. 1, pp. 37–40.
21. T. Tang and **X. Zhou**, "A Dynamic Timing Delay for Accurate Gate-Level Circuit Simulation," *Proc. of the 1996 Midwest Symposium on Circuits and Systems (MWSCAS-96)*, Ames, Iowa, Aug. 1996, pp. 325–327.
22. **X. Zhou**, S. Alexandrou, and T. Y. Hsiang, "Monte-Carlo Investigation of Subpicosecond Pulse Generation by Nonuniform Gap Illumination," *Proc. of the 1994 Conference on Lasers and Electro-Optics (CLEO'94)*, Anaheim, CA, May 1994, paper CThI20.

<u>*Regional Journal and Conference*</u>

1. Y. Wang, **X. Zhou**, K. Y. Lim, and S. B. Chiah, "Investigation of MOSFET Series Resistance by Numerical Simulation and Compact Modeling," *Proc. of the 9th International Symposium on Integrated Circuits, Devices & Systems (ISIC2001)*, Singapore, Sept. 2001, pp. 238–241.
2. **X. Zhou**, "Hetero-Material Gate Field-Effect Transistors (HMGFET's)," (*Invited Paper*), *Proc. of the Bluetooth Technology: Devices and Processes for a Wireless World*, Santa Clara, CA, Mar. 2001.
3. **X. Zhou**, "Mixed-Signal Multi-Level Circuit Simulation: An Implicit Mixed-Mode Solution," (*Invited Paper*), *Proc. of the National Seminar on VLSI: Systems, Design and Technology*, Indian Institute of Technology, Bombay, Dec. 2000, pp. 10–15.
4. W. Qian, **X. Zhou**, Y. Wang, and K. Y. Lim, "Surface-Potential-Based Model of Reverse Short Channel Effect in Submicrometer MOSFETs with Nonuniform Lateral Channel Doping," in *Design, Modeling, and Simulation in Microelectronics*, Bernard Courtois, Serge N. Demidenko, L. Y. Lau, Editors, *Proc. of SPIE*, vol. 4228, pp. 243–248, 2000. Presented at *the 2nd International Symposium on Microelectronics and Assembly (ISMA2000)*, Singapore, Nov. 2000.
5. Y. Wang, K. Y. Lim, W. Qian, and **X. Zhou**, "Investigation of Reverse Short Channel Effect with Numerical and Compact Models," in *Design, Modeling, and Simulation in Microelectronics*, Bernard Courtois, Serge N. Demidenko, L. Y. Lau, Editors, *Proc. of SPIE*, vol. 4228, pp. 366–373, 2000. Presented at *the 2nd International Symposium on Microelectronics and Assembly (ISMA2000)*, Singapore, Nov. 2000.
6. W. Qian, **X. Zhou**, R. Liu, and T. Wei, "Analytic Model for Currents in Si/SiGe HBT with Heavy-doping SiGe Base," *Proc. of the 8th International Symposium on IC Technology, Systems & Applications (ISIC-99)*, Singapore, Sept. 1999, pp. 407–410.
7. **X. Zhou**, "Process-Dependent MOS Threshold Voltage Formulation Based on 2-D Process and Device Simulations," *Proc. of the 7th International Symposium on IC Technology, Systems & Applications (ISIC-97)*, Singapore, Sept. 1997, pp. 235–238.
8. T. Tang and **X. Zhou**, "Accurate Timing Simulation of Mixed-Signal Circuits with a Dynamic Delay Model," *Proc. of the International Workshop on Computer-Aided Design, Test, and Evaluation for Dependability (CADTED)*, Beijing, July 1996, pp. 309–311.
9. **X. Zhou** and T. Tang, "Modelling and Simulation of GaAs High-Speed HEMT, HBT, and MESFET Analogue/Digital Circuits," *Proc. of the 7th MINDEF-NTU Joint R&D Seminar*, Nanyang Technological University, Singapore, Jan. 1996, pp. 77–83.

10. T. Tang, **X. Zhou**, and C. C. Jong, "Mixed-Mode Simulation of High-Speed HFET Logic Circuit," *Proc. of the 6th International Symposium on IC Technology, Systems & Applications (ISIC-95)*, Singapore, Sept. 1995, pp. 510–514.
11. **X. Zhou** and T. Tang, "Multi-Level Modelling of GaAs High-Speed Digital Circuits," *The EEE Journal*, School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore, vol. 7, no. 1, pp. 58–64, July 1995.
12. H. J. Lee, M. S. Tse, K. Radhakrishnan, K. Prasad, J. Weng, S. F. Yoon, **X. Zhou**, and H. S. Tan, "Selective Wet Etching of GaAs/AlGaAs Heterostructure with Citric Acid/Hydrogen Peroxide Solutions for Pseudomorphic GaAs/AlGaAs/InGaAs HFETs Fabrication," *J. Materials Sci. Eng. B: Solid-State Materials for Advanced Technology*, pp. 230–233, Dec. 1995; *Proc. of the 1st International Conference on Low Dimensional Structures & Devices (LDSD 95)*, Singapore, May 1995.
13. H. J. Lee, M. S. Tse, K. Radhakrishnan, K. Prasad, S. F. Yoon, J. Weng, **X. Zhou**, H. S. Tan, S. K. Ting, and Y. C. Leong, "Characterization of Ni/Ge/Au/Ni/Au Contact Metallization on AlGaAs/InGaAs Heterostructures for Pseudomorphic HFET Application," *J. Materials Sci. Eng. B: Solid-State Materials for Advanced Technology*, pp. 234–238, Dec. 1995; *Proc. of the 1st International Conference on Low Dimensional Structures & Devices (LDSD 95)*, Singapore, May 1995.
14. H. J. Lee, M. S. Tse, J. Weng, K. Prasad, K. Radhakrishnan, S. F. Yoon, **X. Zhou**, H. S. Tan, S. K. Ting, and Y. C. Leong, "Fabrication and Characterization of Pseudomorphic AlGaAs/InGaAs Heterostructure Field Effect Transistors (HFETs)," *Proc. of the 1st International Conference on Low Dimensional Structures & Devices (LDSD 95)*, Singapore, May 1995.
15. M. S. Tse, H. J. Lee, K. Prasad, K. Radhakrishnan, J. Weng, S. F. Yoon, **X. Zhou**, and H. S. Tan, "Characterization of Au/(Ge,Si)/Pd (Si,Ge) Ohmic Contact Metallization on AlGaAs/InGaAs Heterostructures for Pseudomorphic HFET Applications," *Proc. of the 1st International Conference on Low Dimensional Structures & Devices (LDSD 95)*, Singapore, May 1995.
16. **X. Zhou**, "Monte Carlo Calculation of Base Transit Times in Ballistic-Base vs. Graded-Base HBTs," *Proc. of the 5th International Symposium on IC Technology, Systems & Applications (ISIC-93)*, Singapore, Sept. 1993, pp. 717–721.
17. J. Weng, G. Ruan, and **X. Zhou**, "Impact of the Graded Heterojunction in the Base on the Performance of AlGaAs/GaAs HBTs," *Proc. of the 5th International Symposium on IC Technology, Systems & Applications (ISIC-93)*, Singapore, Sept. 1993, pp. 151–155.

INVITED TALKS AND WORKSHOPS

1. "Multi-Level Modeling of Deep-Submicron CMOS ULSI Systems," *Invited Talk (IEEE EDS Distinguished Lecturer Program)*, Institute of Microelectronics, Tsinghua University, Beijing, Dec. 13, 2002.
2. "Multi-Level Modeling of Deep-Submicron CMOS ULSI Systems," *Invited Talk (IEEE EDS Distinguished Lecturer Program)*, Microelectronics R&D Center, Chinese Academy of Sciences, Beijing, Dec. 13, 2002.
3. "Multi-Level Modeling of Deep-Submicron CMOS ULSI Systems," *1-Day Short Course*, organized by Center for Continuing Education, Nanyang Technological University, Sept. 2, 2002.

4. "MOSFET Compact *I–V* Modeling for Deep-Submicron Technology Development," *Invited Talk*, Swiss Federal Institute of Technology - Lausanne (EPFL), Lausanne, Switzerland, June 17, 2002.
5. "Mixed-Signal Multi-Level Circuit Simulation: An Implicit Mixed-Mode Solution," *Invited Talk*, Motorola, Geneva, Switzerland, June 17, 2002.
6. "MOSFET Compact *I–V* Modeling for Deep-Submicron Technology Development," *Invited Talk*, LSI Logic Corp., Santa Clara, CA, Apr. 18, 2002.
7. "MOSFET Compact *I–V* Modeling for Deep-Submicron Technology Development," *Invited Talk*, Intel Corp., Santa Clara, CA, Apr. 17, 2002.
8. "MOSFET Compact *I–V* Modeling for Deep-Submicron Technology Development," *Invited Talk*, Advanced Micro Devices, Inc., Sunnyvale, CA, Apr. 16, 2002.
9. "MOSFET Compact *I–V* Modeling for Deep-Submicron Technology Development," *Invited Talk* (*IEEE EDS Distinguished Lecturer Program*), Wuxi Microelectronics R&D Center, Wuxi, Oct. 24, 2001.
10. "MOSFET Compact *I–V* Modeling for Deep-Submicron Technology Development," *Invited Talk* (*IEEE EDS Distinguished Lecturer Program*), Fudan University, Shanghai, Oct. 18, 2001.
11. "MOSFET Compact *I–V* Modeling for Deep-Submicron Technology Development," *Invited Talk*, LSI Logic Corp., Santa Clara, CA, Mar. 26, 2001.
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28. "Compact Threshold Voltage Modeling for Deep-Submicron MOSFET's Based on Numerical Simulation, Empirical Formulation, and Experimental Correlation," *Invited Talk*, Texas Instruments, Inc., Dallas, TX, June 18, 1998.

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