An Adaptive Integration Time CMOS Image Sensor with Multiple Readout Channels for Star Trackers

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***Abstract*—In this work, we present an adaptive integration time CMOS image sensor with multiple readout channels for star tracker application. The sensor architecture allows each pixel to have an adaptive integration time. By cyclically selecting a row of pixels and checking the integration voltage of each pixel, brighter pixels can be "marked" and read out first. The dimmer pixels will continue integration until their voltage fall into a window defined by two threshold voltages. Each pixel only consists of five transistors. In order to improve the readout throughput and hence to reduce the rolling time, a multiple readout channel architecture is proposed. A proof-of-concept 320×128-pixel image sensor has been implemented using GlobalFoundries 0.18μm mixed-signal CMOS process.**

I. Introduction

Star trackers use a CMOS image sensor to measure the brightness of stars so as to determine the star location on the focal plane. Among various navigation sensors (magnetic, gyros and Sun sensors), star trackers are the most accurate with an angle accuracy in the range of arcseconds [1]. Star radiation is measured by its visual magnitude. A star with Apparent Magnitude M_V=1 is 2.5 times brighter than a magnitude M_V=2 star. Taking into account such factors as luminance spectral distribution, photodetectors' quantum efficiency (QE) and optical point spread function (PSF), we can estimate the number of photons received by the sensor[2]. An Apparent Magnitude M_V=6 star can only generate approximately 300 photons for 50ms exposure time. This is a very challenging number for CMOS image sensor, and in particular, under space radiation environment. Moreover, a typical star tracker camera requires a sensitivity of capture multiple apparent magnitudes ($0<M_V<6$) in the field of view (FOV). Therefore, dim stars need long exposure time in order to receive enough photons; at the same time, bright stars are supposed to have short exposure time to avoid saturation. To handle the wide-dynamic-range star light intensity, it is advantageous to allow "stars" to have adaptive integration time. To incorporate the dimension of time, the scheme of adaptive integration time, often referred as "saturation detection", measures the time it takes the photocurrent to produce a given voltage change at the sense node. The light intensity is then represented by the time domain (PWM) encoding [3] or frequency domain (PFM) encoding [4].

We propose a new architecture for the CMOS image sensor in which each pixel features an adaptive integration time. The adaptive integration time is achieved by cyclically checking the integration voltage of pixels in a row-wise manner during the exposure. In this case, brighter pixels can be "marked" and read out first. In order to improve the readout throughput, a scheme of multiple readout channel is proposed. The rest of the paper is organized as follows: Section II introduces the architecture, operation principle and circuit design. Section III describes the sensor implementation and Section IV discusses the measurements results. Conclusion is given in Section V.

II. Sensor Architecture

The architecture of the proposed image sensor is shown in Fig.1. It includes a 320×128 pixel array, column-parallel comparison circuits, multiple(three) readout channels, a row scanner, a channel assignment controller and a global timer. The pixel array is globally reset by $GRST$. As can be seen from Fig.1(a), each pixel consists of five NMOS transistors. $M1-M3$ forms a typical Active Pixel Sensor (APS). Two extra transistors $M4-M5$ form a pull-down path for the photodiode. As such, the photodiode can be pulled down to its saturation level by external control signal. The column-parallel comparison circuits communicate with the pixel through two vertical buses, $COL(j)$ and $PDN(j)$. They are composed of a Sample-and-Hold (SH) circuit block, comparison circuits (Fig.1(b)) and a group of channel select switches. In each readout channel, the scan register can be configured to bypass a certain column depending on the comparison result. The channel selection logic decides which channel can be used to read out a selected row.

A. Operation Principle

The proposed architecture features column-parallel comparison circuits to decide whether a pixel should stop its integration or not. Fig.2 illustrates the operation principle with an example of a 3×3 pixel array. Initially, the sensor is globally reset and all the pixels start integration. Immediately followed by the reset operation, a row-wise scanner starts rolling. At $T0$, $Row0$ is selected and all the pixels in $Row0$ are simultaneously sampled onto the column-parallel comparison circuits. In this example and at this moment, no pixel has gathered enough photons and therefore none of the pixel's voltage falls into the threshold window. Next at time $T1$, $Row1$ is sampled and checked in the same manner. There are two bright pixels ($Col1$, $Col2$) whose voltages are within the thresholds. This will enable the readout process and the whole $Row1$ is assigned to a readout channel. In the meanwhile, the

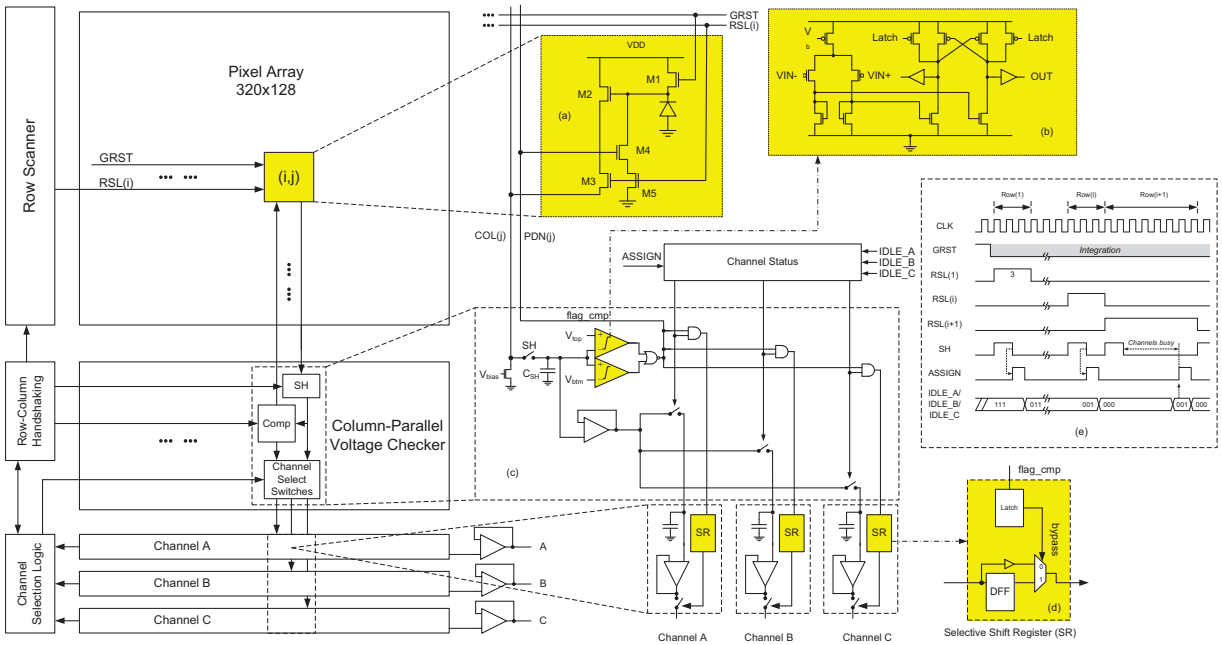

Fig. 1. Sensor architecture. Main building blocks include a pixel array, column-parallel comparison circuits, three readout channels, row scanner and channel assignment controller.

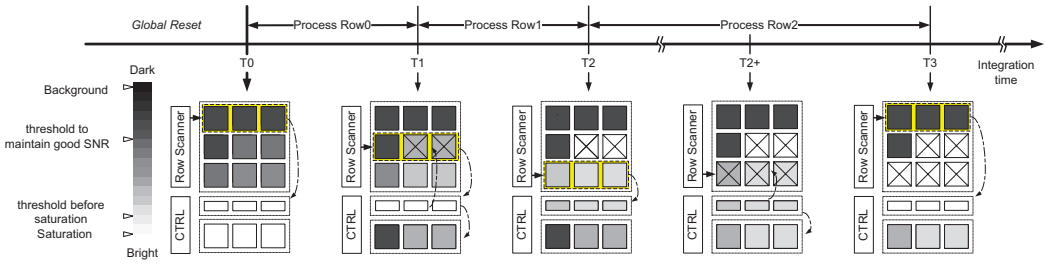

Fig. 2. Operation principle of the adaptive-integration-time readout scheme.

column circuits will raise a flag signal to "mark-off" the two bright pixels. In this way, these two pixels will be ignored in the future checking process. The readout channel takes two clock cycles to readout the active pixels in $Row1$. Instead of waiting for the completion of readout, the sensor continues to check $Row2$ immediately after channel assignment (proceed to next row immediately after $Assign$ pulse in Fig.1(e)). A pipeline mechanism has been proposed so that the voltage checking and readout can work in parallel. In the case that all readout channels are occupied, at time $T3$ for example, the row-wise scanner will pause until at least one channel becomes free. For a particular row, the readout time is proportional to the number of "active" pixels. This is implemented by a scanner with bypass control. When the row scanner hits the last row, it will loop back to the first row to scan another round.

B. Readout Channel Assignment

The sampled pixel voltage on capacitor C_{SH} is compared to two threshold voltages namely V_{top} and V_{bottom}, respectively. The comparison result is fed back to the array and the pixel is "marked-off" by pulling down the diode voltage using transistor $M4$. At the same time, the result is stored in a latch and further used as a bypass control for the column-wise scanner. The shift register at a specific column is therefore skipped when $flag_{cmp} = 0$ and hence a row with less "active" pixels will take shorter readout time. Besides, our architecture builds three readout channels managed by a channel selection logic. Each channel has a flag register indicating the status of "BUSY" or "IDLE". The assignment logic uses a simple priority rule to decide the channel assignment. Channel A has the highest priority and Channel C will be used only when both Channel A and B are unavailable. Once a channel is identified as "IDLE", the assignment switches will be turned on and the analog voltage will be transferred from capacitor C_{SH} to the corresponding local sample-and-hold capacitor in the channel.

C. Image Reconstruction

With this scheme, pixels with different illumination level will have their own integration time as illustrated in Fig.3. $PixelA$ experiences a sharper discharge slope due to a larger photocurrent. $PixelB$ shows a moderate photocurrent while $PixelC$ is apparently under dark condition. We can set a maximum integration time and $PixelC$ that fail to reach the readout window will be treated as dark pixels. The sensor outputs both analog voltage (V_s) and the time (t_s) when the voltage is sampled, which is used to reconstruct a picture:

$$I_{ph} = \frac{C_{\text{int}}\,(V_{rst} - V_s)}{t_s} \tag{1}$$

where I_{ph} is the pixel's photocurrent and C_{int} is the photodiode capacitor. The scheme allows each pixel to be autonomously adapted to its own integration time, so that the dynamic range (DR) in both the voltage and time domain encoding is given by:

$$DR = 20\log\frac{I_{\max}}{I_{\min}} = 20\log\frac{C_{\text{int}}\,(V_{rst} - V_{btm})/T_{\min}}{C_{\text{int}}\,(V_{rst} - V_{top})/T_{\max}} \tag{2}$$

where V_{btm} is the bottom threshold and V_{top} is the top threshold, respectively. $T_{\max}$ is the maximum integration time mentioned above. $T_{\min}$ is the minimum integration time during first-round voltage checking. $T_{\min}$ depends on the pixel position and dynamics of the image scene. Therefore, $T_{\min}$ can be regarded as the waiting time for a pixel to be processed in the first-round scanning. For pixels in the first row, $T_{\min}$ is 150ns at 10MHz(one and half cycle as shown in Fig. 1(e)). If $T_{\max}$ of 200ms is considered and assuming V_{rst}, V_{btm} and V_{top} are 0.9V, 0.2V and 0.6V respectively, a 130dB DR is expected.

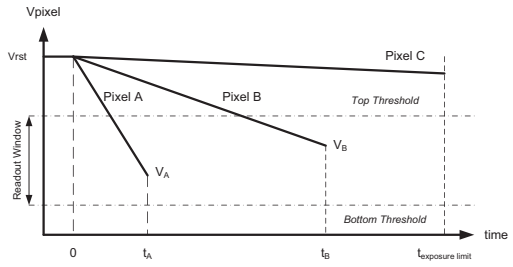

Fig. 3. Illustration of different pixel's response. Pixels with different illumination level will have their own integration time.

III. Sensor Implementation

The proposed image sensor has been fabricated in Global Foundries 0.18μm 1P6M CMOS technology. Fig. 4 shows the chip microphotograph where the main building blocks are highlighted. The overall chip dimension is 2.5 $\times$ 2.5 mm^2. The array contains 320 $\times$ 128 pixels. Each pixel features a footprint of 5$\times$5μm^2 with a fill-factor of 38%. The sensor has three readout channels. Each channel outputs signal pairs consisting analog signal, time and column address. An Opal-Kelly XEM 3010 Opal Kelly FPGA board is used to provide control signals and references including top and bottom thresholds.

TABLE I
Performance Summary of the Sensor

Technology	Global Foundry 0.18μm mixed-signal CMOS
Clock Frequency	10MHz
Power Consumption	247mW with 1.8V power supply
Pixel Array Size	320(H) $\times$ 128(V)
Photodetector Type	N+/P-sub photodiode
Pixel size	5μm $\times$ 5μm with 38% fill factor
Signal Swing	180mV - 950mV
Temporal Noise	148e-
Sensitivity	0.25V/lux·s
FPN	1.6%

The row address is also generated on the FPGA board. The acquired data are transferred to PC for post-processing and image reconstruction. During sensor characterization, we have observed that the chosen process shows poor light responsivity. The average dark current is measured at 1537fA for a N+/P-sub photodiode with an area of 4.26μm $\times$ 2.28μm. The sensor consumes 247mW power at 10MHz clock frequency. The sensor parameters and characterization details are listed in Table I.

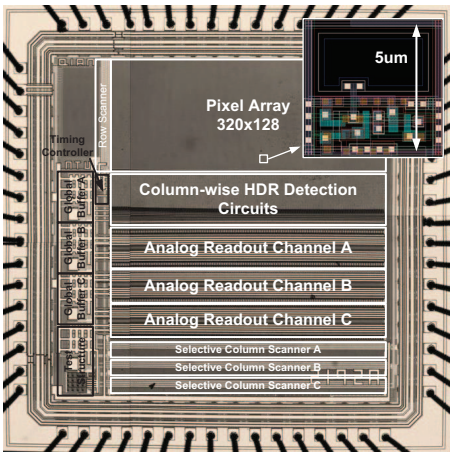

Fig. 4. Chip microphotograph.

IV. Measurement Results

The sensor is used to image the scene of star field where the star objects (bright pixels) in the scene are of primary concern. In order to simulate the star field imaging, we let a light source about 10klux back-illuminate through a star pattern mask in a dark room. The star pattern is made of a PCB stencil with precise position control of the "stars". The captured raw sample images are shown in Fig. 5 without any post-processing or compensation. We have swept the bottom threshold from 250mV to 450mV for three different top thresholds. The photocurrent of each pixel is extrapolated using Eq. 1. The unread pixels are shown as dark pixels. The analog outputs of the sensor are first converted to 12-b digital values by external Analog-to-Digital Converter (ADC). Then, they are further compressed to 8-bit grayscale values to display on the monitor.

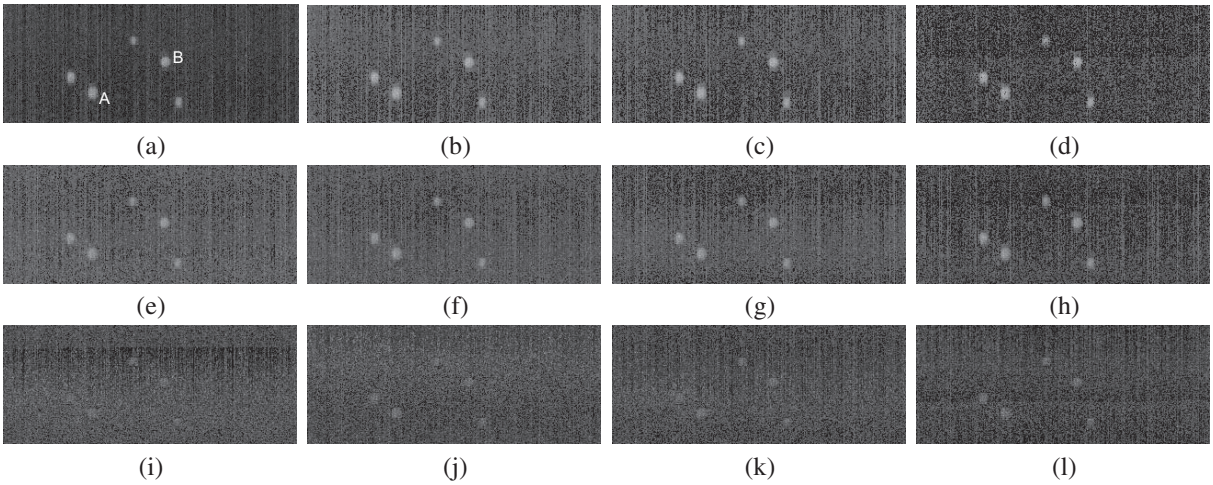

Fig. 5. Raw sample images for simulated star-pattern measurement under different parameter settings. Images in the first row (a)-(d), top threshold is set to 500mV and bottom threshold are 250mV, 300mV, 350mV and 450mV, respectively. In (e)-(h), top threshold is changed to 600mV and in (i)-(l), top threshold is set to 700mV. Two "stars", marked as A and B, are selected for centroiding evaluation.

Both top threshold and bottom threshold play an important role in readout pixel numbers. Fig. 6 shows the corresponding readout percentage with different size of the readout window. Readout percentage reduces with the shrinking of the readout window. Most of the missing readouts are located in the dark background because they are regarded as dark pixels like $PixelC$ in Fig. 3. The sparse "stars" are completely captured except when the readout window decreases down to 50mV as shown in Fig. 5(c). Missing readouts appear undesirably inside "stars" due to these pixels falling out of the readout window.

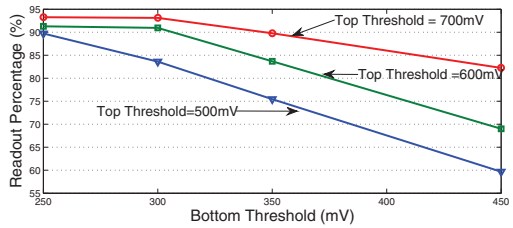

Fig. 6. Readout percentage of the simulated star-pattern images.

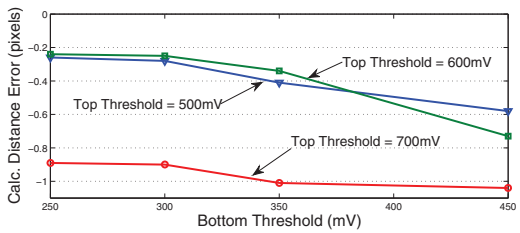

Fig. 7. Calculated distance error with different top threshold voltage.

Moreover, we have implemented star centroiding [2] algorithm (Center of Mass) to calculate the centroid position to assess the measurement accuracy. As shown in Fig. 5(a), two "stars", A(63, 97) and B(96, 176), and their distance (85.62 pixels) are used. Top threshold has demonstrated critical in measurement accuracy as shown in Fig. 7. The absolute calculated error of more than 0.9 pixels is observed when the top threshold is 700mV. In fact, if we further increase the top threshold, the "stars" can be hardly captured and mixed with the background. The raised top threshold will trigger "bright" pixels to be read out earlier with lower number of received photons. The reduced signal magnitude results in degraded Signal-to-Noise Ratio (SNR) for "star" pixels, thus affecting the centroding accuracy. In addition, if there are missing readouts inside "stars"(Fig. 5(d)), it obviously causes the centroid to shift due to dark pixels in the "stars".

V. Conclusion

We have introduced a novel CMOS image sensor architecture for star tracker application. The pixel is allowed to have adaptive integration time while maintaining compact footprint and high fill factor, which is suitable for high-resolution integration. A proof-of-concept chip has been fabricated and measured. Our experimental results show the architecture is potential for star tracker applications where "objects" are sparsely distributed. Two voltage thresholds defining the readout window have shown critical influence in terms of readout rate as well as measurement accuracy.

VI. Acknowledgement

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References

[1] M. Pham, K.-S. Low, and S. Chen, "An Autonomous Star Recognition Algorithm with Optimized Database," *Aerospace and Electronic Systems, IEEE Transactions on*, vol. 49, no. 3, pp. 1467–1475, 2013.

[2] C. Liebe, "Accuracy Performance of Star Trackers - A Tutorial," *IEEE Transactions on Aerospace and Electronic Systems*, vol. 38, no. 2, pp. 587 –599, apr 2002.

[3] C. Posch, D. Matolin, and R. Wohlgenannt, "A QVGA 143 dB Dynamic Range Frame-Free PWM Image Sensor With Lossless Pixel-Level Video Compression and Time-Domain CDS," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 1, pp. 259 –275, jan. 2011.

[4] C. Shoushun, F. Boussaid, and A. Bermak, "Robust Intermediate Read-Out for Deep Submicron Technology CMOS Image Sensors," *IEEE Sensors Journal*, vol. 8, no. 3, pp. 286 –294, march 2008.