

# A Time-Delay-Integration CMOS Image Sensor with Pipelined Charge Transfer Architecture

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**Abstract**—In this paper, we report a novel Time-Delay-Integration (TDI) CMOS image sensor for low-earth orbit (LEO) nano-satellite imaging application, where limited exposure time and unexpected flight fluctuations are major design challenges. The sensor features programmable integration time per stage, dynamic charge transfer path and tunable well capacity. A prototype chip of  $1536 \times 8$  pixels was implemented using TSMC  $0.18\mu\text{m}$  CMOS image sensor process. Photodiode and other transistors are floor-planned in different arrays, providing small pixel pitch of  $3.25\mu\text{m}$  and high fill factor of 57%.

## I. INTRODUCTION

There is an increasing use of satellites for meteorological, oceanographic and other scientific applications[1]. Many satellites are equipped with multi-spectral remote sensing system that can operate in multiple bands and measure radiations in a series of discrete spectral bands. Usually this is implemented by closely assembling multiple types of sensor and sharing one optical system. On the focal plane, each type of sensor is based upon the concept of push broom scanner, as shown in Fig. 1. There is a ruler of detectors oriented crosswise to the direction of flight. The image is produced in direction of flight as the result of movement of the satellite. The produced image generally includes several kinds of geometric distortions due to both static errors caused by pixel mismatch and misalignment of the multi-band sensors and dynamic errors caused by changes of orientation angles, the orbit perturbations or attitude fluctuation. In addition, due to fast orbital speed, each ground resolution cell has limited exposure time. Taking Low Earth Orbit (LEO) satellite as example, with height of 700km, focal length of 25cm, and pixel pitch of  $5\mu\text{m}$ , the sensor is only allowed to have a maximum integration time around 2ms. This consequently results in unacceptably low Signal to Noise Ratio (SNR) at twilight light condition and thus limits the practical usage of the satellite imaging system. To address the problem, TDI scheme has been widely used for imaging high speed motion objects or still objects with the sensor in motion[2]. The charge accumulated in each pixel does not directly output after the first exposure time, but shifted to the second row of pixel at the same column, and are added to the charge pockets of second pixel. The output charge is thus summed over the number of TDI rows available. Thanks to the high charge-transfer efficiency, TDI principle has typically been implemented in CCD sensors.

In TDI, the signal charge must be transferred in the same direction and at the same speed as those of the objects

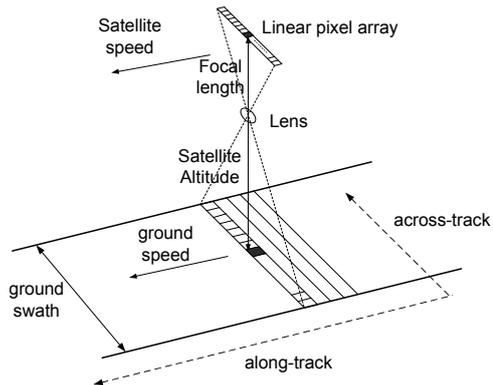


Fig. 1. Line Scanner System.

to be imaged. Due to limited charge transfer modes, the successful operation of most TDI-CCDs only works with the assumption that the flight direction is perfectly crosswise to the row of pixels. Unfortunately, this is not realistic in practice due to either orbital perturbations and dynamic satellite altitude control. Moreover, CCD technology suffers from several weaknesses, such as a high power consumption and CMOS incompatibility. A number of CMOS solutions have been developed[2][3][4]. In this paper, we propose a new TDI CMOS image sensor for Low Earth Orbit (LEO) satellite imaging. Firstly, the number of transfer stages is optimized for SNR performance. Increasing the number of stages allows longer exposure time (thus favoring low light pixels), however, this comes at the expense of more readout noise. Secondly, a well capacity adjustment scheme is used to adapt to different space illumination condition, which varies over 7 orders of magnitude according to orbit position around the earth. The sensor consists of 8 rows of transfer stages with a horizontal resolution of 1536 pixels. The rest of the paper is organized as follows. Section II describes the sensor architecture. Section III discusses the system analysis. Section IV describes the VLSI implementation and Section V concludes this paper.

## II. SENSOR ARCHITECTURE

The block diagram of the proposed image sensor is shown in Fig. 2. The sensor consists of a pixel array of  $1536 \times 8$  pixels. The 1536 columns define the spatial resolution of the image and all the pixels in each column comprise a chain of 8 transfer stages, *Row0*–*Row7*. The row shift registers transfer the intermediate integration charge to the next stage at a fixed

time interval, i.e., the time for the satellite traveling one ground resolution pixel. There is a switch network between stages, enabling various transfer paths. The final integration results presented at the end of the integration chain are sequentially accessed by the column scanner. The selected column is then readout by a global output buffer, which is a two-stage operational transconductance amplifier (OTA) to drive the analog pad.

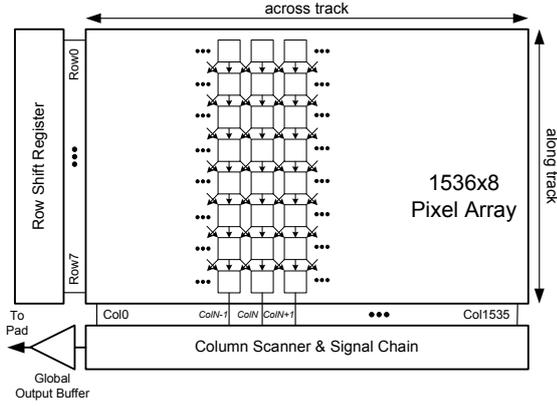


Fig. 2. Sensor's block diagram.

#### A. Signal Path from Pixel to Global Buffer

The signal path from the pixel to the global output buffer is shown in Fig. 3. The first stage (*Row0*) pixel consists of a reset transistor ( $RST0$ ), mode switches ( $Ax$ ,  $Bx$  and  $Cx$ ), a photodiode with configurable integration capacitors and a unity gain buffer. PMOS transistor is used to reset the photodiode voltage to  $VDD$ , enabling higher photodiode voltage swing (than NMOS reset transistor). In the rest stages (*Row1* – *Row7*), each pixel contains a photodiode, a reset switch ( $RSTx$ ), mode switches, a sample and hold capacitor ( $C_{memx}$ ) and a unity gain buffer. Between stages, three switches allows the pixel ( $ColN$ ) to transfer the intermediate photo signal either to its direct next stage pixel via switch  $D_D$ , or its left neighbor ( $ColN - 1$ ) via switch  $D_L$ , or the right one ( $ColN + 1$ ) through switch  $D_R$ , respectively. In case of strong illumination condition, there is no need for extended integration time and hence the integration stages should be programmable. By-passing a stage can be implemented using mode switches. In each stage, the unity gain buffer is enabled only during the short period of charge transfer for power saving.

#### B. TDI Operation

The TDI operation follows a sequence of “Sample-Hold, Reset (*Row0*)/ Transfer (*Row1* – *Row7*)” and “Integration/By-passing”.

1) *Sample-Hold, Reset/Transfer*: At the end of each time interval when satellite travels one ground resolution cell, TDI stages perform a “Sample-Hold, Reset/Transfer” operation. In each stage, the intermediate integration signal will be temporarily sample-and-hold by an analog memory ( $C_{memx}$ ).

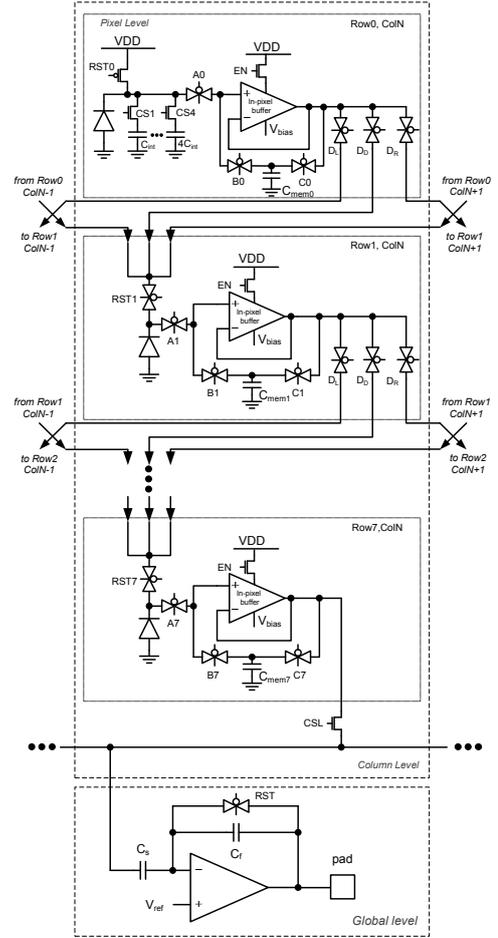


Fig. 3. A signal path from pixel to global buffer in a column.

This is done by turning *ON* switches  $Ax$  and  $Cx$ . After that, switches  $Ax$  and  $Cx$  are *OFF* while  $Bx$  is turned *ON*. This will transfer the photo signal from  $C_{memx}$ , to its next stage photodiode. Apparently, in first stage, pixels are transferred to an initial  $VDD$  voltage. The operation sequence and corresponding circuit configuration is illustrated by Fig. 4 (a) and (b), respectively.

2) *Integration/By-passing*: When a stage is used for integration time extension, switch  $RSTx$  is turned *OFF*,  $Ax$ ,  $Bx$  and  $Cx$  are *OFF*. When a stage is selected for by-passing, switches  $RSTx$  and  $Ax$  are kept *ON*,  $Bx$  and  $Cx$  are *OFF*. That stage will simply act as a direct path formed by a unity gain buffer. The switch configuration is shown in Fig.4 (c).

#### C. Dynamic Transfer Modes

An external image processor will determine the illumination level and the direction of the satellite motion for the whole image. The switches in the TDI stages can therefore be controlled to implement different charge transfer modes. A few scenarios are simulated and shown in Fig. 5. In the first example, all stages are used to extend the integration time and the partial integration charges are summed stages by stages

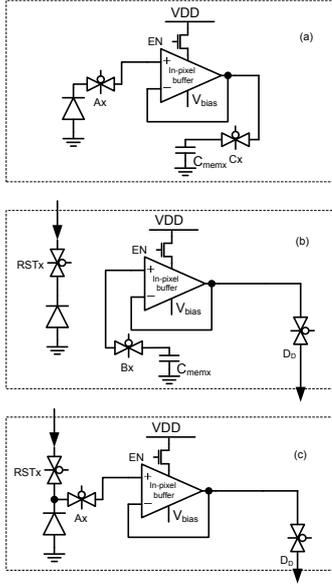


Fig. 4. Three pixel configurations for TDI operation in a single pixel stage. (a) Sample-Hold configuration, (b) Reset/Transfer configuration and (c) Bypassing configuration.

until it reaches last row. In Fig. 5 (b), some stages are bypassed to adapt the sensor for strong illumination condition to avoid saturation. At extreme bright condition, only the first stage integrates with additional integration capacitors and all the other stages are by-passed. Thirdly, direction control switches allow dynamic transfer paths, as shown in Fig. 5 (c). The path can be real-time updated during the integration according to the result of on-board image processing. This will effectively address the image smear caused by flight fluctuations.

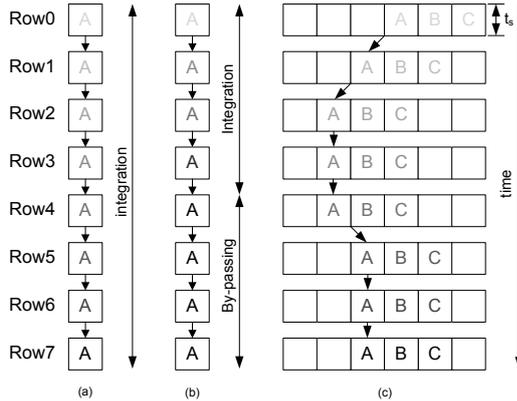


Fig. 5. TDI operation scenarios: (a) straight integration (b) integration and bypass stages (c) integration with direction control.

### III. ANALYSIS AND DISCUSSION

In this section, we conduct system level analysis and present simulation results.

Two important figures for integration mode images sensor, dynamic range (DR) and signal-to-noise ratio (SNR), are

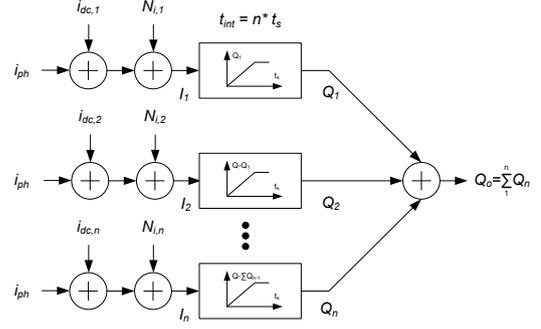


Fig. 6. TDI sensor model with input referred noise.

investigated. We extend a sensor model in [5] to suit our TDI architecture, intending to analytically relate the sensor response with the photocurrent signal, dark current signal, and the noise for sensors output in the integration mode as well as integration stages. The sensor model is illustrated in Fig. 6. There are  $n$  pixel stages in the model. The integration time in each stage is  $t_s$  so the total integration time is  $n \cdot t_s$ . If we assume that the integration does not saturate through the TDI, the partial accumulated charge  $Q_n$  in stage  $n$  are added together to form the final the output charge  $Q_o$ . The photocurrent and the dark current in stage  $n$  are  $i_{ph}$  and  $i_{dc,n}$ , respectively. Here we assume the photocurrent is constant for all integration stages.  $N_{i,n}$  denotes the equivalent zero-mean input referred noise introduced in each stage and the average power of which is given by

$$\sigma_{N_{i,n}}^2 = \frac{q(i_{ph} + i_{dc,n})t_s + \sigma_{r,n}^2}{t_s^2} \quad (1)$$

where  $q(i_{ph} + i_{dc,n})t_s$  is the output referred noise due to the shot noise and  $\sigma_{r,n}^2$  is the variance of the noise charge caused by the readout circuit in the pixel, including reset noise of the photodiode, offset noise in the in-pixel amplifier as well as fixed pattern-noise (FPN) between stages.

The corresponding DR and SNR in single stage  $n$  can be expressed as

$$DR_n = 20 \log \left( \frac{q_{max} - i_{dc,n}t_s}{\sqrt{q i_{dc,n}t_s + \sigma_{r,n}^2}} \right) \quad (2)$$

$$SNR_n = 20 \log \left( \frac{i_{ph}t_s}{\sqrt{q(i_{ph} + i_{dc,n})t_s + \sigma_{r,n}^2}} \right) \quad (3)$$

where  $q_{max}$  is the full well capacity. We expect to find out the relation of both DR and SNR regarding the stage depth. With the assumption that the dark current  $i_{dc,n}$  is constant for all the stages, equal to  $i_{dc}$ , the corresponding DR and SNR as functions of number of stages are given by

$$DR(n) = 20 \log \left( \frac{q_{\max} - i_{dc} n t_s}{\sqrt{q i_{dc} n t_s + \sum_1^n \sigma_{r,n}^2}} \right) \quad (4)$$

$$SNR(n) = 20 \log \left( \frac{i_{ph} n t_s}{\sqrt{q(i_{ph} + i_{dc}) n t_s + \sum_1^n \sigma_{r,n}^2}} \right) \quad (5)$$

The noises due to readout circuits,  $\sigma_{r,n}^2$ , introduced in all stages are uncorrelated and are assumed to have the same variance,  $\sigma_r^2$ . Then the above equations can be simplified as

$$DR(n) = 20 \log \left( \frac{q_{\max} - n \cdot i_{dc} t_s}{\sqrt{n} \cdot \sqrt{q i_{dc} t_s + \sigma_r^2}} \right) \quad (6)$$

$$SNR(n) = 20 \log \left( \frac{\sqrt{n} \cdot (i_{ph} t_s)}{\sqrt{q(i_{ph} + i_{dc}) t_s + \sigma_r^2}} \right) \quad (7)$$

We evaluate the sensor model and these two performance figures with a sensor example. The relevant sensor parameters are chosen as  $q_{\max} = 125000e^-$ ,  $Nr = 20e^-$ ,  $i_{ph} = 1pA$ ,  $i_{dc} = 1fA$  and  $t_{int} = 1ms$  [5]. The simulation results are shown in Fig. 7. DR drops with the number of stages, which introduce more input referred noises and dark current, adding to noise floor and thus the minimum detectable photocurrent. On the other hand, SNR increases with the square root of the number of stages, thanks to the fact that signal increases more quickly than the input referred noises with integration time.

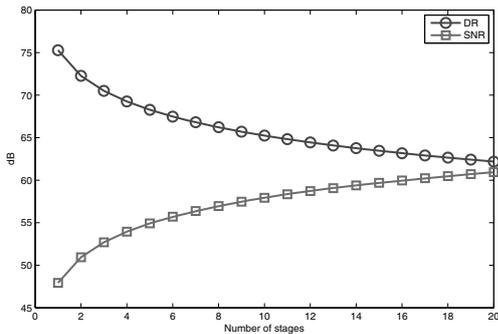


Fig. 7. Simulated DR and SNR with regard to stage number based on the TDI sensor model.

#### IV. SENSOR IMPLEMENTATION

A prototype chip of  $1536 \times 8$  pixels was implemented using TSMC  $0.18\mu m$  CMOS image sensor process (two-poly, six-metal layers). In order to achieve higher ground resolution, efforts were made to optimize the layout. Fig.8 (a) shows the layout of the chip. A portion of the pixel array is highlighted in Fig.8 (b). Photodiode and other transistors are floor-planned in

different arrays. The top off-array pixel circuits are dedicated to the first four stages and the bottom for the last four. Fig.8 (c) highlights a single column of the photodiodes, with each occupying  $3.25\mu m \times 3.25\mu m$ . In order to further reduce signal routing area, at each column and each side the 4 photodiodes communicate its pixel circuits via *M2-M5*, respectively. *M6* layer is used to transfer the 4th row pixel to the 5th row. This physical implementation strategy allows to minimize the pixel pitch ( $3.25\mu m$ ) and maximizes the fill factor (57%).

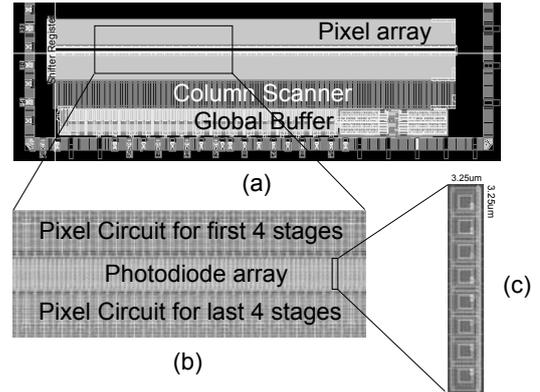


Fig. 8. Layout of the proposed TDI image sensor. (a) Layout of the image sensor, (b) layout of part of the pixel array and (c) layout of the photodiode in a single column.

#### V. CONCLUSION

We proposed a novel TDI CMOS image sensor for space imaging applications. The architecture features a highly programmable pipelined charge transfer, to deal with the variance in space illumination and the orbit perturbations or attitude fluctuation. The operational concept of the image sensor is explained in detail. The physical optimization of the pixel array has granted the effective pixel pitch to be as small as  $3.25\mu m$ . Limited by the length, the paper did not elaborate other design consideration such as space radiation and temperature variance.

#### VI. ACKNOWLEDGEMENTS

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