Design of a Radiation Tolerant CMOS Image Sensor

Xinyuan Qian[1], Hang Yu[1], Bo Zhao[1], Shoushun Chen[1] and Kay Soon Low[2]
[1]VIRTUS IC Design Center of Excellence, [2]Satellite Research Center,
School of Electric and Electronic Engineering,
Nanyang Technological University, Singapore

***Abstract*—This paper presents the design of a radiation tolerant CMOS image sensor for space applications. The pixel is based on a commercially available 4T pinned photodiode architecture and is designed using a number of radiation-tolerant physical layout techniques. In addition, a simple yet robust programmable column biasing current is proposed to deal with the dramatic temperature fluctuations. A prototype chip consisting 256×256 pixel array has been implemented using TSMC 0.18 CIS process.**

I. Introduction

CMOS image sensors (CIS) have overwhelmed their CCD counterparts in many applications for their predominant advantages of providing low power consumption at low voltage operation, high integration capability for SoC design, cost effective solution from its standardized fabrication process [1][2][3]. However, for space applications, the CIS has to be tolerant to space radiation and dramatic temperature fluctuation. Extensive reviews of radiation damage to microelectronic devices were well documented in the literature [4][5]. The impact of radiation has historically been categorized into two groups: one reflects the effects over a long period of time, termed as Total Ionizing Dose (TID) and the other is the immediate result of a single radiant charged particle, known as single event effects (SEE). The TID effects are cumulative, in which the absorption of radiation energy makes permanent changes in the device. All forms of radiation are capable of generating cumulative effects and the impact on device performance is determined by the integrated history of radiation exposure. The three major and consequential effects of total ionizing radiation on standard CMOS devices are shift of threshold voltages, leakage current in NMOS transistors, and n-channel inter-transistor (isolation field) leakage current.

In addition to sharing the various radiation-induced undesirable characteristics with other semiconductor devices, image sensors are inherently susceptible to pixel leakage current. Threshold shifts may result in an inversion region connecting n-channel sources and drains along the gate oxide to field oxide transition. This produces leakage current that can be very serious in the charge sensitive applications found in image sensors. Secondly, leakage current arises from the increased surface generation/recombination rate due to the formation of interface states. These are energy levels within the bandgap of the silicon, located at the silicon-oxide interface, so that they can communicate with the carriers in the silicon. Wherever interface states are in a depletion region, they result in electron-hole pair generation, leading to dark current and leakage. The pinned 4T APS structure (Fig.1) is now widely used because of its capability of minimizing dark current generated by interface defects in photodiode region. Extensive efforts have been made to analyze and understand the radiation effects on 4T APS [6][7][8][9][10]. These studies have outlined suggestive guidelines for designing radiation tolerant CIS based on 4T pixel architecture in deep submicron technology.

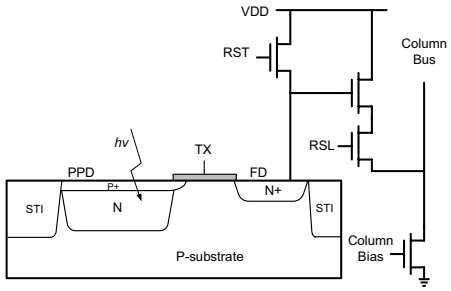

Fig. 1. Schematic and cross-sectional view of a typical 4T pixel architecture.

In this paper, we introduce the design of a CMOS Image sensor for space application. In order to achieve high stability, a variety of radiation-harden-by-design techniques are employed. Four pixel arrays with different configurations were fabricated. Due to page length constraint, we focus on one architecture and discuss the radiation-tolerant design considerations, namely: critical transistors in the pixel use enclosed layout transistor (ELT) and P+ guard ring; the N implant for the pinned photodiode is spaced from the STI; floating diffusion was carefully sized to deal with leakage current. In addition, we proposed a simple yet robust programmable column biasing current to deal with the dramatic temperature fluctuation. This paper is organized as follows. Section II discusses the pixel design and operation principle. Section III describes the VLSI implementation. Section IV concludes this paper.

II. Sensor Architecture

The schematic and cross-sectional view of a typical 4T pixel architecture is shown in Fig.1. It has four NMOS transistors: transfer gate (TX), reset transistor (RST), source follower (SF) and row select (RSL) and a pinned photodiode (PPD), in which a thin P+ pinning layer is utilized on the top of the photodiode

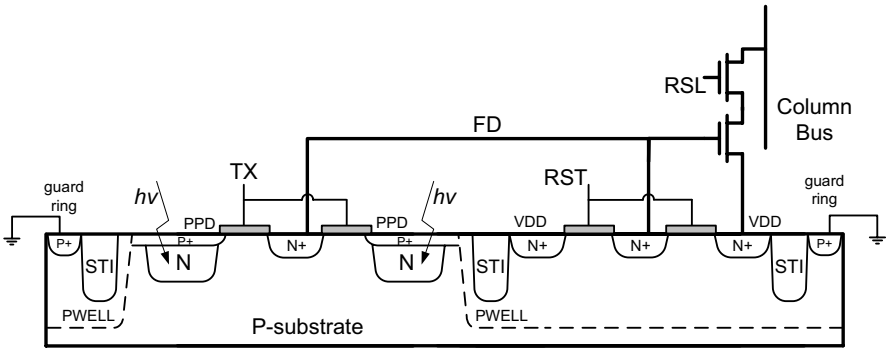

Fig. 2. Proposed radiation tolerant pixel architecture with its highlighted cross sectional view of the pinned photodiode and floating diffusion node.

to shield it from the Si-SiO2 surface defects and suppress the noise charges. The floating diffusion (FD) node is where the integrated charges in the PPD are transferred via TX and converted to the voltage signal. This is followed by a unity gain buffer (SF) and the voltage signal is conveyed to the output bus when the row is selected for readout.

The proposed radiation tolerant pixel architecture is illustrated in Fig.2. It has the same schematic as the typical 4T pixel architecture. However, extra design efforts are made to deal with dark current: critical transistors in the pixel are designed using enclosed layout transistor (ELT) and P+ guard ring; the N implant for the pinned photodiode is spaced from the STI in order to prevent the photodiode junction from interaction with the defective sidewalls and edge; floating diffusion is carefully sized to deal with leakage current. These approaches primarily highlights charge-sensitive regions of the PPD and FD node in the pixel and are explained in detail in the following sections.

A. Design of the Pinned Photodiode

The PPD is very susceptible to the ionizing radiation where the increased leakage current contributes to destroy the collected charges, and accordingly falsify the real signal. During the integration time, the PPD is open-circuited by the TX. It senses the incident light and accumulates the generated charges in the boundary of the depletion region. Fig.3 shows the cross-sectional view of the PPD in the proposed design. The photo collection region is composed of the N-implant/P-substrate junction. The pinning P+ layer has a much higher doping than the N implant so the depletion region extends only slightly into the pinning P+ layer. This efficiently isolate the photodiode from the surface defects. However, it has been found that another significant source of leakage stems from the defective sidewalls and the edges of shallow trench isolations (STIs) separating the photodiodes [11]. Protecting the STIs by P-Well structures has been proven to be effective against this type of leakage [8]. More spacing between the N-implant to STI results in higher immunity to radiation degradation, but trade off should be taken to balance the sensitivity and saturation level of the sensor (fill factor).

As shown in Fig.3, P-Well structure is used to protect

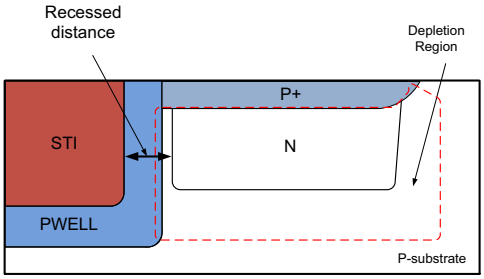

Fig. 3. Highlighted Cross-Sectional View of a Pinned Photodiode.

the PPD from STI and the space between the two was set to 0.2μm. Since the doping density of the P-Well is higher than the intrinsic P-substrate, the extension of the depletion region of the photodiode peripheral junction into the P-Well is curtailed and short compared to the intrinsic P-substrate, which additionally pushes the depletion region of the photodiode away from the STI sidewalls. It is worth to mention that the recessed STI, in fact, is realized by reducing the geometric size of the N implant of the PPD from the STI.

B. Design of the Floating Diffusion

One major effect of ionizing radiation is the increase of leakage current which arises from the inversion region connecting n-channel sources and drains along the gate oxide to field oxide transition. This produces edge leakage current that can be very serious in the charge sensitive applications found in image sensors. In our pixel, the floating diffusion (FD) node is where the integrated charges in the PPD are transferred via TX and converted to the voltage signal. Since the array is readout by sequentially scanning using column and row scanners. During readout, the FD node of the last pixels in a row are electrically floated as dynamic memories and suffer edge leakage from transistors RST and TX. Physical design techniques of enclosed layout transistor (ELT) and P+ guard ring[12] are proved to be very effective for significantly reducing leakage current in NMOS transistors. The source/drain diffusion is completely isolated by the gate and the edge leakage is significantly reduced. By employing the P+ guard ring, the inter-transistor leakage through the inverted

field oxide is substantially curtailed.

In our pixel, both transistors RST and TX are designed using ELT. As shown in the Fig. 2. The floating diffusion is composed of two enclosed geometry. In this configuration, the floating diffusion has no directly interaction with the defective STI, and the edge leakage current from these two NMOS transistors is considerably reduced. The leakage on the floating diffusion is only dominated by the junction leakage which does not increase in the presence of radiation. On the other hand, the adoption of ELT transistors and P+ guard rings results in silicon area penalty and leads to reduced fill-factor. ELT transistor is usually several times larger than traditional layout and should only be used for critical transistors. The other two transistors, SF and RSL, are therefore designed using non-ELT. This is consolidated by the fact that the biasing current in the source follower is usually larger at several orders of magnitude than the leakage current.

C. Programmable Source Follower Biasing Current

Circuits designed for space applications must be able to operate under wide temperature range. The biasing current in the source follower determines the settling time on the column bus and therefore affects the readout speed. Although a bandgap reference circuit can be used to generate a stable column biasing voltage, the basing transistor itself can be vulnerable to temperature fluctuation (variation of mobility and threshold voltage). Fig. 4 shows the simulated biasing current under different temperatures. The gate voltage is constantly biased using a bandgap-generated 550 mV. It shows that the current increases almost linearly with temperature. The biasing current is designed to be 1.3μA at room temperature, but it deviates to maximum over $\pm 30\%$ within the range of temperature from $-40°C$ to $110°C$.

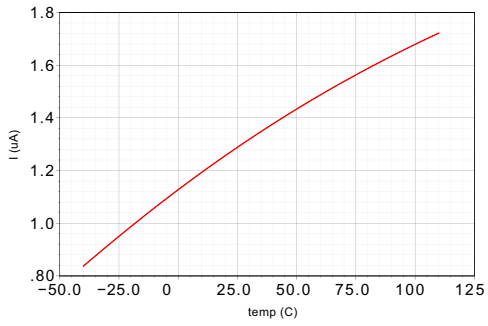

Fig. 4. Simulation result of the biasing current due to temperature change.

When switching from one pixel to another, the settling time on the column bus depends on the signal swing on the FD node. In the worst-case scenario, the FD nodes of two consecutive pixels can experience the maximum possible swing and thus need the longest settling time. Fig. 5 shows the simulation waveform on the column bus at the worst-case scenario with respect to different temperatures. The discharge requires around 350ns before the column bus attains the steady

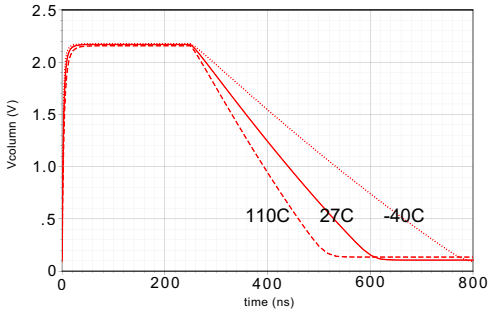

Fig. 5. Simulated waveform of the column bus showing the operation of charging and discharging under different temperature in a 256×256 pixel array. The waveform denotes the worst-case readout scenario of two consecutive pixels with maximal voltage difference. The charging operation shows no significant difference. However, discharging through the biasing transistor is strongly affected under different temperature

state at room temperature, but much longer at lower temperature ($-40°C$). The incomplete discharging within 350ns fails to attain the steady state on the column bus and violate the readout timing.

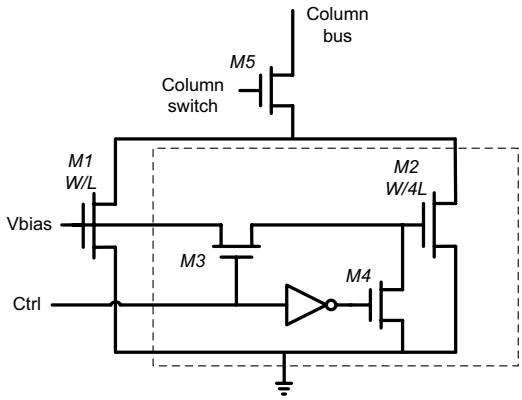

Fig. 6. Schematic of the proposed programmable column biasing circuit for temperature compensation. The circuit in the dotted-line box is enabled at low temperature when digital $Ctrl$ signal generated from the off-chip controller is high. $M3$ is turned on and $M4$ is turned off, so $M2$ is connected in parallel with $M1$ to supply an additional 25% biasing capability.

A programmable column biasing circuit is designed in order to compensate the biasing current variation due to temperature change. As illustrated in Fig. **??**, $M1$ is sized to provide nominal current for high temperature ($110°C$). While at low temperature, off-chip controller can produce a signal ($Ctrl$) which turns on transistor $M2$. The W/L ratio of $M2$ is a quarter of $M1$, the biasing current is thus scaled to 125%. This enlarged biasing current offers the opportunity to compensate the reduced biasing current due to temperature fall and therefore assure the discharge time within the timing requirements.

III. VLSI Implementation

A prototype chip including four arrays of 256×256 pixel was implemented using TSMC 0.18 μm CIS process (2-poly

6 metal layers). Fig. 6 (a) illustrates the layout of the chip as well as one pixel. In the pixel, the recess distance between the N implant and STI is set to 0.2μm and the P-Well structure is used in between for protection. The PPD is also geometrically designed to be as square as possible to reduce the junction perimeter to minimize the dark current. The RST transistor and the TX transistor, as discussed earlier, are designed to be ELT transistors. P+ guard ring is employed around the photodiode and the RST transistor. SF transistor and RSL transistor are designed using minimum size, and they are protected by the P+ guard ring as well to avoid inter-transistor leakage current. The pixel pitch of 6.5μm is approximately the size limitation in this compact pixel configuration for a fill factor of about 30%.

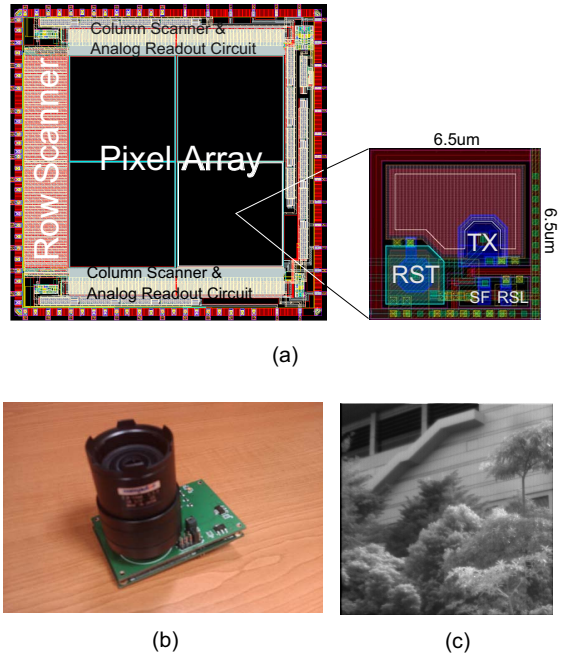

Fig. 7. (a) Layout of the proposed pixel architecture which has been embedded into a test chip. (b) Chip test platform which uses a FPGA system for chip controller and image readout. (c) Reproduced sample image

TABLE I
CHARACTERIZATION RESULTS OF THE IMAGE SENSOR

Technology	TSMC 0.18 μm CIS
Supply voltage	3.3V
Pixel pitch	6.5μm
Pixel array format	256×256
Voltage swing	1.28V
Dynamic range	60dB
Sensitivity	2.92V/lux·s
FPN	1.02%
Dark current	16.2mV/s

As illustrated in Fig.6 (b), the chip test platform is used to characterize the chip. Table I gives the summary of the preliminary characterization results and Fig.6 (c) shows a reproduced sample image under outdoor illumination conditions with about 2ms integration time and off-chip correlated-double sampling.

IV. Conclusion

In this work, we have presented a radiation tolerant 4T pixel architecture for space application. The design approaches of the pixel were described in detail and major design concerns lie within the design of the photodiode and the floating diffusion node against radiation-induced dark current. In order to adapt the sensor to the dramatic temperature change in space environment, a programmable column biasing current circuit was proposed. Circuit simulations demonstrate the successful operation of the sensor. A prototype chip including four arrays of 256×256 pixel was fabricated using the TSMC 0.18 μm CMOS image sensor process. We have included our preliminary characterization results of the chip.

V. Acknowledgements

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References

[1] C. Shoushun, F. Boussaid, and A. Bermak, "Robust intermediate readout for deep submicron technology cmos image sensors," *IEEE Sensors Journal*, vol. 8, no. 3, pp. 286 –294, march 2008.

[2] S. Chen, W. Tang, and E. Culurciello, "A 64 × 64 pixels uwb wireless temporal-difference digital image sensor," in *Proceedings of 2010 IEEE International Symposium on Circuits and Systems (ISCAS)*, june 2010, pp. 1404 –1407.

[3] S. Chen, A. Bermak, and Y. Wang, "A cmos image sensor with on-chip image compression based on predictive boundary adaptation and memoryless qtd algorithm," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 19, no. 4, pp. 538 –547, april 2011.

[4] H. Hughes and J. Benedetto, "Radiation effects and hardening of mos technology: devices and circuits," *IEEE Trans. Nuclear Science*, vol. 50, no. 3, pp. 500 – 521, 2003.

[5] D. Mavis and D. Alexander, "Employing radiation hardness by design techniques with commercial integrated circuit processes," in *AIAA/IEEE 16th Digital Avionics Systems Conference, 1997*, vol. 1, Oct. 1997, pp. 2.1 –15–22 vol.1.

[6] V. Goiffon, M. Estribeau, and P. Magnan, "Overview of ionizing radiation effects in image sensors fabricated in a deep-submicrometer cmos imaging technology," *IEEE Trans. Electron Devices*, vol. 56, no. 11, pp. 2594 –2601, 2009.

[7] V. Goiffon, P. Magnan, O. Saint-pe, F. Bernard, and G. Rolland, "Total dose evaluation of deep submicron cmos imaging technology through elementary device and pixel array behavior analysis," *IEEE Trans. Nuclear Science*, vol. 55, no. 6, pp. 3494 –3501, 2008.

[8] P. Rao, X. Wang, and A. Theuwissen, "Degradation of spectral response and dark current of cmos image sensors in deep-submicron technology due to gamma-irradiation," in *37th European Solid State Device Research Conference (ESSDERC)*, 2007, pp. 370 –373.

[9] J. Tan, B. Buettgen, and A. Theuwissen, "Radiation effects on cmos image sensors due to x-rays," in *2010 8th International Conference on Advanced Semiconductor Devices Microsystems (ASDAM)*, 2010, pp. 279 –282.

[10] M. Innocent, "A radiation tolerant 4t pixel for space applications," in *International Image Sensor Workshop, Bergen, Norway, 2009.*, 2009.

[11] H. I. Kwon, I. M. Kang, B.-G. Park, J. D. Lee, and S. S. Park, "The analysis of dark signals in the cmos aps imagers from the characterization of test structures," *IEEE Trans. Electron Devices*, vol. 51, no. 2, pp. 178 – 184, 2004.

[12] E. El-Sayed, "Design of radiation hard cmos aps image sensors for space applications," in *17th National Radio Science Conference*, 2000.