

# A New Match Line Sensing Technique in Content Addressable Memory

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The paper presents a new match line sense amplifier for Content Addressable Memory. It successfully addresses the weaknesses of contemporary designs. Extensive simulation results using a 1 V/65 nm CMOS process from STMicroelectronics have verified that the proposed sense amplifier outperforms other five contemporary designs in terms of energy consumption, area requirement and robustness. This is achieved by using a differential amplifier coupled with a pulse pre-charge technique. More specifically, the proposed sensing technique consumes 78% less energy than the conventional design. Additionally, it can work under a wide range of temperatures (from 0 °C to 100 °C) and is almost insensitive to process variations.

Keywords: Low-energy, CMOS memory, VLSI

## 1. Introduction and Literature Review

CONTENT-ADDRESSABLE Memory (CAM) is a type of solid-state memory that compares the search data with all stored data in parallel and returns the address at which the match data is found[1]. Fig. 1 shows the simplified architecture of a CAM, consisting of an array of CAM cells, a search-word register, a column of sense amplifiers and a priority encoder. Each row of the array has  $n$  CAM cells and one associated match line (ML). Its operation is as follows: first a search word is broadcasted to the array through the differential search lines (SLs), and then the search data on the SLs will be compared directly with the stored data within each CAM cell by the comparison circuits (N1-N4). If at least one mismatch occurs on a row, one of the compare branches in the mismatched cell is turned on. A path (or multiple paths) to ground will discharge the ML, indicating a miss. If all of the stored bits on a row are identical to the search bits, none of the compare branches will be turned on hence the ML voltage remains unchanged, indicating a match. A match line sense amplifier (MLSA) is used in each row to improve the speed by digitizing the voltage transition on the ML. The priority encoder receives the search results from the sense amplifiers and returns the address of the highest priority row that indicates a match.

Since CAM compares all of its stored words concurrently, its search speed is high. However, this comes at a cost of high energy consumption, mainly due to the high switching activity of the MLs[1]. Therefore, a lot of works have been proposed to reduce the energy consumption of CAM by reducing either the switching activity or voltage swing of the MLs. Among those designs, the charge-injection[2] and the pre-charge low MLSAs[3-5] are the most attractive designs because of their single-clock, high-speed and low energy characteristics. However, all of these designs have their limitations. The charge-injection design[2] is robust but a capacitor is associated for every ML, so the area of the MLSA increases a lot; the pre-charge low MLSAs including the current-race[3], the stability[4] and the positive-feedback[5] designs are very sensitive to external environment variations including temperature and process corners. In view of that, we propose an improved MLSA design offering a better performance in terms of energy, area, and robustness.

## 2. The Proposed MLSA design

The proposed sense amplifier is shown in Fig. 2. It consists of two differential inputs (ML and SML), an asymmetrical differential amplifier, a pulse generator, four reset NMOSs (N5-N8), one excitation PMOS (P1) and one inverter. The SML input is taken from the CAM cell as shown in Fig. 2. Unlike the conventional design, the sources of transistors N2 and N4 in the CAM cell are connected by a wire named SML instead of directly connecting them to ground.

The operation of the proposed design can be divided into three phases, namely standby, excitation, and evaluation. During standby, both the ML and the SML are discharged to ground through N5 and N6 by asserting RST to high. Meanwhile, the EN signal is also asserted high to reset the sense amplifier. As a result, nodes C1 and C2 are discharged to zero through N7 and N8 while node MLSO is charged to  $V_{DD}$ . During excitation, (from now on, we assume the search data is already broadcasted into the differential SLs), the excitation pulse from the pulse generator is asserted to pre-charge the ML to a certain level as shown in Fig. 3. During evaluation, the search data on the SLs are compared with the stored data within each CAM cell by the comparison circuits (N1-N4). In a match case, since there is no path from the ML to the SML,

the ML voltage will stay at the pre-charge level while the SML voltage stays at zero volt. In a mismatch case, the ML voltage will decay through the charge sharing between the ML and the SML, while the SML voltage will rise steadily until the ML voltage and the SML voltage of this word become the same. After a certain duration of time, EN is asserted low to turn on the sense amplifier to amplify the evaluation result to a full CMOS output. As shown in Fig. 2, in the match case, since the ML voltage is higher than the SML voltage, the gate-to-source voltage of P3 ( $V_{GS3}$ ) is larger than that of P2 ( $V_{GS2}$ ). Although P3 has a smaller W/L ratio, I2 is larger than I1, hence C2 is charged to a high voltage level. Then MLSO is discharged to zero indicating a match. For a mismatch, the ML and SML voltages will be almost the same. Since P2 has a large gm ratio, I1 is larger than I2. Through a current mirror, C2 will keep low thus the MLSO will stay at  $V_{DD}$ . In addition, a dummy word which is identical to a matched ML is also included to turn off the sense amplifier by charging EN to a high level when the output has been sensed to save energy.

### 3. Simulation and Performance Comparison

The proposed design and another five representative circuits[2-6] have been simulated in a standard 65nm/1V CMOS process from STMicroelectronics at 500 MHz. All six designs are optimized to obtain the same sensing delay of 1.2 ns. After that, the other design factors, namely, energy consumption, sensing delay, leakage and stability will be used to evaluate the relative performance of the proposed design.

Fig. 4 shows the sensing delays of all six designs at different operating temperatures. It clearly shows that the stability[4] and the positive-feedback[5] designs are very sensitive to temperature variations. The other four designs' sensing delays only have about 2.5% variations but the proposed design gives the fastest sensing speed. As for the leakage current (Fig. 5), the proposed design is the best performer with 68% less leakage when compared with conventional design[6] and 38% less leakage when compared with the current-race design[3].

As shown in Fig. 6, the process corner analysis suggests that only the charge-injection[2] and the proposed design are almost insensitive to process variations. However, the proposed design has a lower sensing delay when compared with the charge-injection design[2].

Table I summarizes the overall performance of the six circuits at 1V/500 MHz frequency, room temperature. Among the six designs, it's apparent that the proposed design is the best performer in terms of energy consumption. It consumes 78% less energy when compared to its conventional counterpart[6]. This is mainly due to the low voltage swing of its ML. In addition, the proposed design consumes the least total gate area of only  $0.498 \mu\text{m}^2$  thanks to its simple structure. On the other hand, the charge-injection design[2] requires a much larger area of  $23.12 \mu\text{m}^2$  because of the tank capacitor associated with each ML.

### 4. Conclusion

A new match line sense amplifier in parallel CAM is presented in this paper. It reduces 78% of energy consumption compared with conventional MLSA and outperforms other four recently published low-energy MLSA designs. The temperature variation and corner analysis also prove that the proposed design is sufficiently robust to operate at varying external condition while offering the highest speed performance and lowest leakage current. Therefore, the proposed design is the most suitable candidate for implementing high capacity parallel CAM in nano-scale CMOS technologies.

### 5. References

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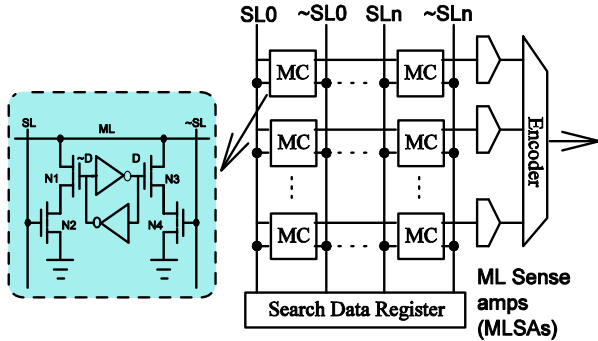


Fig. 1 A general CAM architecture consisting of an array of CAM cells, a search data register, a column of MLSAs and a priority encoder.

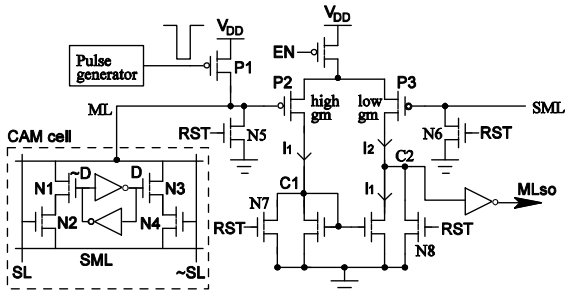


Fig. 2 The proposed MLSA with ML and SML, coupled with a pulse generator and an asymmetrical differential amplifier.

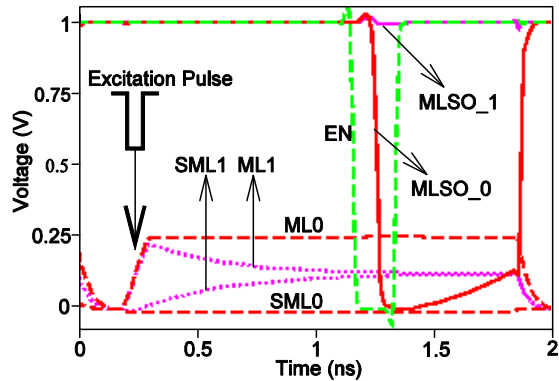


Fig. 3 Voltage waveforms of ML, SML and sensing output, match (ML0, SML0, and MLSO\_0) and one mismatch (ML1, SML1, and MLSO\_1).

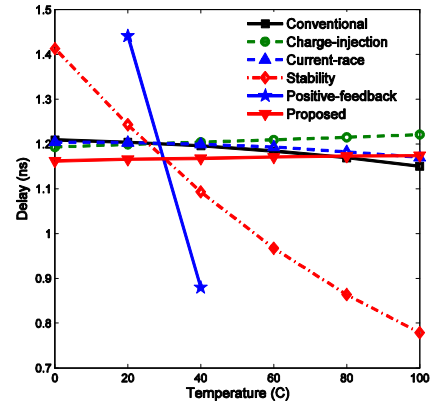


Fig. 4 Sensing delay for all circuits in comparison at different operating temperatures.

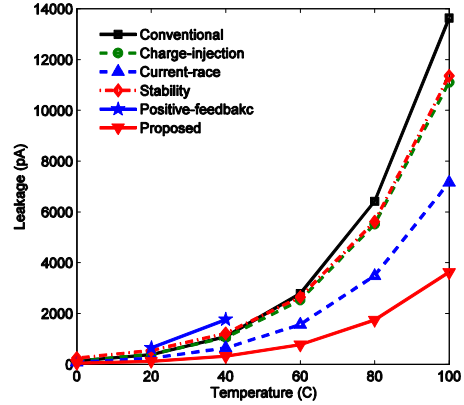


Fig. 5 Leakage current for all circuits in comparison at different operating temperatures.

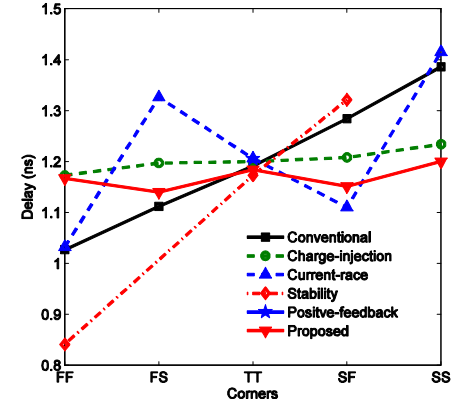


Fig. 6 Sensing delay for all circuits in comparison at different process corners.

Table I Performance comparison of the MLSAs using a 1V/65 nm CMOS technology at 500 MHz.

	Conv[6]	Charge injection[2]	Current race[3]	Stability[4]	Positive feedback[5]	Proposed
Energy, fJ/bit/search	1.15	0.382	0.748	0.373	0.307	0.253
Delay, ns	1.206	1.199	1.203	1.203	1.203	1.167
Total gate area, $\mu\text{m}^2$	0.54	23.12	0.626	0.98	0.83	0.498