Compact Gray-Code Counter/Memory Circuits for Spiking Pixels

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Abstract

In this paper, novel compact counter/memory circuits are proposed for spiking pixels. The proposed in-pixel circuits combine digitizing and memory functions, and use Gray code to limit switching activity and read-out error. Three possible implementations are proposed to meet the requirements of speed, pixel fill-factor and dynamic range.

1. Introduction

With the advent of deep submicron CMOS processes, which feature a minimum lithographic feature size below 0.18µm, it becomes now possible to build high performance single chip cameras, integrating image capture and advanced on-chip processing circuitry [1][2][3].

The fully integrated camera-on-chip, promises to offer significant advantages in terms of manufacturing cost, system volume and weight, power dissipation and increased built-in functionalities in deep submicron CMOS technologies [1][3]. An increasingly large number of high-volume consumer imaging products do now integrate CMOS image sensors. Examples include cell phones, cameras, fax machines, scanners to name a few. However, the ongoing aggressive scaling of the power supply is rapidly limiting the analog signal swing at the sensing node, degrading sensor signal to noise ratio (SNR) [4][5]. This is because noise source contributions increase with device scaling [4][5]. For example, as the thickness of the dielectric material is scaled down below 3nm, significant tunneling current may flow from the drain to the gate in an off-state device or from the gate to the source in an on-state device [4]. This leakage current is "exponentially" dependent upon the oxide thickness. For sub-3nm gate oxide thicknesses, the tunneling current can be five orders of magnitude larger than acceptable photodiode dark current densities [4], degrading significantly the performance of conventional active pixel sensors. Their dynamic range, commonly defined as the ratio of the largest non-saturating signal to the standard deviation of the noise under dark conditions, will consequently significantly worsen with device scaling, since the analog signal swing is reduced and noise contributions are seen to increase due to the predominance of short channel effects [5]. The sensor dynamic range and peak SNR are directly proportional to the well capacity $Q_{sat}=V_{swing} \times C_{sense}$, where V_{swing} and C_{sense} represent the voltage swing and capacitance at the sensing node, respectively [6]. The peak SNR of conventional active pixel sensors can be expressed as $SNR_{peak}=Q_{sat}/q$ [6]. For a 0.13µm technology, the projected peak SNR is less than 30dB, which is inadequate [7].

Pulse-Frequency Modulation (PFM) pixels (or spiking pixels) have been proposed to tackle SNR and dynamic range degradation [8]. These pixels encode illumination information into a train of spikes or pulses [8] and use an asynchronous self-reset scheme to increase the effective well-capacity of the photodiode. As a result, the effective well-capacity for PFM pixels becomes $m \times Q_{sat}$, where m is the number of self-resets performed during integration. This results in a m-fold increase in peak SNR [7]. The achievable dynamic range will only be a function of the resolution of the in-pixel counter, which in turn is limited by the pixel size.

The actual integration of a high resolution counter at the pixel level has received so far little attention and has been limited to a conventional flip-flop construction, resulting in a prohibitively high number of transistors and significantly degraded fill-factor [9]. In this paper, we describe a novel compact counter circuit topology combining counting and memory functions and evaluate its performance in a number of logic design styles. Potential advantages and application of the proposed implementation over previous implementations [8][9] include robust operation at low voltages, multiresolution high speed imaging, motion vector estimation, real-time imaging as well as dynamic range extension. This paper is organized as follows. The next section describes the basic operating principle and implementation of an in-pixel counter memory for spiking pixels. Section III discusses design optimization to meet compactness and speed requirements for spiking pixels. Finally, a conclusion is given in Section IV.

2. Pixel Circuitry

The block diagram of the proposed in-pixel circuitry is given in Fig.1. The in-pixel building blocks include a photosensitive element, a reset circuitry, a comparator, a delay chain and an 8-bit Gray counter memory.

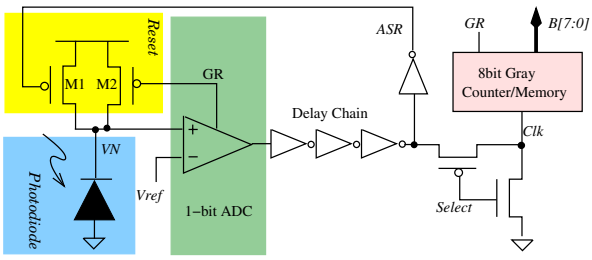

Fig.1 – In-pixel building blocks

The basic operation of the pixel can be described as follows. Initially, a reset operation is performed with the global reset signal GR maintained low. This disables the in-pixel comparator and resets the voltage V_N to V_{DD}. The integration phase starts when transistor M2 is opened (i.e. GR high), enabling the comparator and leaving the photodiode floating. Incident light generates electron hole pairs in the depletion region of the photodiode causing the voltage at the sensing node to decrease from V_{DD} in response to the generated photocurrent. V_N decreases as a function of the intensity of incident light that falls upon the photodiode with high illumination levels resulting in faster voltage drops for V_N. When V_N reaches the reference voltage V_{ref}, the output of the comparator goes high, causing the photodiode to be self-reset through the reset transistor M1. This has the effect of switching back the output of the comparator, which in turn desactivates the reset transistor M1.

To allow for sufficient time to pull up V_N to V_{DD}, an inverter delay chain is used. Note that the voltage at the sensing node V_N is not reset from 0 to V_{DD} but from V_{ref} to V_{DD}. A pulse is generated and received by the Gray code counter each time this self-reset operation occurs. This process is repeated until the end of the integration phase (i.e when global reset signal GR goes low). The time separating successive pulses depends on the rate of decrease of V_N. In fact, if we assume that the intensity of incident light is constant during the integration process, then the frequency of the generated pulse train is a linear function of the incident light intensity. The pulse train Clk at the output of the delay chain is used as a clock signal by the in-pixel counter memory, which counts and stores the number of generated pulses in the form of an 8-bit digital Gray code (Fig.1). Note that the duty cycle of the Clk signal is a function of the number of delay elements present at the output of the comparator.

For the case of 3 inverters, the active pulse width is around 2ns, which means that a simple dynamic memory can be used to maintain charge during this period. This feature is behind the compact Gray code counter memory cell structure shown in Fig.2. The basic idea is to combine counting and memory functions into a compact single circuit. Each bit circuitry comprises an SRAM cell, a DRAM cell and a toggling combinational logic control circuitry (Fig.2). The SRAM cell is implemented by means of two coupled inverters, the DRAM cell by means of a simple MOS capacitor. The role of the DRAM is to hold the value of the pulse count *X* while it is being incremented in the SRAM as shown in Fig.3. Because the duration of the generated Clk pulses is very short, there is no need to refresh the content of the DRAM A_i ($i=0 \rightarrow 7$). During the update (Clk high), the content B_i of the SRAM is inverted and fed back to the SRAM if the toggle condition of the bit is fulfilled (transistor Mn_i ON). When the Clk pulse goes inactive, the DRAM and SRAM cells become connected (transistor Mp_i ON) and the DRAM cell content is updated. Fig.4 illustrates the overall operation of a spiking pixel with in-pixel counter/memory.

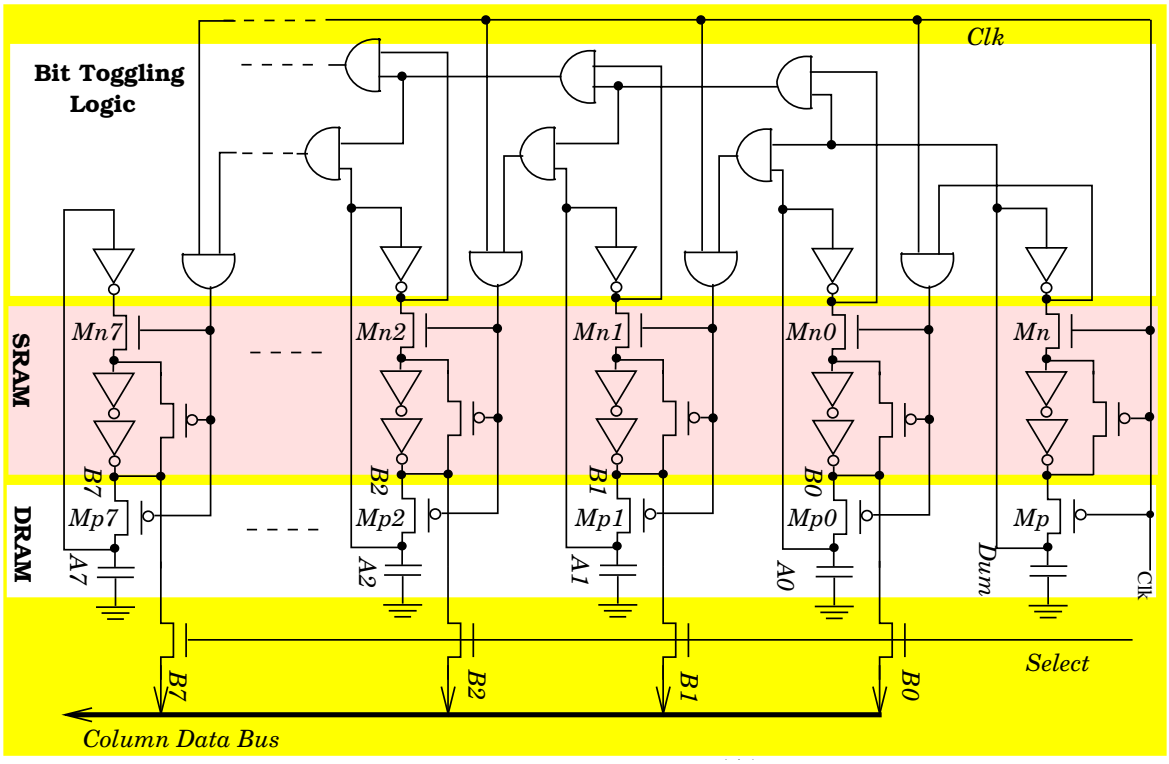

Fig.2 – Gray code counter memory: Circuitry

The operating principle of the Gray counter/memory can be explained by examining the case of the 3-bit Gray code sequence, given in Table I. Note that B_0 toggles every two clock cycles. To monitor whether the number of clock cycles is even or odd, a dummy bit Dum is added and used for this purpose. From Table I, one can deduce that the toggling conditions for bits B_0 and B_1 are $\overline{Dum.Clk}$ and $A_0.Dum.Clk$, respectively. In the same manner, one can deduce a general "toggling condition" for $i \geq 2$ expressed for bit B_i as:

$$Dum.Clk.A_{i-1}\prod_{k=0}^{i-2}\overline{A_k}$$

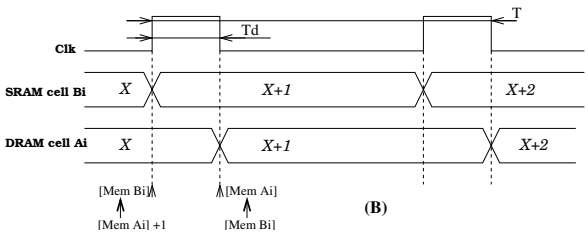

Fig.3 – Gray code counter memory: Operation

3. Design Optimization

The static CMOS implementation of Fig.2 requires a total of 187 transistors, as compared to 214 transistors for a conventional binary counter [9]. In the proposed implementation, the number of transistors can further be reduced by implementing the bit "toggling condition" circuitry using transmission gates. Fig.5 illustrates the implementation methodology in the case of transmission gates for bit B_1. The basic idea is to use cascaded transmission gates in series with transistor Mn_1. When the clock Clk goes high, the content of the SRAM will be updated provided that transmission gates are enabled. As a result, the toggling condition for each bit can be implemented with limited cascaded transmission gates while bringing the overall number of transistors from 187 transistors down to 139 transistors. The number of transistors can further be reduced by implementing the toggling conditions described in Table I, using domino logic gates (Fig.6). The total number of transistors can then be brought down from 187 transistors down to 105 transistors.

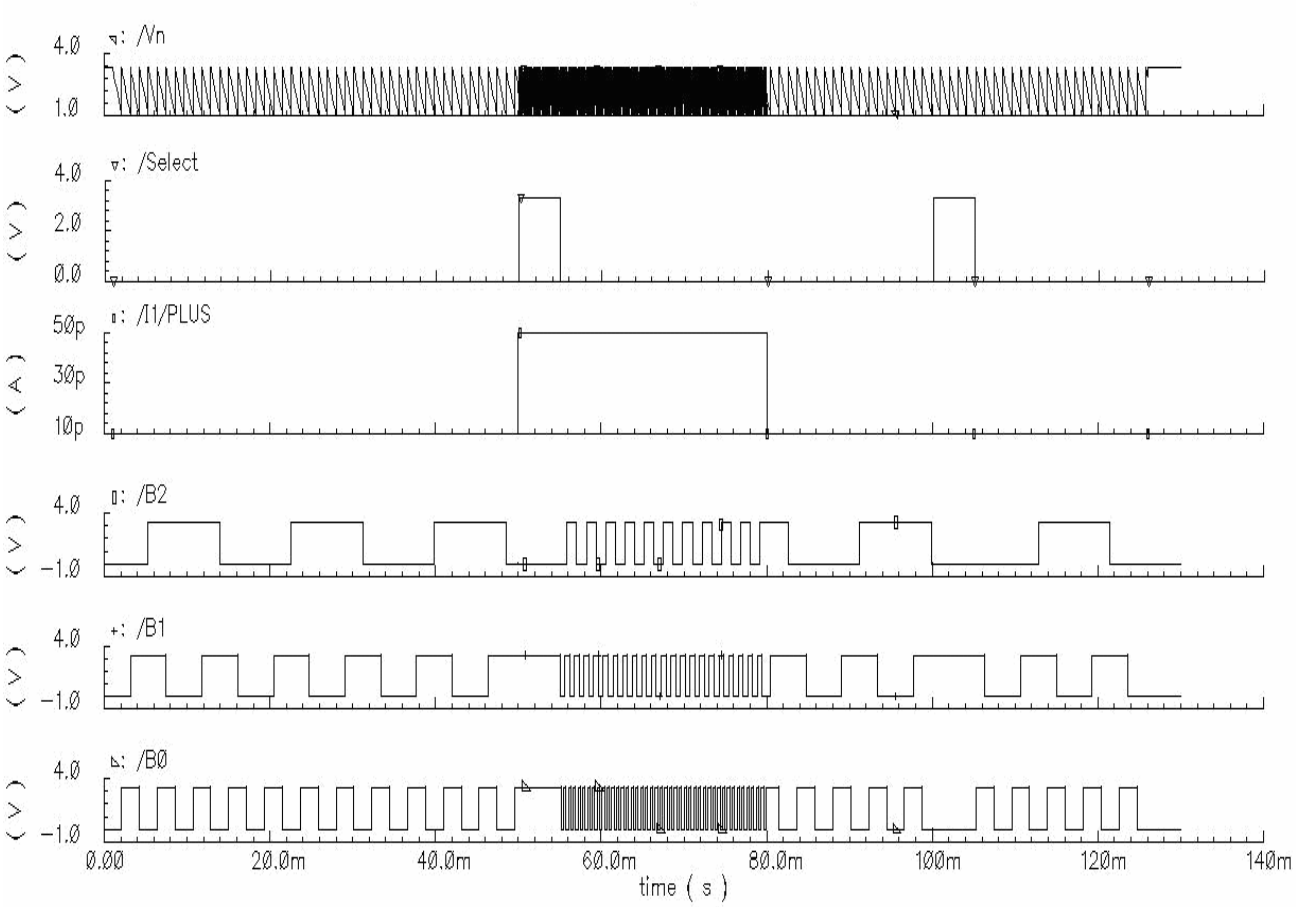

Fig.4 – Gray code counter memory: simulation results

Table I – Counter Sequence for a 3-bit Gray code and corresponding bit toggling conditions. The Gray counter increments with each incoming clock pulse Clk.

Decimal Number	Gray code $B_2B_1B_0$	Dummy Bit	Cycle Number	Toggled Bit	Toggling Condition
0	000	0			
1	001	1	1	B_0	$\overline{Dum}.Clk$
2	011	0	2	B_1	$A_0.Dum.Clk$
3	010	1	3	B_0	$\overline{Dum}.Clk$
4	110	0	4	B_2	$A_1.\overline{A_0}.Dum.Clk$
5	111	1	5	B_0	$\overline{Dum}.Clk$
6	101	0	6	B_1	$A_0.Dum.Clk$
7	100	1	7	B_0	$\overline{Dum}.Clk$

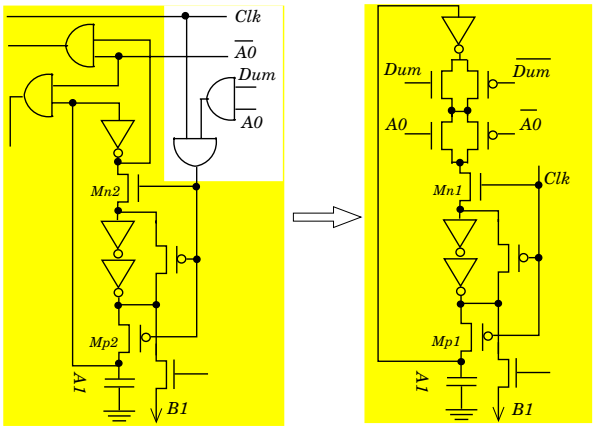

Fig.5 – Improved implementation using transmission gates for B1.

An important feature of the proposed in-pixel Gray counter memory is that the inputs to each bit toggling circuitry are constant upon generation of a Clk pulse. As a result, Clk is the only critical signal in the proposed design. The Clk pulse should thus remain high long enough to enable the update of the content B_i of the SRAM (Fig.3).

Table II – Performance of 3 different implementation schemes in a 0.35µm CMOS process.

Implementation scheme	Transistor count	Minimum Clk pulse
Static Logic	187	190ps
Transmission gate	139	170ps
Domino	105	1.8ns

In a spiking pixel (Fig.1), the width of the generated pulse train becomes wider at higher illumination levels, because the photocurrent continues to discharge the photodiode while the photodiode is being charged by the reset current. For instance, an excessively large photocurrent of 30nA and V_{ref} at 2.8V, result in a clock pulse width of about 3ns. If the photocurrent is now lowered down to 1nA, the pulse width reduces to about 1ns. Note that a wider pulse width does not affect the toggling capability of the proposed counter memory since the upper bound of the pulse width must only ensure that there is no loss of information at the DRAM level.

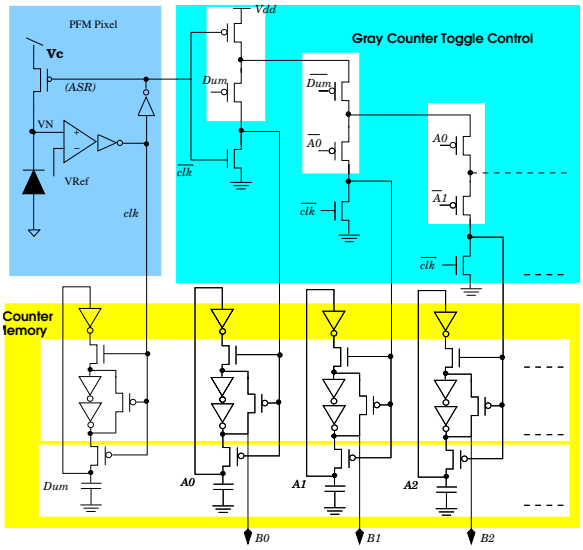

Fig.6 – Counter memory structure implemented using domino

Table II summarizes the performance of the proposed Gray-code memory for three different design logic styles. Reported results reveal a trade-off between compactness and operating speed. The transmission gate implementation was found to offer a good trade-off. The domino logic implementation of the counter memory boasts the lowest transistor count but requires a significantly longer delay chain.

4. Conclusion

Novel Gray-code compact counter memory circuits are proposed for spiking pixels. The proposed in-pixel implementations combine digitizing and memory functions and result in a significant reduction of the transistor count, by a factor of up to 1.78. The proposed in-pixel circuits address the necessary trade-off between compactness and read-out speed for time-domain image sensors.

5. Acknowledgments

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6. References

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