A Second Generation Time-to-First-Spike Pixel with Asynchronous Self Power-off

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***Abstract*— In this paper we propose a second generation time-to-first-spike (TFS) pixel based on an asynchronous self power-off architecture. In this architecture time-to-first spike is used to encode the photocurrent information. Once the first spike is received and read-out using an address event representation (AER), the pixel is forced into standby mode by cutting off the power supply of itself. Simulation results shows that significant reduction in leakage power is achieved which is a major concern when implementing high resolution image sensor in deep-submicron technology. Based on this proposed architecture a prototype was designed in UMC 0.18 μm technology. Each pixel include a photodiode, an event generator and hand-shaking communication protocol using 15 transistors. Each pixel occupies an area of $8.3 \times 8.3\mu m^2$ with a fill factor of 15%. In addition, the new generation TFS sensor features reduced depth of the arbitration tree using high-radix AER building block resulting in reduced overall delay.**

Keywords: Low Leakage Pixel, Time-to-first-spike Pixel, CMOS image sensor, Address Event Representation

I. Introduction

With the ever growing demand for low power and high performance, device dimensions and operating voltages are constantly being reduced. Designing CMOS image sensors using $0.18\mu m$ or even more advanced technologies, which is needed for implementing true camera-on-chip systems, is a challenging task due to the scaling of supply voltage and the increase in leakage currents [1]. Leakage induced power consumption leads to reduction in the battery life in the case of battery-powered applications. The leakage power also affects reliability, packaging, and cooling costs. Moreover, it brings more noise into the system.

In [2], we proposed a vision sensor in which illumination information is encoded in the time-to-first-spike scheme. Each pixel will fire only once per frame. When a pixel reaches the threshold voltage, an event will be passed out of the pixel array using an asynchronous read out protocol (Address Event Representation). After that the pixel will be asynchronously self-reset to the supply voltage and then enters into a standby mode until the start of the next frame. It was shown that the proposed pixel permits significant saving in terms of dynamic power consumption, particularly when compared to a spiking pixel [3]. However, the high reverse-biased voltage on the photodiode constantly draws leakage current from power to ground which will result in an additional power consumption, particularly critical in the case of high photocurrent and large array image sensor designed in advanced CMOS technology. In addition, one should consider the leakage power dissipated in the remaining circuitry of the pixel such as the event generator. One interesting fact about the TFS concept is that information is encoded in the signal latency. The pixel can therefore be completely powered off after receiving the first spike without loosing any information. In this paper, we propose a second generation TFS sensor based on a novel pixel-driven asynchronous self power-off architecture. Once the first spike is received and read-out using the address event representation (AER), the pixel is forced into a standby mode by cutting off the power supply of itself. While maintaining the advantages of the first generation TFS sensor (low dynamic power and low bandwidth requirement), significant reduction in leakage power is achieved using the proposed self power-off sensor. The pixel is reactivated again at the start of next frame. In addition to lower leakage as compared to the first generation TFS imager, improvement is proposed in the handshaking communication between the pixel and the arbitration tree. Indeed, the proposed circuit avoid the use of the column acknowledgment signal hence reducing the number of required buses. A higher radix arbitration building block is also proposed to reduce the depth of the arbitration tree and hence the associated delay.

The paper is organized as follows: Section II introduces the vision sensor based on the new self power-off pixel. In this section we will introduce the pixel operation as well as the leakage reduction technique. Section III shows the image sensor's architecture as well as its VLSI implementation and the proposed higher radix arbitration tree. Section IV concludes this paper.

II. Self Power-off TFS Sensor

A. Operating principle

The schematic of the self power-off time-to-first-spike pixel is shown in figure 1. It is composed of a photosensitive device (reverse biased photodiode P_d) with its internal capacitance C_d, a PMOS reset transistor (*m2*) for global reset, transistors *m3,m4,m6-m8* for event generation and transistors *m9-m13* for handshaking communication protocol with both row and column AER circuits. Transistor *m1* is used as a power gate and transistor *m12* is used to acknowledge the pixel without resetting the photodiode's voltage.

Initially an active high "Rst" pulse will turn On transistor *m15* which turn On the power gate transistor *m1* and thus

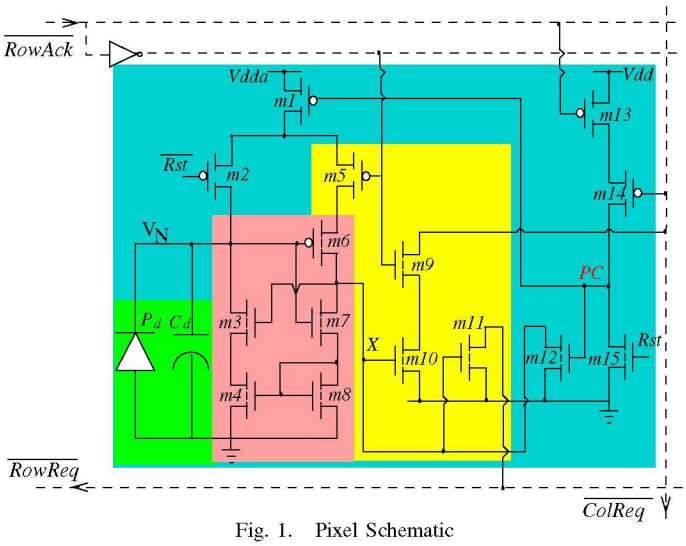


Fig. 1. Pixel Schematic

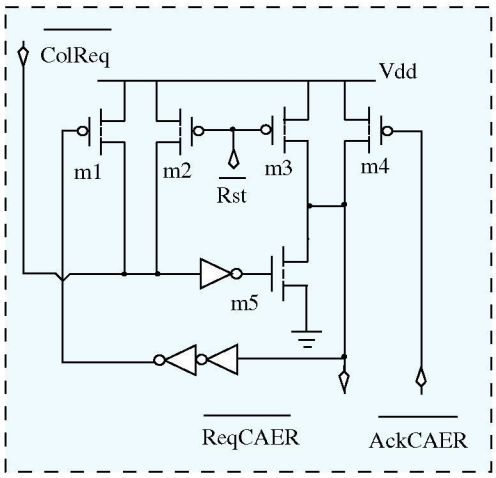


Fig. 2. Column Buffer

the photodiode *Pd* will be pre-charged to the supply voltage. After that, the integration process starts and the photodiode *Pd* is gradually discharged by the photocurrent. The current feedback event generator [4] will be activated when the voltage across the photodiode (V_N) reaches the threshold voltage of the inverter (*m6,m7*) and an active-high event is generated at the output of the inverter (node "X"). To avoid meta-state, the event will be transmitted only if the row within which the pixel allocated is not being acknowledged. This is realized by transistor *m5* which will block the event when the row acknowledgment is active. If the row is not being processed, the event will generate an active low request "$\overline{RowReq}$" through transistor *m11* which is then transmitted to the row AER. When the row AER acknowledge back ("$\overline{RowAck}$"), the pixel will immediately send another request ("$\overline{ColReq}$") to the column buffer which is latched and then propagated to the column AER. When the bit-line of "$\overline{ColReq}$" signal is low enough, which means that the column buffer can successfully receive the request signal, transistor *m14* will be enabled which means that a pull high path by transistor *m13 and m14* is formed to charge the node *"PC"*. Transistor *m1* is closed and this turns off the power supply of the photodiode and the event generator. The event at node "X" will be discharged as well by transistor *m12*. This is an important operation otherwise "$\overline{RowReq}$" signal can not be pulled back by the row AER circuits.

Another new feature in the proposed new generation TFS sensor is the removal of the column acknowledgement signal. One can note that each pixel asynchronously turns off the power itself when the "$\overline{ColReq}$" signal is successfully transmitted. This means that the pixel is only responsible for generating the request by pulling down the "$\overline{ColReq}$" signal while leaving the task of pulling-up the "$\overline{ColReq}$" signal to the column buffer. This not only results in less signal routing in the imager, but also less noise as no column acknowledgment is sent back to the pixel. Figure 2 shows the schematic of the proposed column buffer. It acts as the interface circuits between the pixels array and the column AER. It accepts the column request signal from the pixel array and propagates it to the column AER. The "$\overline{ColReq}$" signal is restored back to its original level by the column buffer after some delay.

B. Leakage Reduction Technique

In our previous self-reset pixel architecture, the photodiode's voltage will be restored to the supply voltage after being serviced by the AER circuit. However, when we implemented this concept in deep sub-micron technologies, the standby mode (after self-reset) will require maintaining the node of the photodiode to Vdd. This will require a flow of current from the power supply which equals to $I_{DC} + I_{Ph}$, where I_{DC} is the dark current and I_{Ph} is the photocurrent, respectively. In addition to this, a leakage current is drawn from the event generator and the rest of the circuit even during this standby mode. Simulation results based on UMC $0.18\mu m$ technology shows a photodiode leakage $I_{DC} = 3.6pA$. The total leakage will obviously increase by orders of magnitude when the pixel is exposed in higher illumination.

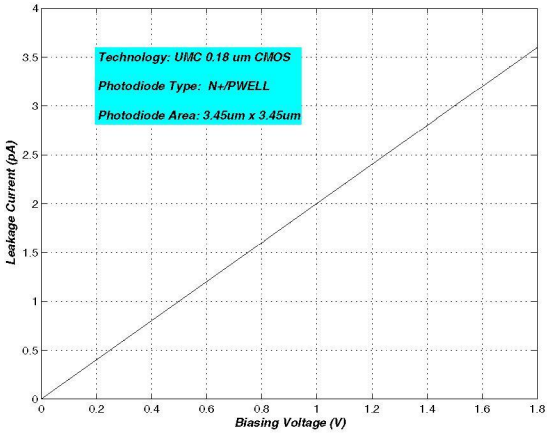
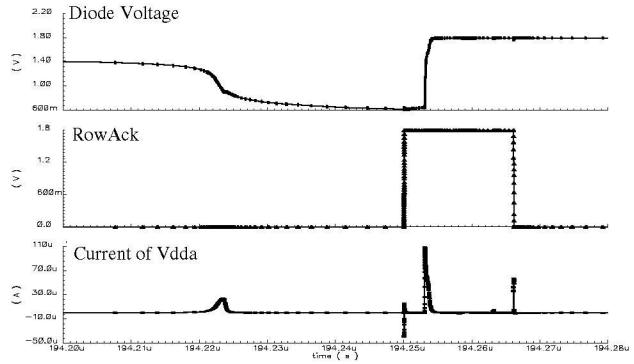


Fig. 3. Simulated photodiode leakage I_{DC} current vs biasing voltage

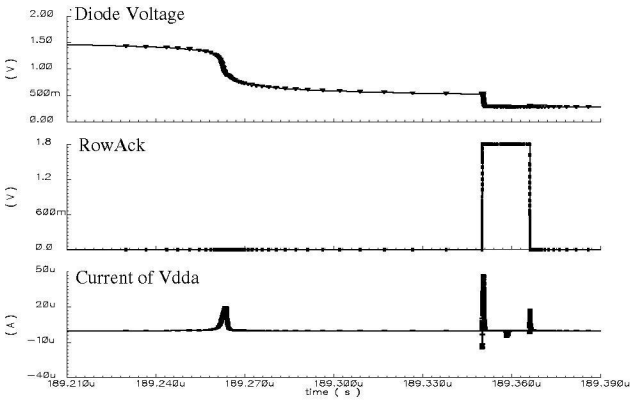
As shown in figure 3, simulation result shows that the photodiode leakage current increases linearly with the reverse biasing voltage which suggests that it is desirable to decrease

this voltage as much as possible during the standby mode. In the proposed new generation TFS pixel, instead of charging back the photodiode to the supply voltage, we let the photodiode to continue to be discharged to ground. In this case, the leakage current discharged by the photodiode is reduced to the minimum possible level.

The leakage current drawn by the event generator also plays a significant role in the total leakage power consumption when the photodiode is biased at the supply voltage. Both of the feedback component (*m3 m4*) and the PMOS *m6* within the inverter (*m6, m7*) contribute to the leakage current. In our new pixel, not only the input voltage to the inverter is lowered, but also the supply voltage is cut off by transistor *m1*. This stack effect [5] leakages much less than a single device.



(A)Photodiode operation and current consumption of self-reset pixel



(B)Photodiode operation and current consumption of self power-off pixel

Fig. 4.

In order to provide a fair comparison between the two generations of TFS pixels, both the two architectures are implemented using the same 0.18 μm CMOS technology. The voltage change on the photodiode of the two architectures are simulated and illustrated in figure 4. One can note the difference of the photodiode voltage between the two cases. In the new pixel architecture, the photodiode keeps discharging after it is acknowledged by "RowAck" signal while the previous self-reset pixel restores the photodiode to the supply voltage. The waveform shows that the pixel's peak operating current is reduced by more than two times which means less noise to the pixel array as well.

The standby current of the photodiode and the event generator is also simulated and shown in Table I. The photodiode's leakage is reduced to $0.1fA$ which is near to negligible. It should be noticed that more saving is to be expected as this figure do not include the photocurrent. Indeed, in the first generation pixel, the standby current required to maintain the photodiode reset level not only needs to compensate for the leakage in the photodetector but also the photogenerated current which is orders of magnitude higher than the photodiode leakage. The event generator's leakage is also reduced 5 times due to the stack effect on the inverter and the lower biasing voltage of the feedback transistors (*m3,m4*).

Architecture	1^{st} Generation	2^{nd} Generation
Photodiode leakage	$3.6pA$	$0.1fA$
Event generator leakage	$20pA$	$4pA$
Total leakage	$23.6pA$	$4pA$

TABLE I

COMPARISON OF LEAKAGE CURRENT IN BOTH TFS PIXEL GENERATIONS.

III. ARCHITECTURE AND VLSI IMPLEMENTATION

The architecture of the vision sensor built with self power-off pixel is shown in figure 5. The architecture includes a pixel array of 128 × 128 pixels, row and column AER for event read-out, and address encoding circuits to output the address corresponding to a subsequent acknowledged event.

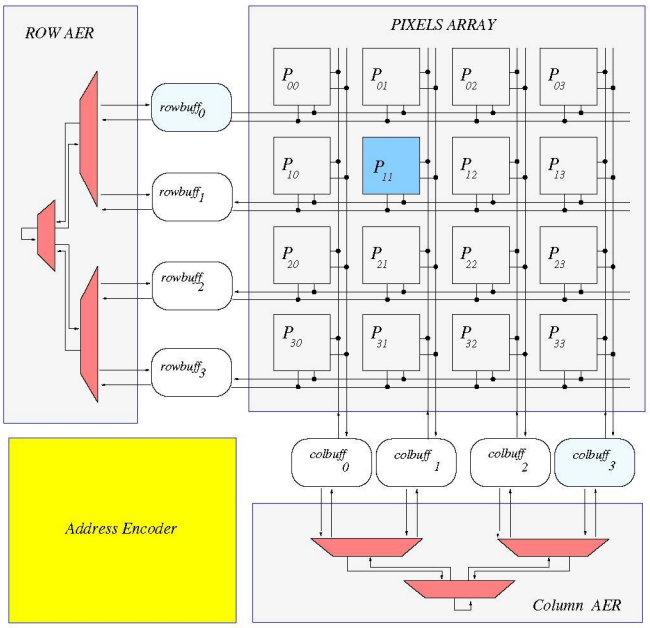


Fig. 5. Imager Architecture

AER(Address Event Representation) is an asynchronous read-out technique which is based on event-driven concept. When a pixel reaches the threshold voltage, an event will be passed out of the pixel array by the AER together with its address. Using a chip level timing unit we can measure the latency or time-to-first spike and therefore the pixels'

brightness can be converted to a digital value as is the case in a conventional DPS without requiring any pixel-level memory. In [2], we proposed a two-input fair arbitration unit in which the priority of the two requests can be toggled every time a request is serviced. Figure 6 shows the experimental results showing how collision (two requests received at the same time) is handled and how priority is toggled.

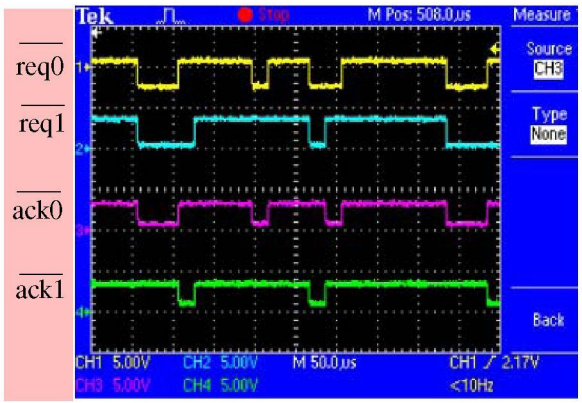


Fig. 6. Experimental results of the 2-input aribter. The results shows that initially Req0 is serviced when both Req0 and Req1 are received at the same time. When a second collision occurs, Req1 is first serviced.

In the second generation TFS sensor, We expanded this concept to implement an arbitration unit which can process four inputs at the same time. With such an arbiter, the depth of the AER tree is reduced while the delay of one arbiter is kept at acceptable level. This will result in a faster processing time when collision occurs, which is very important in order to reduce mismatch due to timing delays in the arbitration tree.

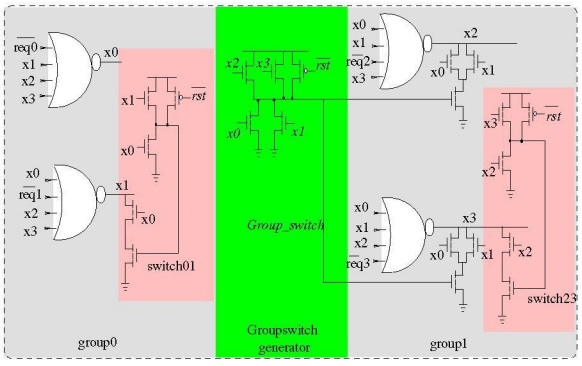


Fig. 7. Arbitration unit of the high radix AER building block

Figure 7 shows four cross-coupled NOR4 gates organized into two groups, group0 ("$\overline{req0}$" and "$\overline{req1}$") and group1 ("$\overline{req2}$" and "$\overline{req3}$"). Within each group, the principle of priority switch is the same as the one in the 2-input building block. A group priority switch signal "Groupswtich" is used to toggle the priority between group0 and group1. For example, if the current priority order is "x0" $\mapsto$"x1" $\mapsto$"x3" $\mapsto$"x2", then after "req0" is received and processed, the priority order will be changed to be "x3" $\mapsto$"x2" $\mapsto$"x1" $\mapsto$"x0". The building block arbiters are then organized in a tree structure. Each building block makes a local priority allocation and transmit the decision as a request to a deeper cell in the tree until a global decision is made by the building block located at the root of the tree.

In order to test the concept proposed in this paper and to compare it with the first generation TFS pixel, a prototype chip was designed and sent for fabrication using UMC 0.18 μm technology. The pixel occupies an area of $8.3 \times 8.3 \mu m^2$ with a fill factor of 15%. Figure 8.A shows the layout of the chip while Figure 8.B shows the layout of the new pixel.

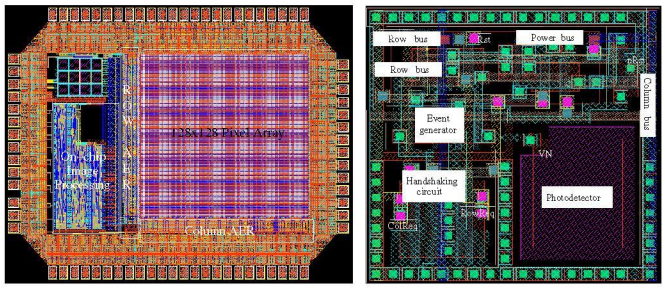


Fig. 8. (A.) Chip Layout and (B.) pixel layout.

IV. Conclusion

In this paper a self-power-off second generation pixel sensor is proposed using power gate technique which reduces the leakage power in the time-to-first spike scheme. In this pixel, latency information is read-out using the AER circuit. Once the pixel is serviced, it is automatically forced into a standby mode in which the power is cut-off from both the photodetector and the event generator. It was shown that around 85% of the leakage power is saved in each pixel making the concept very interesting for high resolution CMOS vision sensors fabricated in deep-submicron technologies, in which leakage is a very critical issue. In addition, in the proposed second generation TFS pixel an improved handshaking protocol is proposed which avoids the use of column acknowledgment signal. Furthermore, higher radix arbitration unit is proposed in order to reduce the depth of the arbitration tree.

Acknowledgment

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