Time-Delay-Integration CMOS Image Sensor Design For Space Applications

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Abstract

In recent years, remote imaging systems have been used for a wide range of applications in geological exploration, oceanography, meteorology, military reconnaissance, etc. Differing from the normal cameras, the remote imaging systems capture still scene with the camera in uniform motion. With the limitation of the system moving velocity, only a short integration time is allowed, which will result in a low signal-to-noise ratio (SNR) in dark illumination conditions. Therefore, time-delay-integration (TDI) image sensors are widely applied. In an integration-mode TDI image sensor, the active pixels are placed in more than one row (stage) in across-track direction, with the pixel stages perpendicular to the image sensor movement direction (along-track direction). When the camera system moves at a constant velocity, the pixels are exposed to the same scene stage by stage and the panoramic image in the along-track direction is thus produced. As a result, each pixel stage has contribution to the optical integration, so the effective integration time and the signal strength is enhanced. For the multi-pixel-stage integration mechanism of TDI, the charge-coupled devices (CCDs) offer an effective solution. In CCD image sensors, the photo charge is stored in the potential well of the original pixel following integration, and then transferred out row by row. Meanwhile, the charge of the same column yet different rows can be added together during the transfer operation with higher efficiency. Accordingly, CCDs can perform TDI operation without any external support. Consequently, CCDs still have the largest share of the TDI image sensor market,

even through complementary metal-oxide-semiconductor (CMOS) image sensors have increased in popularity in recent years.

In most office and industrial applications, TDI cameras are supported by stationary rails and powered by direct current (DC) adapters. Accordingly, the additional motion and power consumption are not serious concerns. Nevertheless, in remote imaging applications, the issues and limitations should be taken into account. Firstly, the satellites which support them are sometimes affected by unforeseen disturbances, such as adjustments of the solar panels, alterations to the momentum wheel and so on, which would introduce residual motion to the across-track direction (vibrations). In TDI CCD sensors, the traveling of the charge pockets on the focal plane should be always aligned with the along-track direction. However, owing to the vibrations, the image produced would be blurred and distorted. Furthermore, miniaturization is a prevailing trend in satellites. Consequently, the batteries and solar panels cannot provide sufficient power for the CCDs, which have higher power supply voltage and power dissipation, to sustain long-term operation. Moreover, the CCDs lack random accessibility and system-on-chip capability. Therefore, based on these factors, TDI CCD sensors have been rendered unsuitable for small satellites.

In a attempt to overcome the aforementioned shortcomings, this thesis primarily focuses on the TDI CMOS image sensors. The main contributions can be summarized as four aspects: (1) A TDI CMOS image sensor was proposed with dynamic pipeline adjacent pixel signal transfer. Following the operation of conventional TDI, the photo signal will be shifted stage by stage and a given photodiode will be reset by the previous-stage photo signal. Meanwhile, this TDI sensor can also configure effective TDI stages for dynamic range and signal-to-niose ratio optimization, as well as the signal transfer direction to compensate for the vibrations. (2) A TDI architecture with single-ended column-parallel signal accumulators was proposed. The TDI operation will be conducted

by the off-pixel accumulators, whereby all the photo signals of each TDI stage will be read out after exposure. Accordingly, a 256×8-pixel prototype sensor was designed and fabricated. (3) An online deblurring (ODB) algorithm was proposed to address the blurred image issue caused by vibrations, which was subsequently developed into an 8-stage TDI CMOS image sensor with 256 column-parallel signal accumulators. The sensor can compensate for image shifts on the focal plane, enabling the production of sharper images even in scenarios involving complicated vibrations. (4) A two-step analog-to-digital convertor (ADC) prediction scheme was proposed for low-power CMOS image sensors, and optimized for TDI sensors. Based on the spatial likelihood of natural scenes, the prediction scheme identifies the most significant bits (MSBs) of a selected pixel using the quantization results of its neighboring pixels in the previous row, which enables a significant reduction in A/D conversion steps on MSBs and power consumption. A 384×256-pixel prototype chip was also developed to verify the scheme. Based on it, an improved TDI CMOS image sensor with high dynamic range was designed.

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List of Abbreviations

AC	Alternating Current
ADC	Analog-to-Digital Convertor
APS	Active Pixel Sensor
ASF	Average Sharpness Function
BDI	Buffered Direct Injection
CCD	Charge-Coupled Device
CDS	Correlated Double Sampling
CMOS	Complementary Metal-Oxide-Semiconductor
CTE	Charge Transfer Efficiency
CTIA	Capacitive Trans-Impedance Amplifier
DC	Direct Current
DDS	Delta Double Sampling
DI	Direct Injection
DR	Dynamic Range
FD	Floating Diffusion
FF	Fill Factor
FFT	Fast Fourier Transforms
FMC	Forward Motion Compensation
FPN	Fixed Pattern Noise

FOV	Field of View
GA	Gain Amplifier
LEO	Low Earth Orbit
LSB	Least Significant Bit
MOS	Metal-Oxide-Semiconductor
MSB	Most Significant Bit
NIR	Near-Infrared
ODB	Online Deblurring
OP-AMP	Operational Amplifier
PD	Photodiode
PFM	Pulse Frequency Modulation
PPD	Pinned-Photodiode
PPS	Passive Pixel Sensor
PSF	Point Spread Function
PWM	Pulse Width Modulation
RSF	Relative Sharpness Function
RTS	Random Telegraph Signals
SAR	Successive Approximation Register
SC	Switched-Capacitor
SF	Source Follower
SNR	Signal-to-Noise Ratio
TDI	Time Delay Integration
UAV	Unmanned Aerial Vehicle

Chapter 1

Introduction

1.1 Background and Motivation

In recent years, remote image sensing systems have found a wide range of applications in geological exploration, oceanography, meteorology, military reconnaissance, etc. Unlike the normal cameras, which must be relatively still to the scene in operation, the remote image sensing systems capture still scene with the camera in uniform motion. So the movement velocity of the system becomes a critical factor and limitation, and higher velocity would mean a shorter integration time. Since the velocity of aircrafts, e.g. unmanned aerial vehicle (UAV), is adjustable, their integration time shall also be capable of changing accordingly. While, the satellites should move at the fast orbital velocity, and thus the integration time is left limited and short.

Taking low earth orbit (LEO) satellites, whose effective optical path is shown in Fig. 1.1, as example. The orbit height is 600 km, and the focal length is 200 mm, so that if the ground resolution is set as 20 m, then the maximum pixel pitch can be expressed as

$$L_{pixel} = 20\ m \cdot \frac{200\ mm}{600\ km} \cong 6.67\ \mu m \qquad \text{(Eq. 1.1)}$$

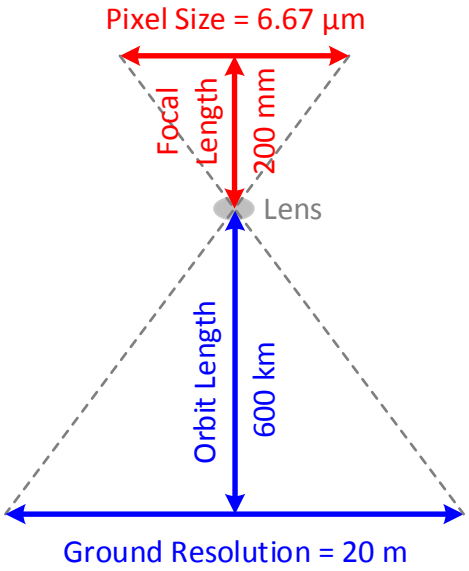

Figure 1.1: Effective optical path of satellite.

Therefore the maximum integration time would be limited to

$$t_{i,max} = \frac{ground\ resolution}{first\ cosmic\ velocity} = \frac{20\ m}{7.9\ km/s} \cong 2.53\ ms \qquad \text{(Eq. 1.2)}$$

Given the hindering limitation of the satellite imaging systems, an exceptionally low signal-to-noise ratio (SNR) on the premises of twilight condition is naturally introduced into the theoretical and real world.

In order to address this pressing problem and make the satellite cameras miniaturized and light in weight, time-delay-integration (TDI) is widely used to photograph the earth surface, the concept of which is described in Fig. 1.2. In an integration-mode TDI image sensor, the active pixels are placed in more than one row (stage) in across-track direction, and the pixel stages are perpendicular to the movement direction of the camera (along-track direction). When the camera system moves at a constant velocity, the pixels are exposed to the same scene stage by stage, and the panoramic image in the along-track direction is thus produced. Drawing a line from the single line scanner, there are several stages of pixels in the set-up of the TDI image sensor, with each exposing itself

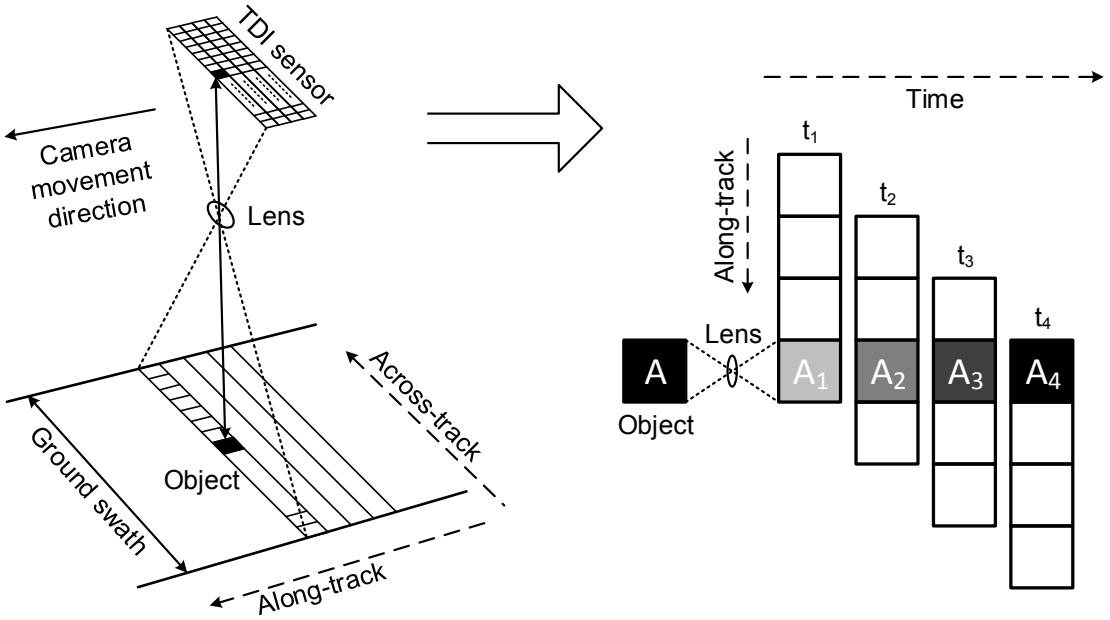

Figure 1.2: TDI image sensor system.

to the same scene once. The structure serves the purpose of enormously beefing up the strength of signal by reinforcing the gathered solar energy and prolonging the time for optical integration.

In the instance of Fig. 1.2, there are 4 pixel stages in one column in the movement direction of the camera. By the sequential order of time, the positions of TDI image sensor are reflected and marked each time in the form of t_1, t_2, t_3 and t_4 accordingly. Take t_1 as an example, the Object "A" on the ground is projected at the first pixel in the column, generating a photo signal as A_1. With the camera's scanning, at t_2, the second pixel produces a new photo signal from "A", and A_2 represents the sum of photo signals having been created out of these first two stages. The theory follows in the same way with the rest two stages. It goes without saying that A_4 amounts to the final output of the photo signals yielded throughout the process of all the four pixels. It can be deducted that with the moving of camera the photo signals are accumulated by transferring each

projection of each pixel stage in the same one column to the next stage, rather than read out directly from each exposure. By doing so, the total sum of photo signals is added up to the final output signal throughout all the TDI stages. It is obvious that where TDI is equipped with n pixel stages, it would bring about the multiplication of integration time by n times as such. In the meantime, effective as it is, the dynamic range (DR) will be correspondingly cut by $\sqrt{n}$ times, owing to input-referred noise and dark current in the integration-mode camera. Since the final photo signal is linearly enlarged by n times, the SNR is accordingly improved by $\sqrt{n}$ times [1–3].

Currently, the mainstream of TDI image sensors are implemented by charge-coupled device (CCD) technology. In CCD image sensors, the photo charge would be stored in the potential well of the original pixel after integration, and then be transferred out row by row. And the charge of same column but different rows can be added up together during the transfer operation. The innate charge transfer operation and high charge transfer efficiency (CTE) render the CCDs competent as TDI sensors run well without additional supporting devices or circuits. In most office and industrial applications, the TDI cameras are placed under proper illumination condition, supported by stationary rails, and powered by the direct current (DC) adapters, hence, the extra motion and power consumption would not be serious concerns. However, regarding remote image sensing systems, the successful operation of TDI CCDs can only be achieved with the assumptions that the movement of satellite and the traveling of the charge pockets on the focal plane are synchronized, and also that the flight direction of the satellite is aligned with the pixel column. Unfortunately, this is not a feasible plan in real-life practice due to the fact that the flexible components on the satellite are likely to cause jitter in the change of the rotation speed of the momentum wheel, adjustment of the solar panels, and so on [4,5]. Furthermore, the synchronization is also affected by the related considerations including satellite orbital motion, attitude change and the Earth's rotation error [6]. To

make it even worse, the pointing accuracy is reported to have reduced to be as low as employing small satellites [7]. Under these circumstances, the charge transferred direction would not be exactly the same as the satellite flight direction. In the final analysis, these non-idealities will cause residual motion in the across-track direction (vibration), which would lead to errors in both alignment and synchronization, and further result in blurred or geometry distorted TDI images. Moreover, the TDI CCDs would cause interruption in the image motion, which would make the image even more blurred and geometry distorted.

Nowadays, miniaturization is a main trend in satellites and UAVs. Correspondingly, the batteries and the solar panels are also gradually shrinking in size, so the power is becoming a critical limitation of the performance of the whole system. Since the CCDs need high power supply voltage and high power dissipation, the small-size batteries and solar panels cannot provide enough power for them to maintain long-time operations. For remote image sensing systems, high power dissipation may increase the risk of system power shutdown, which would lead to permanent communication loss. Thus the power consumption is another drawback of CCDs and a concern of remote image sensing system. Moreover, the CCDs are also lack of random accessibility, system-on-chip capability and on-chip image processing capability. For these reasons, the TDI CCD sensors are not suitable for remote image sensing systems equipped in small satellites and UAVs.

1.2 Objectives

The main objective of this thesis is to develop low-power TDI complementary metal-oxide-semiconductor (CMOS) image sensors for space applications. CMOS processes are employed rather than CCD technologies because of their low-power voltage, low-power operation, high-level integration, random accessibility, system-on-chip capability and on-chip image processing capability [8–10]. Four aspects are included:

(1) Investigate the mechanisms of the various issues that might arise in satellite imaging system, and figure out the effective solutions to the above-mentioned obstacles for remote image sensing systems;

(2) Propose, design and implement innovative TDI CMOS image sensors and/or develop design methods to rectify or compensate for the satellite movement errors, thereby consequently improving the TDI image quality, and extending the usage of proposed TDI design to other airborne imaging systems, such as UAVs;

(3) Propose, design and implement innovative TDI CMOS image sensors with high dynamic range;

(4) Propose, design and implement innovative TDI CMOS image sensors with low-power signal readout path.

1.3 Thesis Contributions

The main contributions can be summarized as four aspects:

(1) A TDI CMOS image sensor was proposed with dynamic adjacent pixel signal transfer and pipelined reset method. Following the conventional TDI operation, the photo signal is shifted stage by stage, and a given photodiode is reset by the previous-stage photo signal. This TDI sensor can also configure the effective TDI stages for DR and SNR optimization, and the signal transfer direction to compensate the vibrations.

(2) A TDI architecture with single-ended column-parallel signal accumulators was proposed. The TDI operation is carried out by the off-pixel accumulators, whereby all the photo signals of each TDI stages will be read out after exposure. Based on that, a 256×8-pixel prototype sensor was designed and fabricated.

(3) An online deblurring (ODB) algorithm was proposed to address the blurred image problems caused by vibrations, and implemented into an 8-stage TDI CMOS image sensor with 256 column-parallel signal accumulators. The sensor can compensate for image shifts on the focal plane, and produce sharper images even in scenarios involving complicated vibrations.

(4) A two-step analog-to-digital convertor (ADC) prediction scheme was formulated for low-power CMOS image sensors, and optimized for TDI sensors. Based on the spatial likelihood of natural scenes, the prediction scheme predicts the most significant bits (MSBs) of a selected pixel adopting quantization results of its neighboring pixels in the previous row, which enables significant reduction of A/D conversion steps on MSBs and power consumption. A 384×256-pixel prototype chip was also fabricated to verify the scheme. Then an improved TDI image sensor with high dynamic range was designed with the prediction-based ADC scheme equipped.

1.4 Thesis Organizations

The rest of this thesis consists of six chapters, and is organized as below.

Chapter 2 makes studies of a literature review on the previous related works. It starts with the brief introduction of CCD and CMOS image sensor technologies, followed by a comparison between them. Then it presents the popular readout technologies for CMOS image sensors in three aspects: signal amplification, noise cancellation and column-parallel ADCs. Next, a brief review of the existing TDI image sensor architectures is provided. After that, the mechanisms of the vibration issue are studied, and the corresponding solutions are discussed in detail.

Chapter 3 employs a dynamic pipeline adjacent pixel signal transfer method to address the vibration-induced blurred images. The photo signals can be transferred to different

directions following the image motion on the focal plane, so as to reduce the vibration effects. This chapter elaborates the sensor architecture, TDI signal path, operation principle, and chip implementation.

Chapter 4 is dedicated to a TDI CMOS image sensor design with column-parallel single-ended signal accumulators, which performs the TDI operations. It illustrates the sensor architecture, TDI signal path, sensor operation, noise analysis, chip implementation, test platform and measurement result in detail.

Chapter 5 proposes an anti-vibration TDI CMOS image sensor with the online deblurring algorithm being integrated into the column-parallel signal accumulators. This chapter concentrates on the basic ideas, algorithm, sensor architecture, TDI signal path, operation principle, noise analysis, chip implementation, test platform and measurement result of the sensor.

Chapter 6 presents a two-step ADC prediction scheme for low-power CMOS image sensors, which can predict the MSBs of a selected pixel according to quantization results of its neighboring pixels in the previous row based on the spatial likelihood of natural scenes, so as to significantly reduce the A/D conversion steps on MSBs and power consumption. This chapter first introduces the algorithm in background, description, implantation and simulation. Then it describes a prototype chip with the prediction scheme in detail, i.e., sensor architecture, ADC architecture, chip implementation and measurement result. Finally, it presents a modified high dynamic range TDI CMOS image sensor applying the prediction scheme.

Chapter 7 draws some conclusions of the presented work, and provides recommendation for the future research.

Chapter 2

Literature Review

This chapter presents the exhaustive reviews on the previous related works and studies in literature. To begin with the brief introduction of CCD and CMOS image technologies and their basic characteristics, followed by a comparison between them. Then the major signal readout technologies are discussed, such as signal amplification, noise cancellation and column-parallel ADCs. Afterwards it presents a concise section of existing TDI image sensor architectures, including CCD-type TDI, pixel-level TDI, column-level TDI and digital-domain TDI. Next, two issues in the remote imaging systems, sun glint and vibration, are studied with both the mechanisms and popular solutions.

2.1 Fundamentals of Image Sensors

The image sensor proves to be the foremost device which determines the image quality of a camera. Since invited by George Smith and Willard Boyle working in Bell Labs in October 1969, the CCD technology has almost completely replaced the tube technology, becoming the most popular imaging device in use in digital still and video cameras. However, after decades of development, the shortcomings of CCDs still remain and affect

the image quality. While, the new CMOS processes bring significant improvements to the image sensors, their low voltage, low-power operation, high-level integration, random accessibility, system-on-chip capability and on-chip image processing capability make the CMOS image sensors occupy most of the consumer electronic market [11]. Nowadays, CCD and CMOS turn out to be the predominant image sensor technologies.

2.1.1 CCD Image Sensors

Generally, an image sensor contains two functions: convert photon to electron and convert charge to voltage/current signal. The difference between CCD and CMOS lies in the way how they carry out their functions. In the CCD technologies, the photo-to-electron conversion is carried out within the pixel. Fig. 2.1 shows the typical architecture of a CCD image sensor and the pixel cross-section view. With regard to the former, a typical CCD image sensor, consists of a two-dimensional pixel array on a thin silicon substrate, a readout amplifier, vertical and horizontal access circuitries. The fundamental photo-detecting unit of CCD is a metal-oxide-semiconductor (MOS) capacitor, which serves as a photodiode (PD) and analog memory. Under the reverse bias condition, a potential well is formed in the substrate. The negatively charged electrons will be migrated to an area underneath the positively charged gate electrode, and electrons generated by photon will be trapped and stored in the depletion region up to the full well capacity. In a two-dimensional CCD array, individual photo-detecting units are separated by biasing voltage applied to the gates in one dimension (column-wised direction); and are electrically isolated from their neighbors by insulating barriers in the substrate in the other dimension (row wised direction) [12]. Therefore, one CCD pixel normally contains three photo-detecting units.

The charge-to-voltage/current conversion in CCD is usually carried out in the off-pixel-array floating diffusion (FD) [13]. It is the last stop that a charge packet is trans-

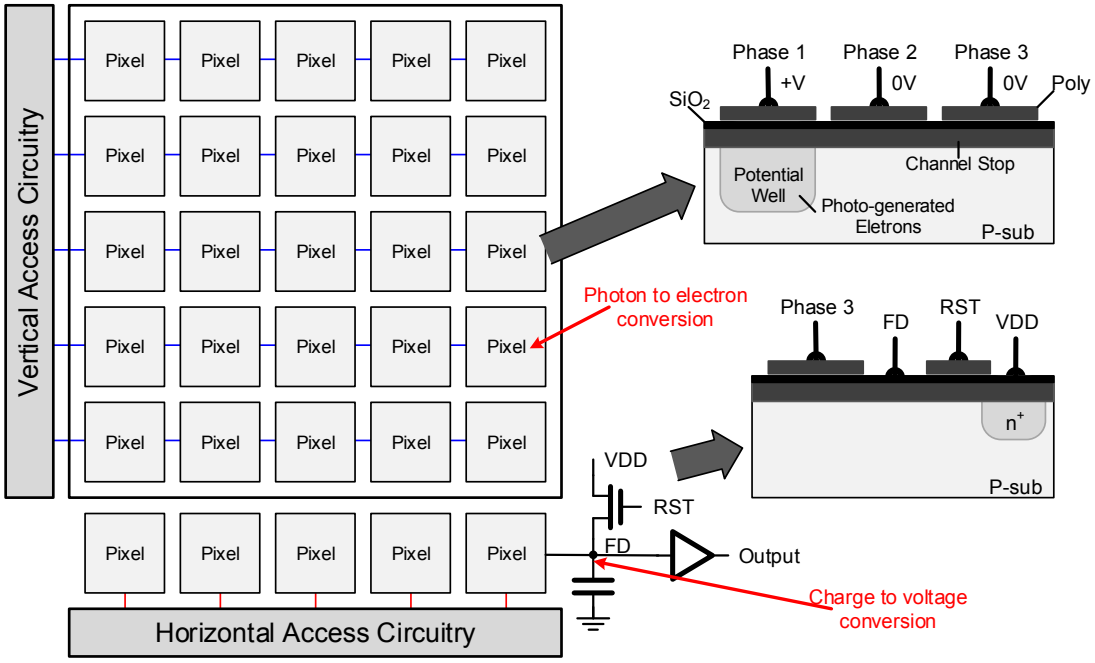

Figure 2.1: Typical architecture diagram of a CCD image sensor and the pixel cross-section view.

ferred out, where the charge is stored in a one-terminal-floated capacitor. The FD is connected to an on-chip amplifier, and the voltage signal converted from the charge packet is output through the amplifier. Then the reset transistor is turned on to clean up the FD for a new charge packet.

In a CCD image sensor, after integration, the pixel array will be read out row by row, for every row will be transferred to the next one till the last row is transferred to the off-pixel-array pixel, also named as the CCD register, in which the charge packets are transferred in row-wised direction. Fig. 2.2 gives the charge transfer operation of CCDs [14]. During integration, only one gate (the left one) is reverse biased, and the charge packet is stored in the potential well. After integration, the neighboring gate (the middle one) is reverse biased to extend the potential well to the middle gate. In this manner the charge packet is stored under both left and middle gates. Afterwards, the

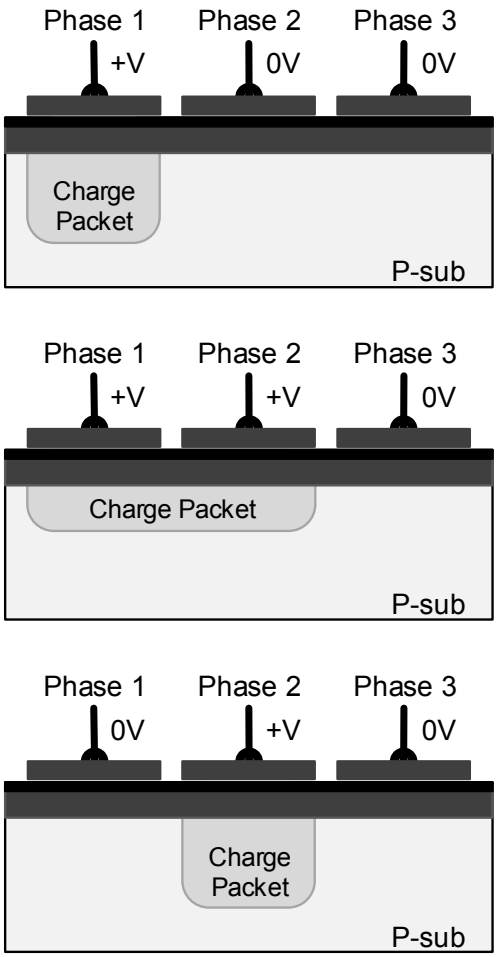

Figure 2.2: CCD charge transfer operation.

left gate is turned off, and the charge packet will be forced to the potential well under the middle gate. By repeating the process, the charge packet can be transfer one pixel by one pixel.

As stated above, it can be learned that in the pixel array, all the photo-generated signals are transferred as charge. In an $m \times n$ pixel array, the charge packet can be transferred $(m + n)$ times in the worst scenario. Therefore, it is of critical importance that all the charge be transferred gate by gate. Charge transfer efficiency (CTE) is defined as the fraction of the well charge that is transferred at each step [15]. Owing to

the specialized techniques, i.e. fringing field and overlapping gates, the CTE in CCDs can be achieved as high as 99.999 % [16].

Following the above-mentioned architecture and transfer method, the noise sources are as follows: photon generated shot noise in the photo-detecting unit, shot noise from dark current (significant at high temperatures), reset noise from the reset transistor switching off, thermal noise and flicker noise caused by the on-chip amplifier.

2.1.2 CMOS Image Sensor

In the CMOS image sensors, both photon-to-electron conversion and charge-to-voltage/current signal conversion are carried out in the pixel. The most widely used photo-detector is p-n junction photodiode. When in reverse bias, the photo-generated current will increase linearly to the input light intensity. The photodiode usually works in accumulation mode, in which one node of photodiode is tied to an electrical potential, and another one is electrical floating. Throughout the exposure, photo-generated electrons or holes will move to the surface because of the potential well of the depletion region, which will decrease the potential voltage. The input light intensity can be achieved by measuring the potential voltage drop. Thus, a single photodiode completes both photon-to-electron conversion and charge-to-voltage signal conversion. By this means the voltage signal can be read out using an in-pixel amplifier, i.e. source follower. Because the output signal from a pixel is voltage/current, it is easier to apply many kinds of circuits to process the signal, and execute various operations, which gives a significant advantage compared to the CCD image sensors [17].

As shown in Fig. 2.3, a typical CMOS image sensor contains a two-dimensional pixel array, vertical and horizontal access circuitries, and readout circuitry. The vertical and horizontal access circuitries are used to provide the control signals, and usually are implemented with scanner or shift register [18]. In the case of one-dimensional array, normally

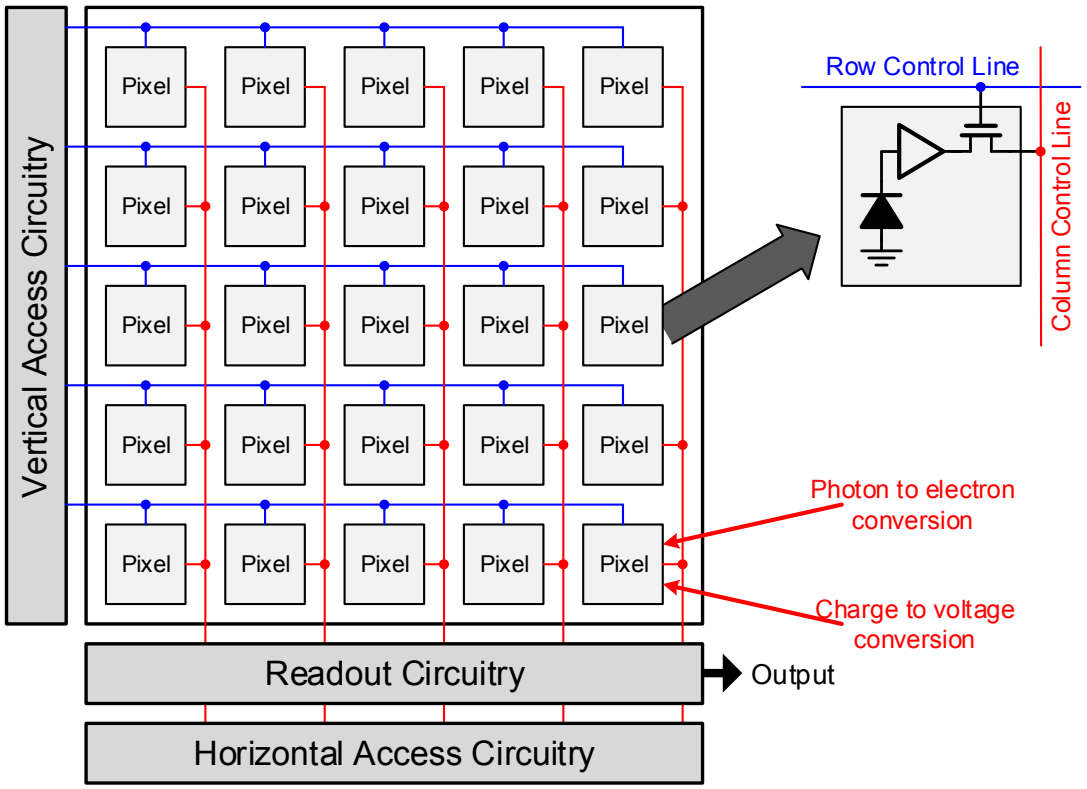

Figure 2.3: Typical architecture diagram of a CMOS image sensor.

one set of readout circuits is shared by pixels in the same column. The readout circuits may consist of a sample-hold (S/H) circuit, noise cancellation circuits, e.g., correlated double sampling (CDS), delta double sampling (DDS), etc., an output buffer or an ADC. The column-parallel structures can not only implement complicated operations, but also largely increase the readout speed of the image data, especially those with column level ADCs [19, 20].

Normally, each pixel holds a photo-detector and transistors. Pursuant to various functions, the transistors can be divided into two groups: amplifier and switch. Between them, the amplifier is optional, and the pixel equipped with only the switch is named as passive pixel sensor (PPS). Carrying only one transistor inside, the PPS possesses a large fill factor (FF), the ratio of the photodiode area to the whole pixel area, which

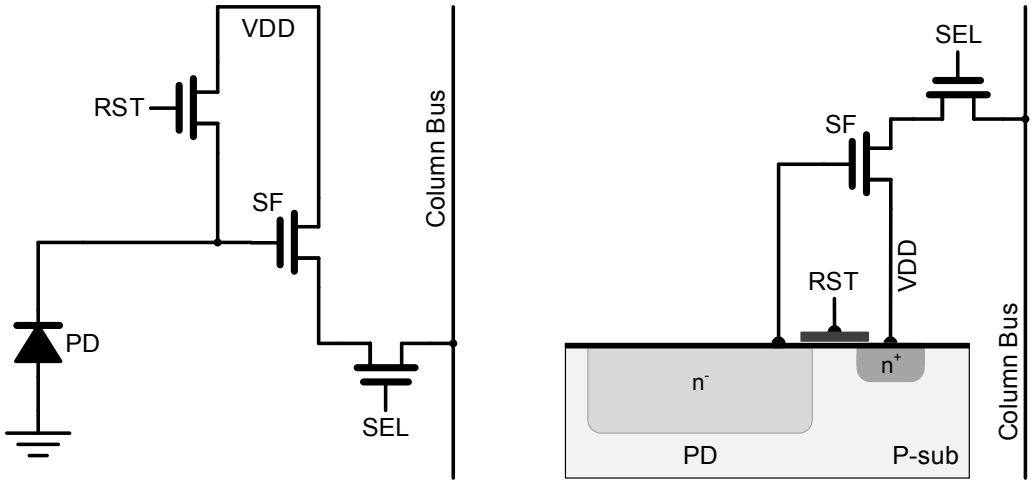

Figure 2.4: Schematic (left) and cross-section view (right) of a 3T-APS pixel.

is desirable for an image sensor. However, the switch will introduce dark current, shot noise, thermal noise and flicker noise that might degrade the output signal strength.

In contrast to PPS, the pixels equipped with active transistors to amplify the output signal are named active pixel sensor (APS). There are two basic APS structures: 3T-APS and 4T-APS, 3T or 4T refers to the pixel consisting of three or four transistors, respectively. Fig. 2.4 shows the schematic and cross-section view of a 3T-APS. The three transistors contained are RST, SF and SEL. RST acts as a switch to reset the PD, SF functions as a source follower to amplify and output the photo signals, SEL also serves as a switch for row-level selective output. The operation procedure runs as follows: first, reset the photodiode by turning on the RST transistor, so as to clean up all the extra charge in photodiode. Then turn off RST to start integration, during which the photo charge is accumulated in the photodiode, while decreasing the voltage of the photodiode. Simultaneously SF would amplify the photodiode voltage and produce the output photo signal before SEL. After integration time, by selectively turning on the $SELs$, the photo signal values of the whole pixel array can be read out from the column buses. After the readout ends, $SELs$ will be turned off, in the same way that a new operation will be

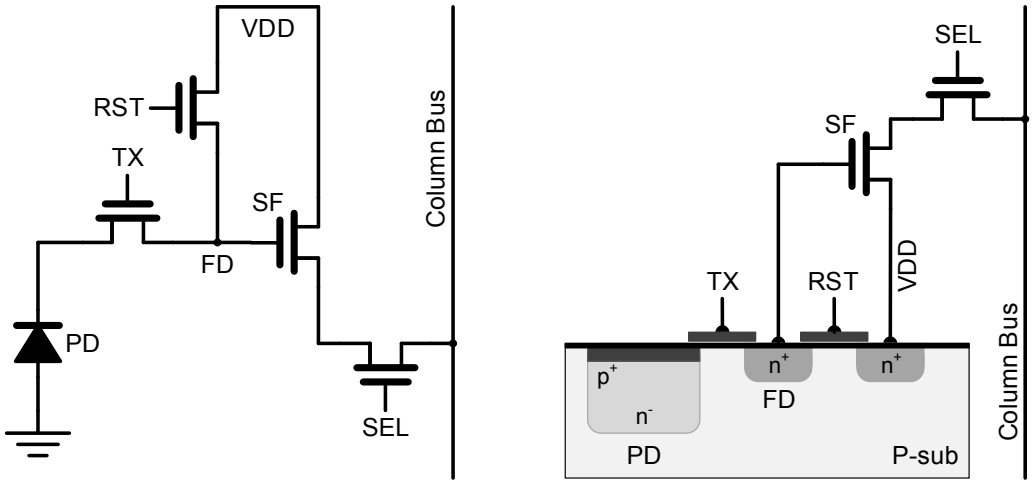

Figure 2.5: Schematic (left) and cross-section view (right) of a 4T-APS pixel.

repeated. With an amplifier inside, the 3T-APS can achieve a higher SNR than that of the PPS, however, the reset noise cannot be reduced as such.

Fig. 2.5 shows the schematic and cross-section view of a 4T-APS. It contains four transistors: among them TX is employed to isolate the photo-to-electron conversion and charge-to-voltage conversion; RST is applied to reset the FD, with SF acting as the source follower to amplify and output the photo signal, and SEL serving as an output switch. The operation procedure works as follows: first, reset the photodiode by turning on the RST and TX transistors, so as to make sure there being no extra charge in photodiode. Then turn off TX to start integration, during which the photo charge will be accumulated in the photodiode, at the same time, keep the RST on to reset the FD, the reset value of FD (containing the reset noise) can be read out through SEL for CDS. After integration, the photo charge is transferred to the FD by turning on the TX, therefore the photo signal value (containing the same reset noise) can be read out. This CDS operation is capable of eliminating the reset noise, and enables the 4T-APS to take on a similar performance to CCDs.

2.1.3 Basic Characteristics

There are numbers of parameters to assess the performance of an image sensor, parts of which are determined by the process technology, in contrast others can be controlled by design. Here lists the important performance characteristics [21]:

2.1.3.1 Dark Current

Dark current, the unwanted charge that accumulates in the photo detector, springs from the random electron-hole pair generation and recombination. This phenomenon is born with very complex generation mechanisms, and usually occurs in the silicon and the silicon-silicon dioxide interface at any temperature above absolute zero. It is a major non-ideality of the image sensor which largely cripples the image quality.

2.1.3.2 Noise

The image sensor is likely to suffer a variety of noise that might degrade its performance. The main types of noise are listed as follows.

Shot noise comes from fluctuations in the number of carriers due to random photon arrive, which is a natural process and cannot be avoided by pixel design. The Dark current also produces shot noise.

Reset noise, also named as k_BTC noise, a kind of thermal noise, is sampled during the shutdown of the reset operation of the FD or photodiode. It can be expressed as $4k_BTR_{on}f$, where k_B is the Boltzmann constant, f is the frequency bandwidth and R_{on} is the ON-resistance of the reset transistor. The thermal noise can be eliminated by CDS operation as mentioned above.

Random telegraph signals (RTS) noise, is introduced by the active Si-SiO_2 interface trap, which is the only type of trap in aggressive MOS transistors with very

small geometries (gate area $< 1\ \mu m^2$). In this kind of transistors, carrier number becomes small, and carriers in the transistor channel are captured and released by interface and near-oxide traps in contact with the channel, that will result the RTS noise. Like flicker noise, RTS noise is also a frequency-related $(1/f)$ noise, and mainly produced by the in-pixel CDS circuit and readout mode [22–25].

Readout noise is the noise caused by the readout circuits, and is mainly embodied in the forms such as thermal noise and flicker noise. Most of the CMOS image sensors are equipped with column level readout circuits, which contain sample-hold circuits, signal amplification circuits, noise cancellation circuits, output buffers or ADCs. The variation and mismatch will bring different offsets to the columns, thereby leading to low image quality. That is called fixed pattern noise (FPN). In image processing level, the FPN can be suppressed by subtracting a dark image taken by the same sensor or superposing many images with the same scene. Also on-chip circuits can be implemented applying the similar algorithm [26].

2.1.3.3 Dynamic Range

The dynamic range of an image sensor is defined as the ratio of the maximum non-saturating signal to the minimum detectable signal [27], as

$$DR = 20log\left(\frac{q_{max}}{q_{noise}}\right) \qquad \text{(Eq. 2.1)}$$

where q_{max} is maximum charge, and q_{noise} is the noise charge. In image sensors, the DR is determined by the noise floor and the full well capacity. It manifests the ability that the image sensor can detect both bright and dark objects in the same scene at the same time.

2.1.3.4 Signal-to-Noise Ratio

The signal-to-noise ratio is an important feature in analog circuits, which represents the signal quality. The SNR is defined as the ratio of the signal to the noise, as

$$SNR = 20log\left(\frac{q_{signal}}{q_{noise}}\right) \quad \text{(Eq. 2.2)}$$

where q_{signal} is the photo charge, and q_{noise} is the noise charge. In image sensors, the signal increases to the light intensity; while the noise is dominated by readout noise in low light illumination and by shot noise in high light illumination.

2.1.4 Comparison between CCD and CMOS

The CCD technologies are developed only for the purpose of image sensors, focusing on the CTE improvement and noise cancellation. While the CMOS technologies aimed at the

Table 2.1: Comparison between CCD and CMOS image sensors

Items	**CCD**	**CMOS**
Fill Factor	High	Moderate or low
Uniformity	High	Moderate or low (FPN)
Output of Pixel	Charge packet	Voltage/Current
Readout	One on-chip SF	SF in every column
Speed	Moderate or low	High
Output of Chip	Voltage	Voltage/Digital
Power Supply	High	Low
Complexity	Low	High, on-chip signal processing
Simultaneity	Simultaneous readout for all pixels, global shutter	Sequential readout for every row, roller shutter

mix-signal processing, even if certain of them require special process for photo detector. The architectures, signal transfer methods and readout methods are all different. Table 2.1 gives the comparison between these two technologies [11].

2.2 Readout of CMOS Image Sensors

Generally speaking, the readout of a CMOS image sensor consists of three parts: signal amplification, noise cancellation and signal output. Among them signal amplification is an effective solution to reduce the readout noise of CMOS image sensors and increase the SNR and DR; noise cancellation is usually utilized to reduce the noise arising from pixel operation, i.e., reset noise and $1/f$ noise; signal output is to output the photo signals outside of the sensor, in analog or digital format, by analog buffer or ADC respectively [28]. Depending on the design requirement, the signal amplification and noise cancellation are optional. Sometimes, they can be put together or linked to the signal output in order to lessen the architecture complexity.

In CCD image sensors, due to their low-level integration, the signals are driven out by an analog buffer in global way, and in advanced technologies, the signal amplification and noise cancellation can also be included [29, 30]. At the beginning of the CMOS image sensors, the readout was also implemented in global way [31], while owing to the high-level integration of CMOS technologies, the multi-channel readout was introduced soon [32, 33], and nowadays, the column-parallel architecture becomes the mainstream method. In this part, the review of the readout technologies is presented elaborately.

2.2.1 Signal Amplification

The typical implementation of the signal amplification circuit uses a switched-capacitor (SC) amplifier, also named as gain amplifier (GA) [34, 35], which can operate the noise

cancellation as well. Fig. 2.6 shows the signal path schematic of a 4T-APS and a gain amplifier, as well as the timing diagram of the signal path. First off, reset the photodiode by turning on the RST and TX transistors, so as to make sure there is no extra charge in photodiode, and the voltage of the PD and FD are pulled to high ($VDD - V_{th,RST}$). Then turn off TX to start integration, during which the photo charge will be accumulated in

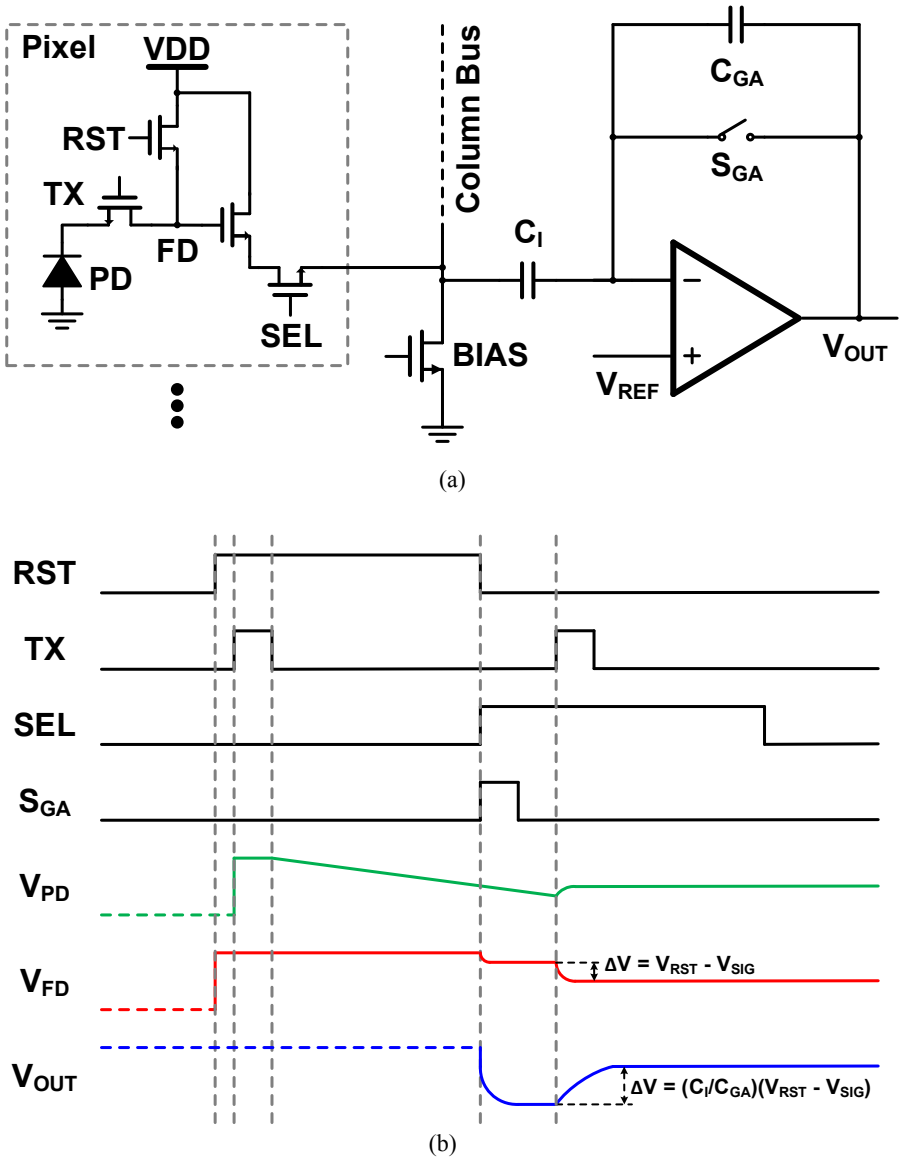

Figure 2.6: (a) Signal path schematic of a 4T-APS and a gain amplifier, (b) Timing diagram of the signal path.

the photodiode and decrease the voltage V_{PD}, at the same time, keeping the RST on to rest the FD. After integration, turn off the RST and on the SEL, S_{GA}, the OP-AMP is configured as a unity-gain feedback, and therefore the reset signal of FD, V_{RST} (containing the reset noise), can be sampled to C_I through SF and SEL. Followed by turn off the S_{GA} and on TX sequentially, to allow the photo signal V_{PH} (containing the same reset noise) would be available on the column bus, and pull the voltage of left terminal of C_I down. in conformity with the law of conservation of electric charge, the extra charge of C_I would be transferred to feedback capacitor C_{GA}, and the output voltage of the gain amplifier can be expressed as

$$V_{OUT} = \frac{C_I}{C_{GA}} (V_{RST} - V_{PH}) + V_{REF} \qquad \text{(Eq. 2.3)}$$

Therefore the photo signal is amplified by (C_I/C_{GA}) times, while the noise from the pixel is reduced by $(\sqrt{C_I/C_{GA}})$ times [36]. Moreover, the noise caused by the RST transistor is cancelled by the subtraction as well.

Combining the signal amplification and noise cancellation together, the gain amplifier is widely applied and developed. In Ref. [37–39], multiple feedback capacitors are employed and can be programmed externally, and then multiple gains can be achieved, as well as the multiple noise behavior. In Ref. [40–42], in the process of the operation, the multiple feedback capacitors can be configured varying from the signal level, so as to realize the adaptive gains, adaptive noise performance and further extend the DR. However, more capacitors would lead to larger area, more mismatch and more parasitic capacitance, which should be taken into serious consideration.

2.2.2 Noise Cancellation

Subtraction is quite a simple but effective way to reduce the noise from pixel, for which several sampling technologies were developed, including correlated double sampling [43–

45], delta double sampling [46–48], quadruple sampling [49, 50], and correlated multiple sampling [28, 51, 52], etc. To discuss the aforementioned sampling technologies, we base on the assumptions regarding to the 3T-APS and 4T-APS structures as follows: n_{rst} is the reset noise due to the RST transistor; $n_{sf,t}$ is the thermal noise caused by the source follower; $n_{sf,f}$ is the frequency-related noise, e.g., flicker noise and RTS noise; n_{ct} is the noise from clock feed through and charge injection when turning off the RST.

2.2.2.1 Correlated Double Sampling

CDS was introduced by White et al. in 1974 [43], and now is the most common solution. The timing diagram of the CDS operation for 4T-APS is given in Fig. 2.7 [44, 45]. The reset signal voltage V_R is sampled just before turning on the TX, and the photo signal voltage V_P is sampled after the voltage of FD is stable. Apparently, n_{rst} and n_{ct} carried by both of the two voltages can be removed. Since the time interval is small, the frequency-related noise n_f can also be eliminated. But the thermal noise caused by the source follower is doubled due to the twice samplings. Thus the effective photo signal and noise are

$$V_{4T,CDS} = V_R - V_P \tag{Eq. 2.4}$$

$$n_{4T,CDS} = \sqrt{2{n_{sf,t}}^2} \tag{Eq. 2.5}$$

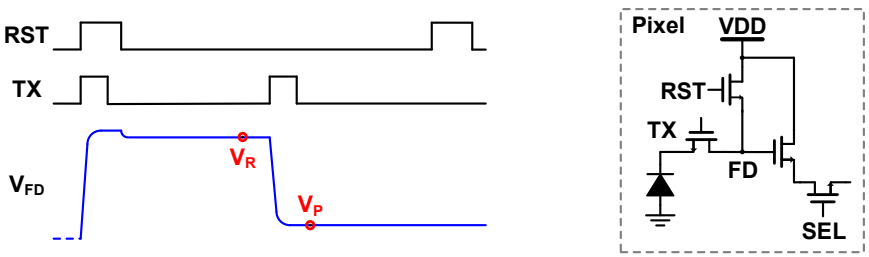

Figure 2.7: Timing diagram of the correlated double sampling for 4T-APS.

As discussed in Section 2.2.1, gain amplifier is the most popular scheme for CDS because it also operates the signal amplification [53, 54]. Sometimes, to reduce the circuit complexity, the CDS function can also be integrated to other circuits, such as the column-parallel ADCs [55].

2.2.2.2 Delta Double Sampling

Unlike 4T-APS, which possesses the floating diffusion to store the reset voltage temporarily all over the pixel array, 3T-APS cannot store the reset voltage in the integration phase and enjoy the benefit of CDS only in analog domain. So another sampling named delta double sampling was proposed [46–48]. As shown in Fig. 2.8, right after the photo signal being sampled, a new reset operation is carried out immediately, and the new reset signal is sampled for subtraction. By doing this, the frequency-related noise n_f can be removed, yet still the reset noise is left unsolved. So the effective photo signal and noise can be expressed as

$$V_{3T,DDS} = V_R - V_P \tag{Eq. 2.6}$$

$$n_{3T,DDS} = \sqrt{{n_{rst}}^2 + {n_{ct}}^2 + 2{n_{sf,t}}^2} \tag{Eq. 2.7}$$

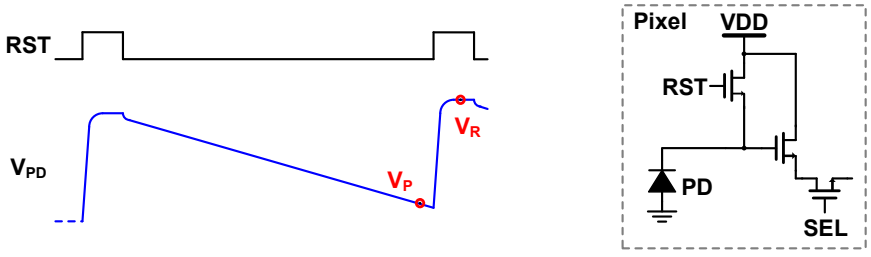

Figure 2.8: Timing diagram of the delta double sampling for 3T-APS.

2.2.2.3 Quadruple Sampling

If twice A/D conversions are involved, the CDS for 3T-APS can be achieved in two solutions. As shown in Fig. 2.9, this first one uses V_{P1} and V_{P2} [49, 50]. After reset, the V_{P1} of each pixel is read out and quantized; followed by integration, the V_{P2} of each pixel is read out and quantized. So the subtraction can be done in digital domain. As the bandwidth of the source follower is limited, the thermal noise of the RST in the reset phase can be ignored. Given that the integration takes a long time, the frequency-related noise is doubled accordingly. Only counting the pixel noise, the effective photo signal and noise can be written as

$$V_{3T,CDS} = V_{P1} - V_{P2} \tag{Eq. 2.8}$$

$$n_{3T,CDS} = \sqrt{{n_{sf,t}}^2 + 2{n_{sf,f}}^2} \tag{Eq. 2.9}$$

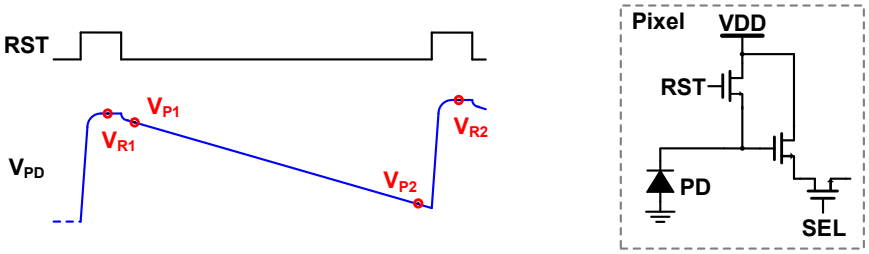

Figure 2.9: Timing diagram of the quadruple sampling for 3T-APS.

Based on the above-mentioned sampling, an improved solution applying four samplings, V_{R1}, V_{P1}, V_{P2} and V_{R2}, was proposed, that is the reason it was named as quadruple sampling. After reset, V_{R1} and V_{P1} are sampled and the subtraction $(V_{R1} - V_{P1})$ is executed in analog domain; after integration, V_{R2} and V_{P2} are sampled and the subtraction $(V_{R2} - V_{P2})$ is executed in analog domain; afterwards the subtraction $[(V_{R2} - V_{P2}) - (V_{R1} - V_{P1})]$ is processed in digital domain. In this way all the frequency-related noise

can be removed, yet in the meanwhile more thermal noise of the source follower is added. The effective photo signal and noise can be written as

$$V_{3T,QS} = (V_{P1} - V_{P2}) - (V_{R1} - V_{R1}) \quad \text{(Eq. 2.10)}$$

$$n_{3T,QS} = \sqrt{4{n_{sf,t}}^2} \quad \text{(Eq. 2.11)}$$

2.2.2.4 Correlated Multiple Sampling

From the aforementioned discussion, it can be concluded that the source follower is the main noise source after the subtraction. To further reduce this part, correlated multiple sampling was introduced [56], with which both the reset signal and the photo signal will be read out many times. For 4T-APS, by applying the gain amplifier, all the sampling, subtraction and addition can be carried out in analog domain [28], Fig. 2.10 manifests the timing diagram, where the reset signal samplings and photo signal samplings have

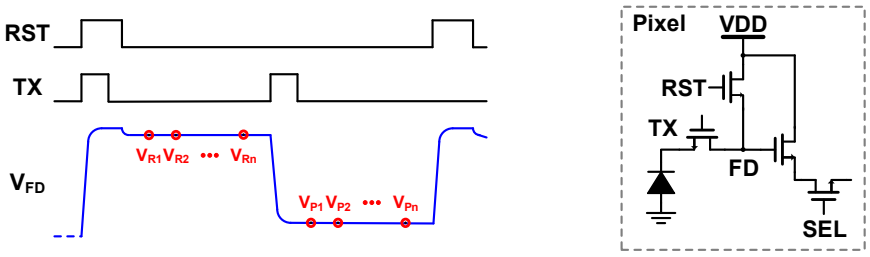

Figure 2.10: Timing diagram of the correlated multiple sampling for 4T-APS.

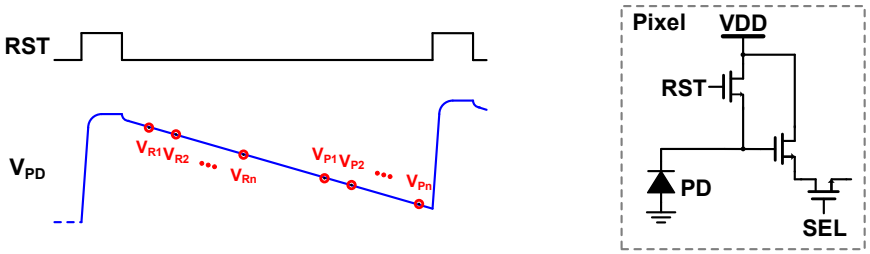

Figure 2.11: Timing diagram of the correlated multiple sampling for 3T-APS.

the fixed time interval. This method can also be explored in 3T-APS, as shown in Fig. 2.11, similarly to quadruple sampling, the sampled reset signals and photo signals need to be read out and quantized separately. The effective photo signal can be expressed as

$$V_{4T,CMS} = \sum_{i=1}^{n} (V_{Ri} - V_{Pi}) \qquad \text{(Eq. 2.12)}$$

where n is the sampling number of each voltage. By correlated multiple sampling, the noise from the RST transistor can be removed. Moreover, it enlarges the effective signal by n times, so that the thermal noise of the source follower can be decreased by $\sqrt{n}$ times, while the reduction factor of frequency-related noise depends on the readout circuits and operations [28, 51].

2.2.3 Column-Parallel ADCs

From the global buffer [31], multi-channel buffers [32], global ADC [57, 58], multi-channel ADCs [33], to column-parallel ADCs [59], the output technologies are well developed, and nowadays, the column-parallel architecture becomes the mainstream method. In this part, the review of the column-parallel readout circuits is elaborated on in detail. Currently, there are various kinds of architectures in use for column-parallel ADCs in CMOS image sensors, for instance, single-slope ADCs [60–62], successive approximation register (SAR) ADCs [63–65], cyclic ADCs [66–68], and Σ-Δ ADCs [69–72]. In this part, the column-parallel ADCs are reviewed in great detail.

2.2.3.1 Single-Slope ADCs

Single-slope ADCs employ the linear search protocol, which is similar to the flash ADC, but have the voltage references to come in serial. Fig. 2.12 shows the 3-bit linear search protocol and the block diagram of a column-parallel single-ramp single-slope ADC array.

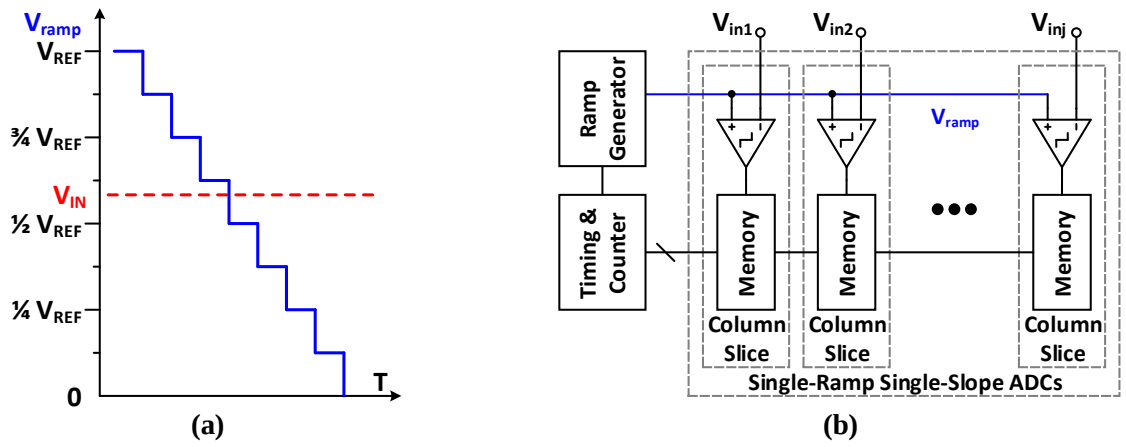

Figure 2.12: (a) 3-bit linear search protocol, (b) Block diagram of a column-parallel single-ramp single-slope ADC array.

The ramp generator and timing circuit are placed globally, while broadcasting the ramp voltage and digital timing signals to all the column slices. Each column slice contains a comparator and a set of digital memories. In regard to a single column, during operation, once the ramp voltage falls below the input voltage, the comparator will toggle and trigger the memory to store the current timing data. It is obvious that since the conversion time is long, and a n-bit A/D conversion will take 2^n cycles, it will limit the sensor readout speed and frame rate.

To overcome the long conversion time of the single-ramp single-slope ADCs, multi-ramp architecture was proposed [61]. The block diagram works similarly to the single-ramp one, but the difference lies in the fact that one column slice would execute two comparison steps for one conversion: the first one is used to compare the input voltage with a coarse ramp with the whole voltage range to make decisions on the MSBs and choose a fine ramp with suitable sub-range; and the second one is to compare the input voltage with the selected fine ramp and decide the least significant bits (LSBs).

However, to broadcast the fine ramps, the multi-ramp architecture would require more ramp generators and buffers, both of which would also consume much power. So another

two-step solution was proposed to decrease the power consumption [62]. Similarly, the first one is coarse comparison, once the comparator is triggered, a differential analog signal would be stored in a capacitor in a given column slice. In the fine comparison, only one fine ramp is required, and the sum of the capacitor voltage and fine ramp would be compared with the input signal. Thus, both of the conversion time and power consumption are reduced. Due to the simple structure, the single-slope architecture can achieve a small-area column slice with both small pitch and short length, so it is widely used in industrial applications [73–76].

2.2.3.2 SAR ADCs

To further reduce the conversion time, SAR ADCs with binary search protocol are also applied. Fig. 2.13 illustrates the 3-bit binary search protocol and block diagram of a SAR ADC. Differing from the single-slope ones', the voltages of SAR ADCs for comparison are generated within each column slices, normally by a switched-capacitor array. With binary search protocol the first MSB is decided in comparison with $1/2V_{REF}$ firstly; and following the comparison result, the second DAC voltage is generated by the capacitor

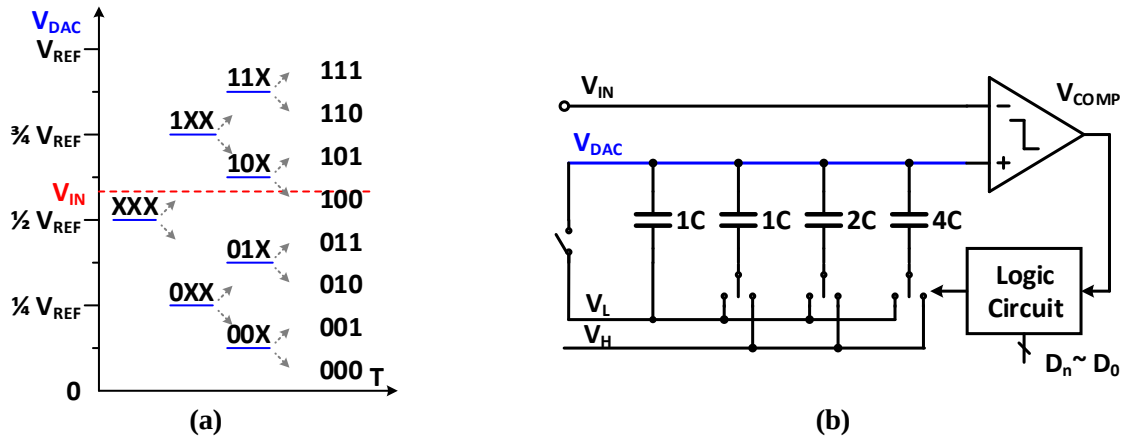

Figure 2.13: (a) 3-bit binary search protocol, (b) Block diagram of a SAR ADC.

array, 0 leads to $1/4V_{REF}$ and 1 leads to $3/4V_{REF}$; and then the second comparison is carried out to determine the second MSB. Following this principle, a n-bit A/D conversion only takes n cycles.

However, considering the capacitor array, n-bit SAR DAC would need 2^n unit capacitors, which will occupy quite a large area, and are difficult to be placed in a narrow column slice. Furthermore, the large capacitance would also consume more switching power and lead to larger mismatch. So the split-capacitor structure is employed to balance the area consumption, power consumption and ADC resolution [65]. There are also some other DAC structures to improve the efficiency [63, 64].

2.2.3.3 Cyclic ADCs

Cyclic ADC provides another solution with small area for column-parallel scheme. Fig. 2.14 describes the block diagram of a typical cyclic ADC, which can be viewed as a single stage of a pipeline ADC. The operation is similar to the delta modulation: in the first loop, the input signal is sampled for comparison to decide the first MSB; in the second loop, depending on the ADC result D_i $(1 < i < n)$, the sampled signal will be doubled by the integrator and add $(D_i = 0)$ or subtract $(D_i = 1)$ the DAC output voltage; the new

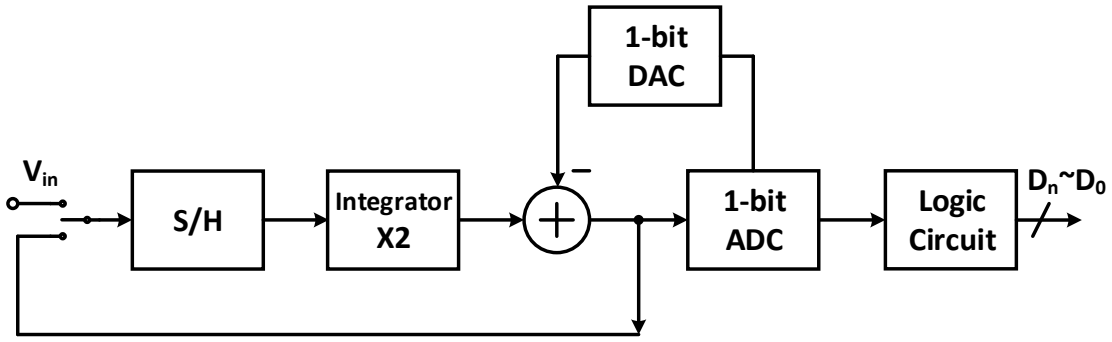

Figure 2.14: Block diagram of a typical cyclic ADC.

output voltage is then sent for comparison and sampled for a new loop. So the sampled voltage can be expressed as

$$V_i = 2V_{i-1} + sin\left[\left(\frac{1}{2} - D_{i-1}\right)\pi\right] V_{REF} \qquad \text{(Eq. 2.13)}$$

Naturally, the time cost of a cyclic ADC is similar to that of a SAR ADC, and the area consumption would not increase much with higher ADC resolution, thus this structure can be used in high resolution ADCs. In practice, the 1.5-bit ADC and DAC can be used to increase the efficiency [77] and the CDS can also be included into the integrator to simplify the operation and reduce the noise [78].

2.2.3.4 Σ-Δ ADCs

Differing from the three aforesaid ADCs of time domain, Σ-Δ ADCs can be treated one of frequency domain. Fig. 2.15 details the block diagram of the conventional Σ-Δ ADC. Assuming the input signal is a DC voltage, the ADC operates as follows: the integrator is ramping up or down, and drives the 1-bit ADC (comparator) to output "1" or "0"; the output of the 1-bit DAC, controlled by the 1-bit ADC, is added to the input signal as a negative feedback; the integrator is fed with the summed result. Due to the negative feedback, the average DAC output must be equal to the input signal. Since the DAC is controlled by the ADC, the input voltage can be calculated from the number of "1"s

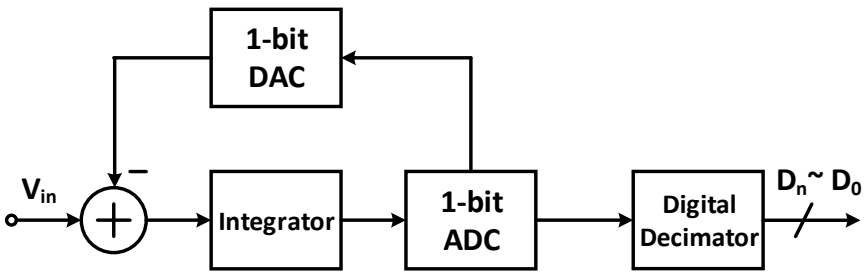

Figure 2.15: Block diagram of the conventional Σ-Δ ADC.

of the ADC output. Note that a single ADC output is meaningless here, only a large number of samples will come to a meaningful result. And generally speaking, to obtain n-bit resolution, 2^n clock cycles is needed. For the complicated operation and transform, the Σ-Δ ADCs are not as popular as the other architectures.

2.2.3.5 Lower-Power ADCs

For the applications such as remote imaging, mobile devices, wearable devices and biomedical devices, power consumption has become a serious concern, and plays an increasingly important part in limiting the image sensor performance with the increment of resolution [75]. Studies have shown that most of the energy in CMOS image sensors is consumed by the ADCs and digital output circuits [79]. An ADC is made up of components as comparator, DAC/amplifier, digital parts and other circuits, with differing power dissipation in each component. Thus, in order to reduce the power consumption, we may diminish the power consumption in each component or change the ADC structure or alternatively how it operates.

Recently, state-of-the-art ADCs were reported to have reduced the power consumption in CMOS image sensors. It is a common and useful way to reduce the power consumption by decreasing the power supply voltages of analog and digital circuits or only of digital circuits, which is also popular in bio-medical and other low power applications [80]. If the power supply cannot be reduced, e.g., an advanced fabrication technology is applied or high dynamic range is required, switched power technique would be alternatively an effective option, which powers off the components not in use [63, 81]. Since digital circuits account for a large proportion of the power dissipation, lowering the clock frequency would be also conducive to achieving lower power consumption [81]. Configuring the circuit operation may sometimes decrease the power dissipation, e.g., in [20, 64], only a small portion of the total capacitor array is used to decide the MSBs, by this means

the capacitor switching power is reduced henceforth. Multi-stage ADC proves to be another effective way to save power, e.g., in the two-stage cyclic architecture, the total power consumption can be reduced by scaling the size of the sampling capacitor of the second-stage [82]; in the single slope architecture, a two-stage ADC or a multi-ramp ADC can also reduce the power dissipation by shortening the total comparison times [62, 83]. Data compression is a recently developed theory, which recovers the photo signals from a number of random linear measurements in a transform domain [69, 71, 84]. Given the number of the measurements is smaller than that of samples dictated by the Nyquist rate, the compression can reduce the total power dissipation as well.

2.3 TDI Image Sensors

According to the introduction in Chapter 1, we are aware that in order to operate the TDI, additional pixel stages in the along-track direction is functionally required, which should be qualified to fulfill the following requirements:

(1) low-noise pixel readout and signal transfer path;

(2) on-chip additional circuit to carry out the TDI operation;

(3) synchronous image signal capture for all pixels in the along-track direction.

Both CCD and CMOS technologies can satisfy these aforesaid requirements. This section will show the typical TDI image sensor designs in detail.

2.3.1 CCD-Type TDI Image Sensors

The conventional TDI image sensors are implemented by the CCD image sensors, which are born TDI image sensors. Owing to the charge transfer and accumulate function, the CCDs can easily realize the TDI operation without the assistance of any other additional pixel readout path, signal transfer path or TDI operation circuit [1, 85, 86]. The only

difference between the frame-based CCD image sensors and TDI CCD image sensors lies: in the frame-based CCD image sensors, after one time exposure, all the pixels are read out; however in the TDI CCD image sensors, only the last stage of pixels are read out, while other pixels are transferred to the next stage in the along-track direction for future integration. Therefore, it only requires to modify the pixel timing controller. Nowadays, most of the commercial TDI image sensors are implemented applying CCD technologies, such as the products from Teledyne Dalsa, e2v, Schafter+Kirchhoff and so on, which can achieve high speed and therefore are widely used in industry applications.

In CMOS technologies, the TDI is more difficult to be implemented, the only exception being the 4T-APS with pinned photodiode (PPD), which shares the similar characterization to the CCD pixels. Fig. 2.16 illustrates the charge transfer operation in pinned photodiode in a CMOS technology [87]. 31 is the P^+ doping, under which the photo charge (36) is stored in the potential well (38); 32 and 34 are transmission gates controlled by the signals $\Phi 1$ and $\Phi 2$, respectively. By controlling the 32 and 34, deeper potential wells can be formed, so that the charge stored in the pinned photodiode can be transferred as the CCD operation. After the charge moving on to the last stage, it can be read out from the 4T-APS as the typical CMOS image sensor.

Nowadays, with advanced CMOS technologies, the CCD structure can also be integrated into a CMOS image sensor, which possesses the CCD pixels and CMOS readout circuits [88]. Thus, it proves to be a useful method to execute TDI function in CMOS technologies. However, only few processes can achieve these special structures, and furthermore the cost can be quite expensive. For most of CMOS technologies, supporting circuits are indispensable for fulfilling the TDI function. Regarding the TDI operation, after one time exposure, all the pixels will be read out for TDI operation or be transferred to the next stage in the along-track direction. For those operations, the low noise signal path is essential element. Since the output signal of CMOS pixel is voltage or current,

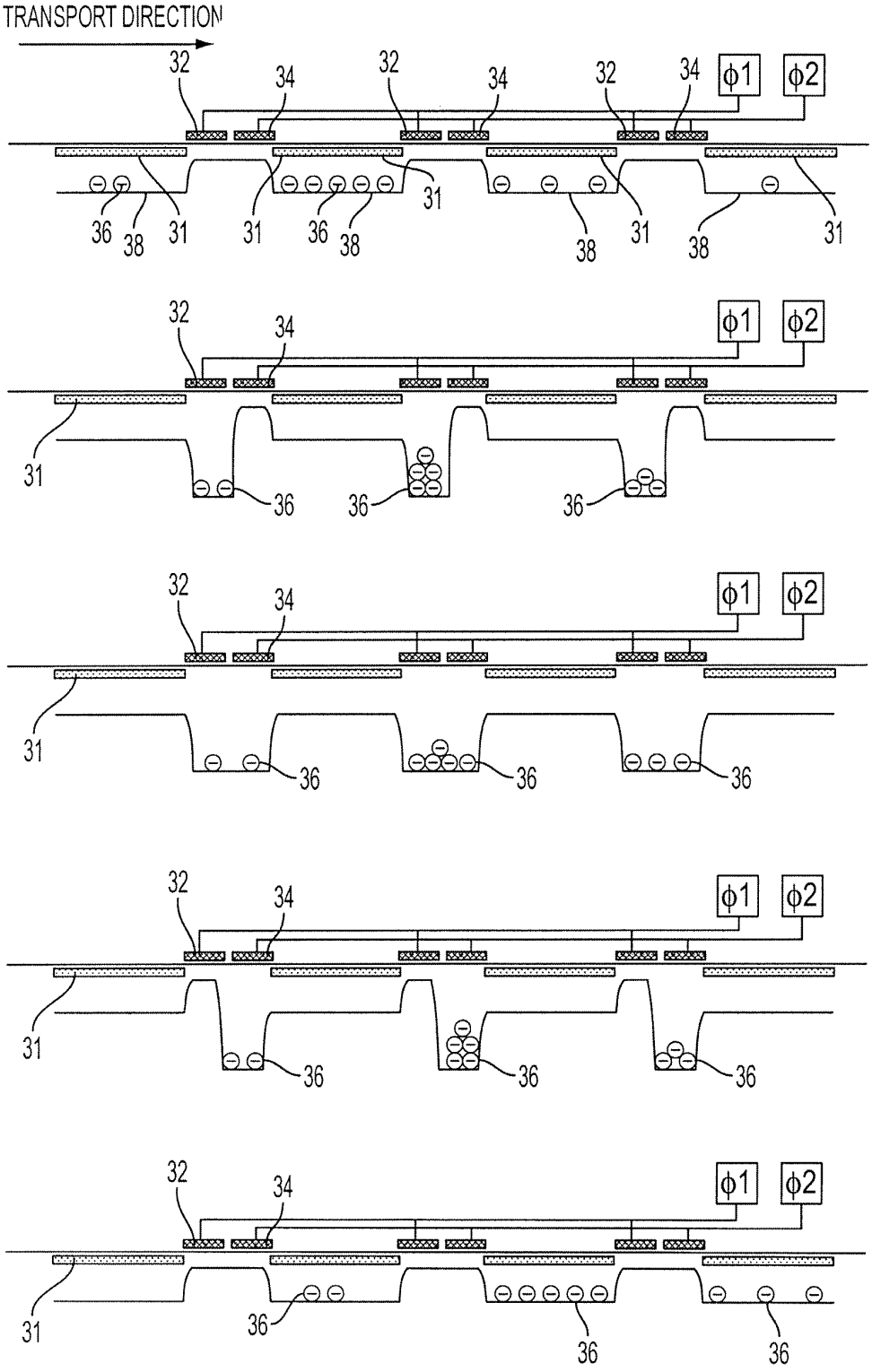

Figure 2.16: Charge transfer operation in pinned photodiode in a CMOS technology [87].

various circuits can be used to perform the TDI function. In the following part, the TDI CMOS image sensors will be introduced.

2.3.2 Pixel-Level TDI CMOS Image Sensors

In light of the function block where the TDI operation is performed, the TDI CMOS image sensors can be categorized into two groups: pixel-level TDI and column-level TDI. Among them the pixel-level implementations can be further divided into adjacent pixel signal transfer and detector-to-storage switch. Their difference lies in the fact that each photo detector possesses its own signal storage in adjacent pixel signal transfer architectures [89–92], while a detector would be assigned a new switched storage after each stage integration in detector-to-storage switch architectures [93–95].

2.3.2.1 Adjacent Pixel Signal Transfer

From the mechanism point of view, the adjacent pixel signal transfer runs probably the same route as the way with the TDI operation in CCDs [89–92]. In this architecture, the photo signals are transferred in the along-track direction, and each pixel would do integration based on the previous stage integration result. The photo signals can be transferred in the forms of charge or voltage.

Fig. 2.17(a) shows the unit cell schematic of a TDI CMOS image sensor with adjacent pixel charge transfer [89]. It consists of a differential amplifier, an integration capacitor, a reset switch, transfer switches, loop open switches, detector open switches, and a dead pixel elimination (DPE) circuit. There are three operations in one TDI cycle, as shown in Fig. 2.17(b)(c)(d):

(1) Reset: by turning on $P_{RST,H}$ and off M_{ON}, P_{LOOP}, $P_{TRAN,H}$, the integration capacitor $C_{INT,n}$ is reset by the amplifier, and the stored charge would be cleaned.

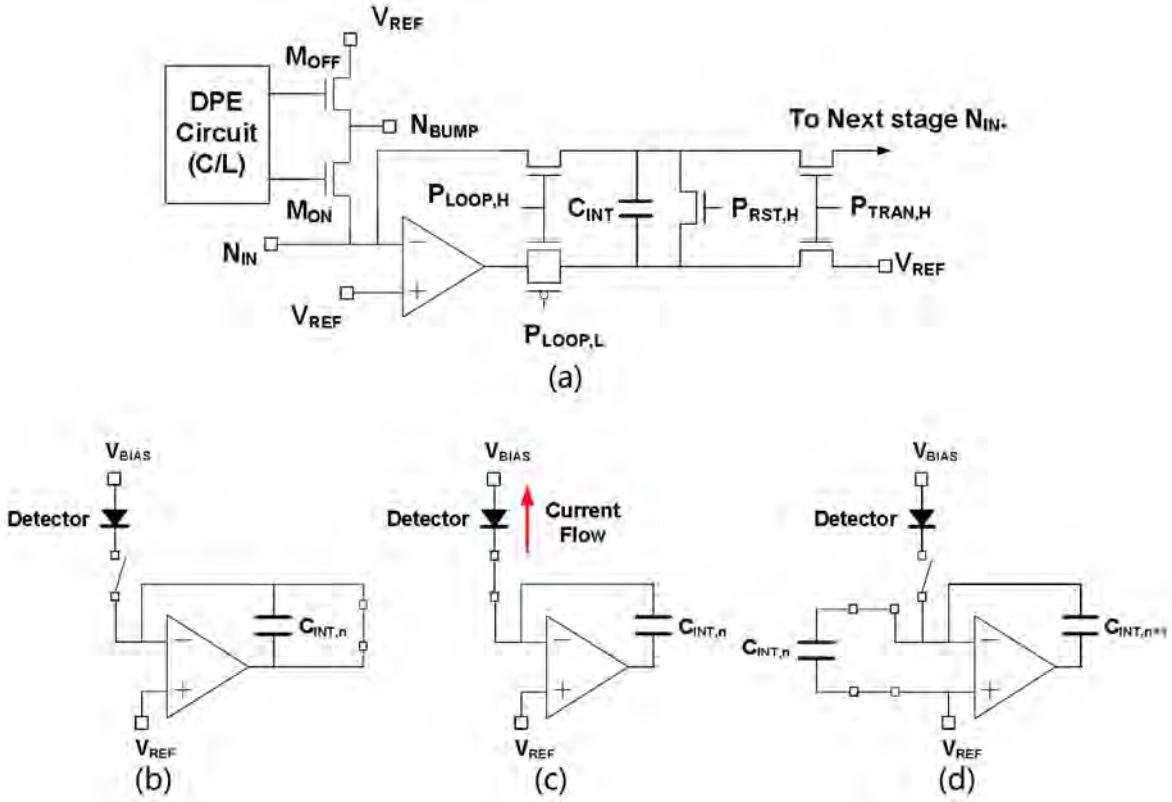

Figure 2.17: (a) Pixel unit schematic of a TDI CMOS image sensor with adjacent pixel charge transfer, (b) reset operations, (c) integration operation, (d) charge transfer operations [89].

(2) Integration: by turning on M_{ON} and off P_{LOOP}, $P_{RST,H}$, $P_{TRAN,H}$, the photo current would be integrated into $C_{INT,n}$.

(3) Charge Transfer: by turning on $P_{TRAN,H}$ and off M_{ON}, P_{LOOP}, $P_{RST,H}$, the photo charge in $C_{INT,n}$ would be transferred to $C_{INT,n+1}$, before which the charge in $C_{INT,n+1}$ has already transferred to $C_{INT,n+2}$. Therefore the charge stored in the last integration capacitor has gone through all the TDI stages, finished the integration, and will be read out.

The DPE part would only control the detector open switch to reduce the negative effect of the dead pixels to the final image. This architecture is similar to the CCD method, with the difference being that the charge transfer relies on the supporting circuits, and

the amplifier and switches would induce thermal noise, flicker noise and FPN in every signal transfer. In contrast, in CCDs no circuits are needed, the charge packet can be easily transferred to the next stage without noise added. Moreover, the above-mentioned design would suffer from large area and high power consumptions.

The photo signal can also be transferred in voltage. Its principle is as simple as to transfer the photo signal voltage from one pixel to its neighboring pixel of the same column in the along-track direction [91]. The transfer operation is carried out by a shared unity-gain buffer or pixel-owned buffers. Fig. 2.18 illustrates the architecture diagram of a TDI CMOS image sensor with adjacent pixel signal transfer. It is comprised of four parts: interlaced APS pixel array, column-shared unity-gain buffer, column-parallel CDS circuits, and digital control circuit. In the pixel array, the pixels are not routed as the normal APS pixels, as that shown in Fig. 2.4 or Fig. 2.5, but configured by the following methodology: the output of the pixel is connected to the input of the unity-gain buffer, and the output of the unity-gain buffer is connected back to the pixel acting as the reset voltage. The unity-gain buffer is column-shared, therefore, the input and output can go to any pixels.

The TDI operation procedure is described as follows: assume the process originate from the integration, during which, the photo charge is accumulated in the pixel. After integration, the last stage of pixels, i.e. *Pixel* (16, 1) is read out, then the *Pixel* (16, 1) is reset by the signal voltage from *Pixel* (15, 1) through the column-shared unity-gain buffer. The similar operation will be carried out from *Pixel* (16, 1) to *Pixel* (2, 1), then the *Pixel* (1, 1) will be reset by the power supply. Afterwards the pixels will start a new integration based on the voltage signals from the previous stage. It is similar to the charge transfer method, with the difference being the signal is transferred as voltage. Similarly, the column-shared unity-gain buffer and switches will also introduce thermal noise, flicker noise and FPN in each stage.

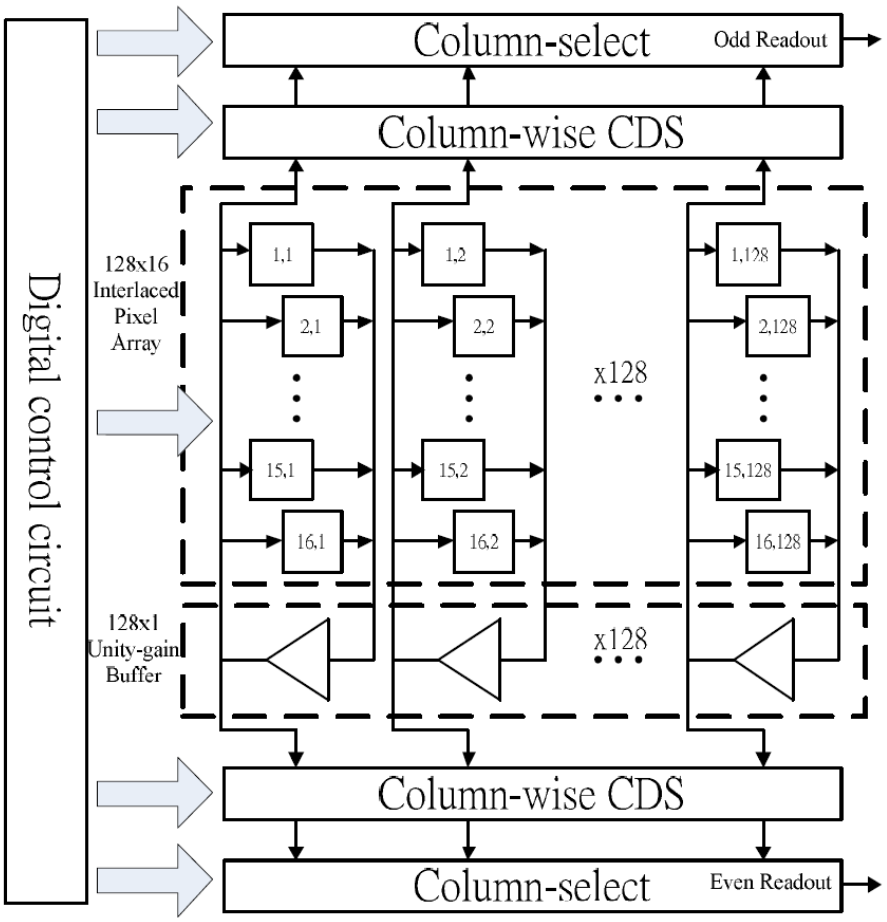

Figure 2.18: Architecture diagram of a TDI CMOS image sensor with adjacent pixel signal transfer [91].

2.3.2.2 Detector-to-Storage Switch

Generally, as a result of the limitation of the silicon properties, the CCD and CMOS image sensors are merely sensitive to visible light. While the infrared image sensors require to fabricate the photo detector separately using special materials other than silicon, i.e. GaAs, and use the standard CMOS process to implement the readout circuits. In this case, the detectors usually do not store the charge, and the detectors and storages are separated into two chips. So the photo signal is transferred as current between chips. For these applications, the TDI function is implemented by switching the serial photo

currents in the same column to charge a same integration capacitor. Although the TDI circuit is physically separated from the photo detector, functionally, they belong to one pixel. Normally, a front-end circuit would be inserted between the detector and storage to decrease the output impendence and compress the noise, such as direct injection (DI) [93, 96], buffered direct injection (BDI) [94, 95, 97] and capacitive trans-impedance amplifier (CTIA) [98, 99].

Fig. 2.19 depicts a TDI architecture applying BDI methodology [94]. The circuit contains four infrared photo detectors in one column, four BDI circuits for each photo detector, four cell-failure control (CC) circuits, a switch box integrated circuit (SBI), and a four-to-one multiplexer. The OP-AMP ($gain = A$), connecting from the photo detector to the common-gate NMOS, is able to decrease the input impedance by A times because of the negative feedback. Thus the injection efficiency (injection ratio) is accordingly increased. The cell-failure control circuit are capable of cutting off the photo

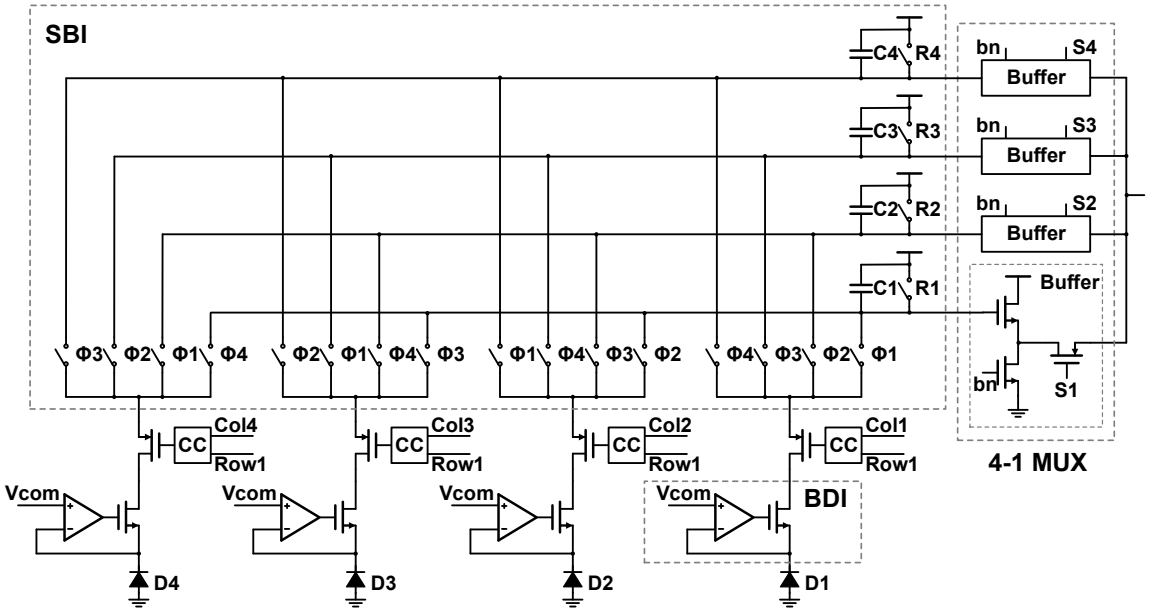

Figure 2.19: Signal path schematic of a TDI CMOS readout circuit with buffered direct injection unit cell.

current path and stopping the integration if faults happen to occur in the photo detector. The switch box integrated circuit is for the purpose of detector-to-storage switching and photo signal accumulating. After four time integrations, the summation of the charge on a single capacitor will be converted to a voltage signal, and then be read out through the multiplexer.

The detector-to-storage switch scheme consumes a great number of switches and capacitors, therefore a large area consumption, cross-die variation and mismatch cannot be avoided. In addition, the complex routing imposes constraint on the pitch of the circuit, making it difficult to achieve a high resolution.

2.3.3 Column-Level TDI CMOS Image Sensors

Unlike the pixel-level TDI architectures, the column-level solutions normally enjoy the standard APS structure, that means the pixel arrays share the same structures as the frame-based CMOS image sensors, and the TDI function is realized in column-level accumulation circuits which are usually implemented by gain amplifier. According to the usage of OP-AMP, the accumulator can be divided into separate structure and united structure. By separate means, each TDI stage would be equipped with a full-functional gain amplifier, including an OP-AMP and an integration capacitor [100–102]; on the contrary in united cases, all the TDI stages enjoy their own TDI integration capacitor but share one OP-AMP, and the detector-to-storage arrangement depends on the switches [103–106].

2.3.3.1 Separate TDI Accumulators

Fig. 2.20 shows the signal path schematic of a TDI CMOS image sensor with separate column-level TDI accumulators [101]. The 3T-APS is applied, of which the output is tied to the column bus. The column slice includes biasing circuit, amplifier, CDS and

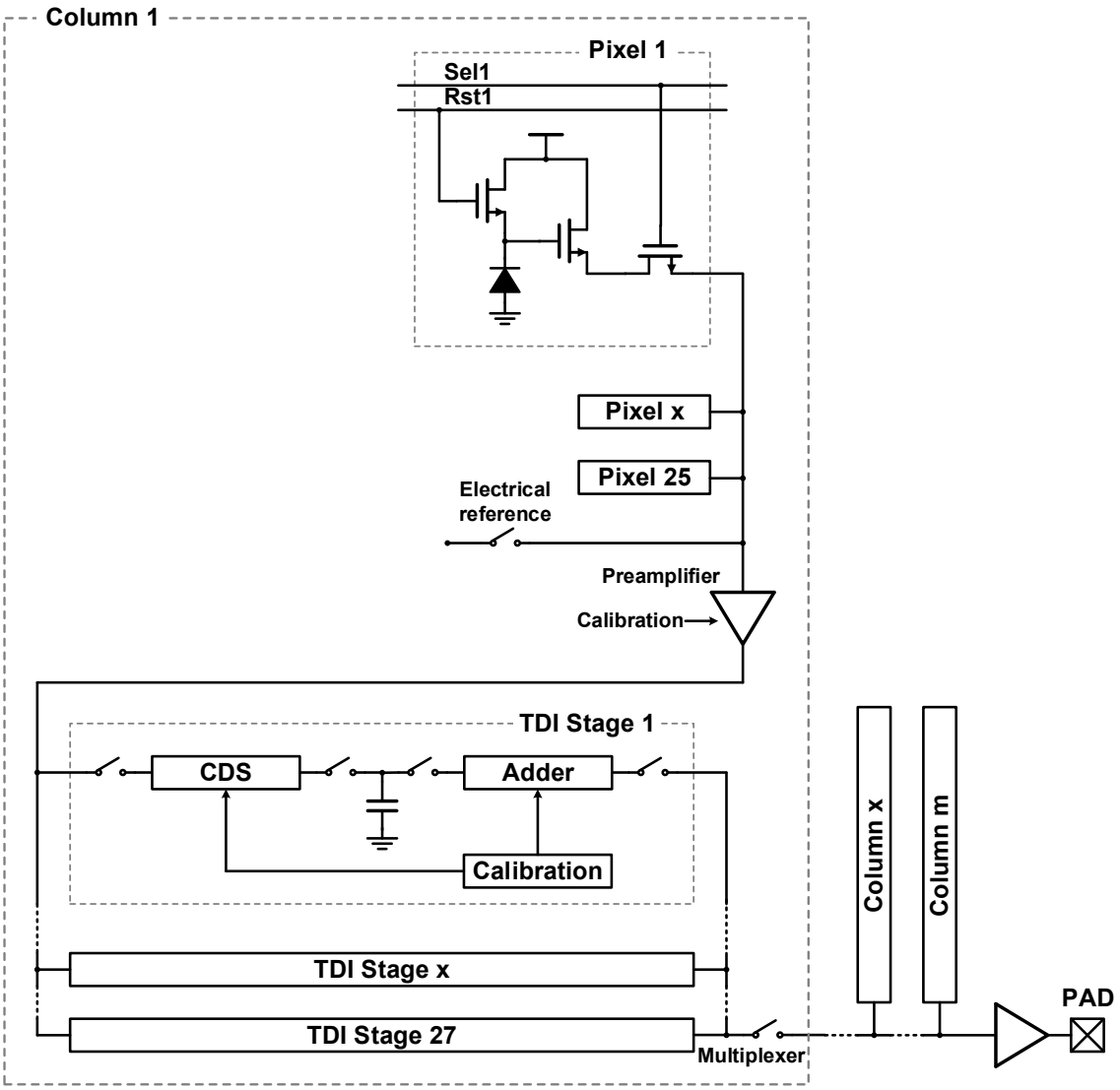

Figure 2.20: Signal path schematic of a TDI CMOS image sensor with separate column-level TDI Accumulators.

accumulator. After exposure, the photo signals would be read out through the column bus to a corresponding TDI stage following the protocol that the photo signals caused by the same object go to the same TDI stage. If one TDI stage has collected the photo signals from all the pixels in the same column, it will be read out through the multiplexer and output driving buffer. Since each TDI stage contains a separate CDS and accumulator circuits, the area and power consumption would be very high. And the mismatch among

the stages should be taken into consideration due to the long stripe placement.

2.3.3.2 United TDI Accumulator

Fig. 2.21(a) shows the signal path of a TDI CMOS image sensor with on-chip analog accumulators [104]. The middle part is the analog accumulator, which contains a fully-differential OP-AMP, a set of sampling capacitors C_S, several complementary switches, and 33 groups of holding capacitors from C_{h1} to C_{h33}. Among the aforesaid elements, the fully-differential OP-AMP is used to carry out the CDS operation for noise cancellation, such as common-mode noise, including clock coupling, ground noise, and charge injection. The time-invariant voltage source V_{OS} is used to model the equivalent input offset voltage of the fully-differential OP-AMP, which stems from the process variation and mismatch. The on-chip analog accumulator is functionally like a multi-stage switched-capacitor integrator, which includes 33 stages to suit the 32-stage CMOS TDI image sensor. Each pair of holding capacitors constitutes a TDI stage in the accumulator.

Fig. 2.21(b) gives the timing diagram of the on-chip analog accumulator, where $T_{nonoverlap}$ is the non-overlap period of the two-phase non-overlap clock $clk1$ and $clk2$. $clk1'$, $clk2'$, lx', and $Resetx'$ ($x \in [1, 33]$) are the same as $clk1$, $clk2$, lx, and $Resetx$, but are designed slightly advanced to avoid the charge injection. Taking the first stage for example to explain the TDI operation: when $clk1 = 1$, $clk2 = 0$, $lx = 0$, and $Resetx = 1$, the first stage of the accumulator is in the first sampling phase. During this period of time, the output of the OP-AMP is the common mode voltage, and the pixel reset signal V_{rst} and the OP-AMP's input-referred offset V_{OS} are sampled in C_S. Meanwhile, the pair of C_{h1} are reset by connecting the top plates to the OP-AMP's outputs and the bottom plates shorted. When $clk1 = 0$, $clk2 = 1$, $lx = 1$, and $Reset_x = 0$, the first stage of the accumulator is in the holding phase. The positive input of the accumulator is the photo signal V_{sig}, hence the charge $(V_{rst} - V_{sig})$ C_S is transferred from C_S to C_{h1}. Then

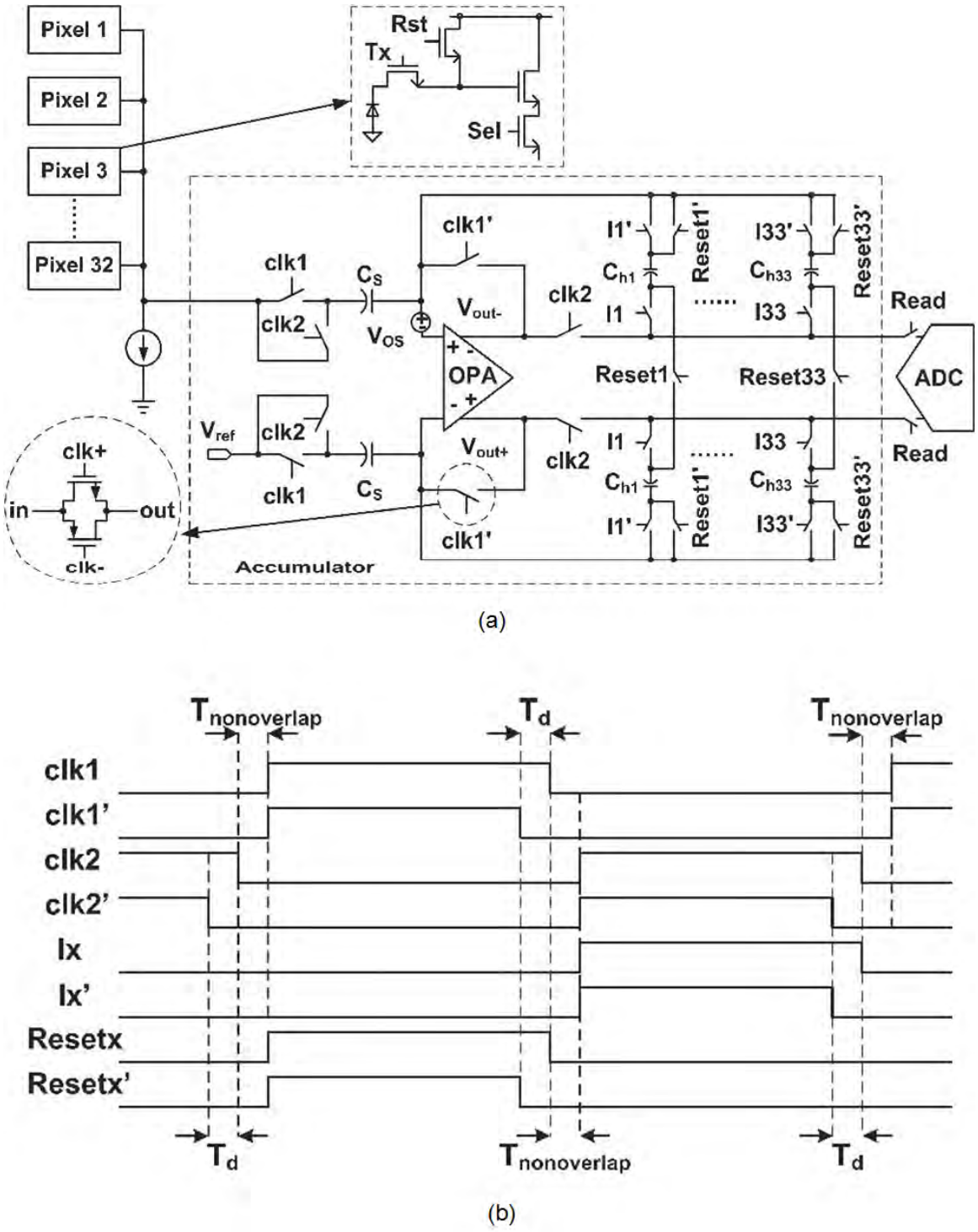

Figure 2.21: (a) Signal path of a TDI CMOS image sensor with on-chip analog accumulator, (b) Timing diagram of the on-chip analog accumulator [104].

$$V_{out-} - V_{out+} = \frac{C_S}{C_{h1}} (V_{rst} - V_{sig}) \quad \text{(Eq. 2.14)}$$

After n stage integration, the output of the accumulator should be

$$V_{out-,n} - V_{out+,n} = V_{out-,n-1} - V_{out+,n-1} + \frac{C_S}{C_{h1}} (V_{rst} - V_{sig}) \quad \text{(Eq. 2.15)}$$

Throughout the whole operation, the accumulator can realize the TDI function. To increase the TDI stage number, only adding integration capacitors and corresponding switches is enough, but it would increase the parasitic capacitance. Moreover, higher DR requirement would lead to larger capacitor area.

2.3.4 Digital-Domain TDI CMOS Image Sensors

All the above-mentioned TDI implementations work in analog domain, besides, the digital domain addition also provides a solution for TDI function. After each time integration, the photo signal would be quantized and output to an on-chip processer, an off-chip processer or a computer. The A/D conversion can be carried out in pixel level [107, 108], column level [109] and even chip level.

Fig. 2.22 shows a TDI CMOS image sensor architecture diagram applying digital output pixel [107]. Through the sensor alone contains a two-dimensional pixel array, control circuits and digital readout circuit, yet the pixel enjoys a complicated structure, for in the pixel, the photo current from photodiode is integrated into an effective capacitor C_{int}, which consists of gate capacitance, diffusion capacitance and interconnect parasitic capacitance in the integration node. A comparator is inserted to monitor the voltage of the integration node, once it reaches to the threshold voltage, the comparator will trigger the reset circuit to reset the photodiode and integration capacitor for a new integration, and also trigger the counter to add one bit. This type of ADC is named as pulse frequency modulation (PFM). After the conversion, the digital data can be easily transferred and processed, with only an additional operation realizing the TDI function.

The counter in the pixel can also be changed into memory. The integration and an off-pixel-array counter start to work at the same time, when the integration node reaches the threshold voltage, the comparator will trigger the memory to write down the counter value. And this operation is called as pulse width modulation (PWM) [110]. Both PFM and PWM can be implemented in use for TDI, however, they suffer from the following drawbacks. Firstly, the large pixel size (normally $20 \sim 30$ μm pixel pitch) restricts the whole sensor resolution; secondly, the effective integration time is too long to be suitable for TDI's fast integration; the third one is that the cross-die mismatch will cause variations to the effective integration capacitor and input-referred offset to the comparator, which will all significantly have negative impact on the sensor's DR.

A column-level design was also proposed in Ref. [109], in which the TDI function is carried out by using column-parallel ADCs, memories and digital adders, and the architecture is like the normal frame based CMOS image sensor. After each integration,

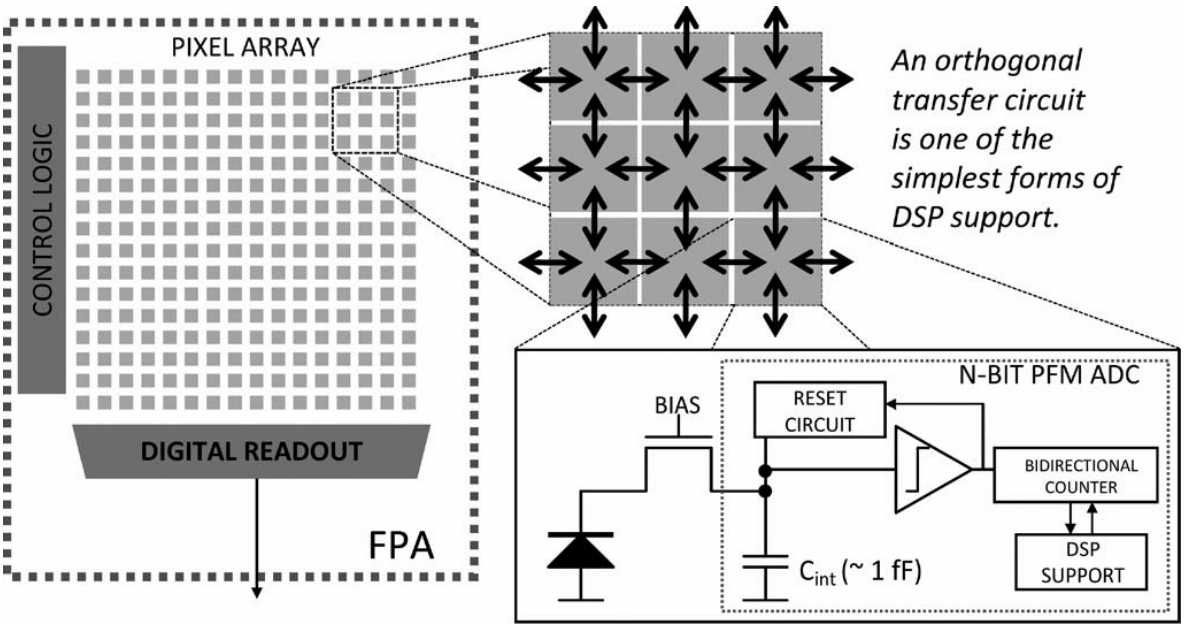

Figure 2.22: Architecture diagram of a TDI CMOS image sensor with digital output pixel [107].

the ADCs will digitize the photo signals, and the results are added to the previous results followed by being stored into the memories. Once the TDI is finished, the digital results would be shifted out. Apparently, the digital addition can be executed off-chip, thus all the frame-based sensors can work as digital-domain TDI sensor. However, it is a big challenge for the ADCs, the ADCs must achieve ultra-low noise and ultra-high linearity, otherwise the TDI would be meaningless without the improvement of DR or SNR.

2.4 Issues and Solutions in Spaceborne TDI Systems

2.4.1 Problem of Vibrations

TDI has well adopted imaging in many forms, including multi-spectral satellite imaging, global environment monitoring, military reconnaissance, industrial online product inspection, X-ray non-destructive detection, document scanning and multimedia dis-

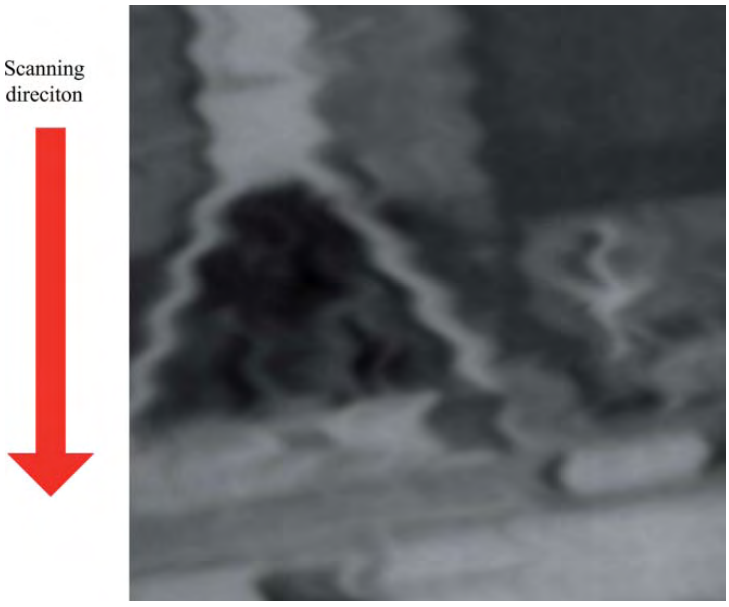

Figure 2.23: An example of distorted and blurred image [111].

play [112–116]. In respect of any of the applications mentioned above, the TDI camera must follow a rule that the camera motion and the traveling of the photo signal on the focal plane shall be synchronized altogether, and that the forward moving direction should be perfectly crosswise to the TDI pixel stages, otherwise the TDI image quality will be destroyed by the residual motion, as shown in Fig. 2.23. Residual motion refers to the motion in the across-track direction that distorts and blurs the image, and it excludes the along-track scanning motion in the TDI camera's mechanism [111]. It widely exists in the TDI camera systems, especially in the remote imaging systems.

Maintaining the attitude of the TDI camera mechanically stable throughout the scanning is the most effective solution to retain high image quality. Fig. 2.24 illustrates an advanced thin film transistor liquid crystal display (TFT-LCD) array automatic optical inspection system developed by Favite Inc. The TDI cameras are mounted to rigid supporting frames and moving in a stationary rail, thus no extra residual motion would be

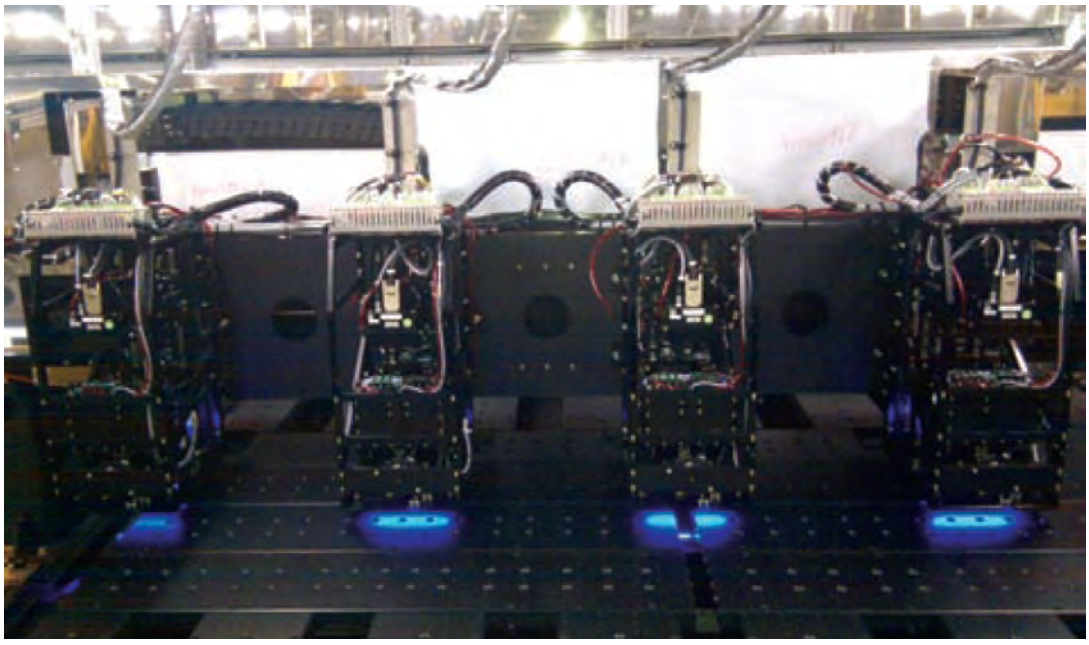

Figure 2.24: Thin film transistor liquid crystal display (TFT-LCD) array automatic optical inspection system developed by Favite Inc [117].

generated therein, and then high image quality can be achieved [117].

Unfortunately, in absence of any fixture to be used, the satellites are "floating" following the orbit in space, and in suffering random disturbances, which can cause the satellites to vibrate and even bring about residual motion in the across-track direction. These non-idealities have complicated mechanisms, with the main sources summarized as follows.

(1) According to the open date of LANDSAT-4 provided by NASA/GSFC [4] and OLYMPUS satellite provided by ESA [5], the random disturbances consist of a large number of harmonic vibrations. These vibrations appear in sine wave with the frequencies concentrated less than 500 Hz.
   (a) The main harmonic vibration is approximately pegged at $1 \sim 2.2$ Hz, caused by solar panel tuning.
   (b) The reaction wheel (momentum wheel) also contributes resonance effects at $100 \sim 200$ Hz in between the rotation speed adjustment.
   (c) The motor and motorized pumps would trigger harmonic vibrations at hundreds Hz as well.

(2) Satellite orbital drift, spacecraft attitude adjustment, earth's rotation and ground relief errors would lead to low-frequency vibrations [6].

(3) Bi-directional mirror scanning would cause the high-frequency jitters [118].

(4) Adjustment of the orientation angles or the orbit perturbations would also result in vibrations, and sometimes the effective substantial motion swing is larger than the pixel size [119].

(5) Moreover, jet blast and pointing control have contributions to the disturbance [7].

In a remote TDI image sensing system, the aforesaid random disturbances would result in residual motion in the across-track direction and further leads to blurred and distorted images. A large quantity of works have been reported to upgrade the image quality, in this part, the representative solutions would be given due attention in detail.

2.4.2 Mechanical Vibration Compensation

Mechanical compensation is a point black solution to compensate for the vibrations. Under normal circumstances, big satellites are equipped with active vibration control system, a means of attenuating unwanted on-board vibrations, as an alternative to passive vibration absorbers [7, 120–123]. The basic principle of the active vibration control lies in a negative feedback system, of which the operation diagram is described in Fig. 2.25 [121]. Sensors are placed to detect the vibrations, and send the vibration signals to the controller; followed by the controller would cause the actuator to produce vibration responses to enhance the system stability.

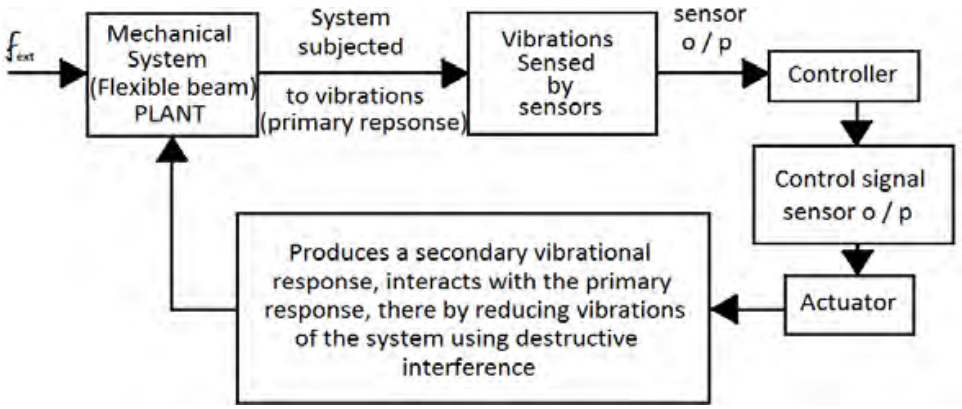

Figure 2.25: Operation principle of an active vibration control system [121].

In Ref. [7], a pair of piezoelectric sensor and piezoelectric actuator are used to compensate for the vibrations. When a disturbance occurs, the piezoelectric sensor will sense the motion, and convert the mechanical vibrations to electrical signals, which will be sampled and processed by the signal processing system, and sent back to the piezoelectric actuator to adjust the attitude.

However, small satellites usually do not enjoy this benefit due to limited volume, weight and power. For instance, nano-satellites are miniature satellites that typically

only keep the weight around $1 \sim 20$ kg, and total power capacity approximately $20 \sim 50$ Watt, thus an active vibration control system might look like too much for them.

2.4.3 Optical Vibration Compensation

In the similar protocol, the optical compensation to the imaging system proves to be another method to reinforce the image quality, which is normally achieved by changing the relative position of the focal plane and lens, rotating the optical wedge and reflection mirror [124–126]. Fig. 2.26 details the block diagram of an optical compensation system. Here the motion sensor (a small resolution image sensor) works in a high speed with short exposure time, by contrast to the main image sensor works in normal speed. The detected image motion data can be obtained from the optical correlator in real-time, and sent back to control the piezoelectric actuator, which would adjust the movable focal plane accordingly. Thus in this way the image motion can be compensated. Apparently, the system cost with optical compensation is still not affordable for small satellites.

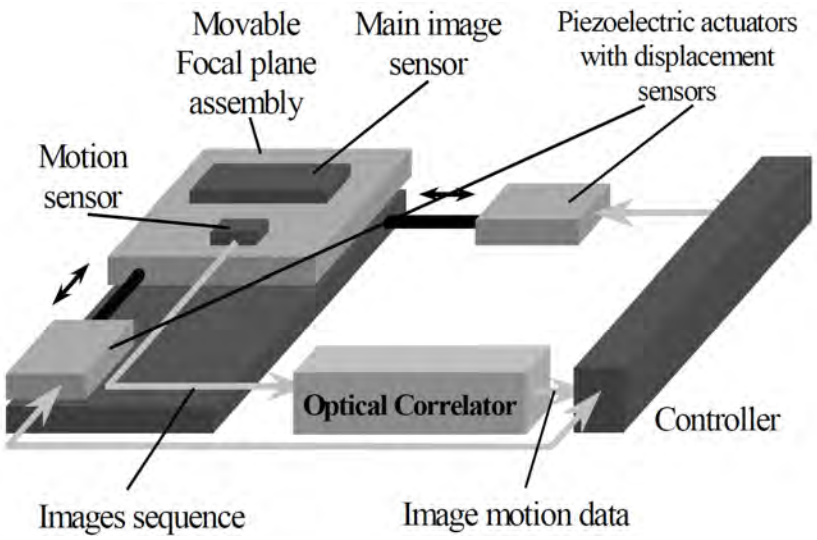

Figure 2.26: Block diagram of an optical compensation system [124].

2.4.4 Electrical Vibration Compensation

Given adjustment of the focal plane can compensate for the image motions, another electrical method aimed at the CCD frame-based image sensors was introduced without flexible components [127–129]. As discussed in Section 2.1, the signal output of CCD image sensors is accomplished by charge transfer, which happens to be the basic mechanism of the CCD TDI image sensor. This is considered to be a possibility to move the photo charge packets in frame level. Fig. 2.27 presents the concept of the forward motion compensation (FMC) implementation on a CCD image sensor [127], with the similar system architecture to Fig. 2.26. The pixels are divided into column groups, with each group maintaining its own separate control signals. Once receiving the image motion data, the pixel control signals would be adjusted to drive the charge packets to move following the image motion. As such the image motion can be compensated. But this solution is only designed for the CCD image sensors, rather than suitable to the CMOS image sensors.

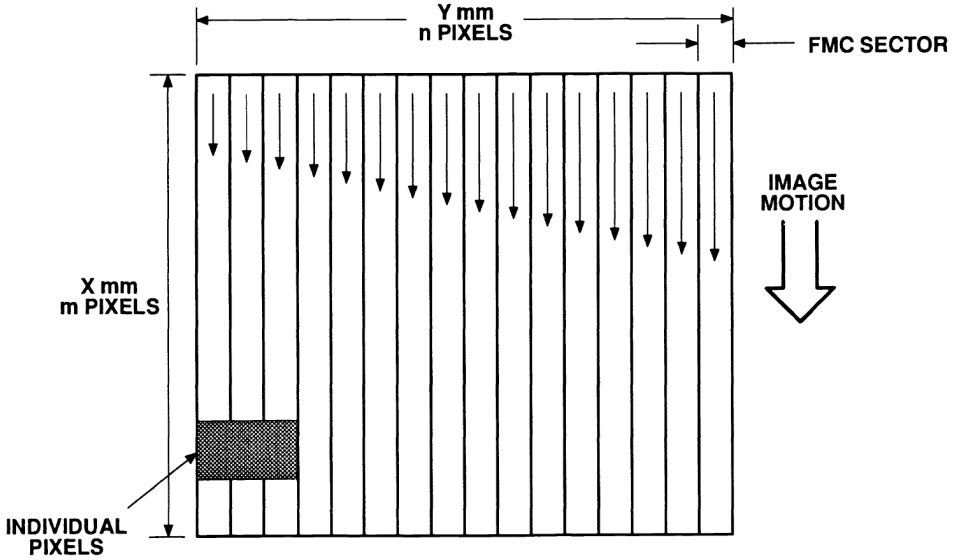

Figure 2.27: Concept of the forward motion compensation implementation on a CCD image sensor [127].

2.4.5 Post Image Processing for Vibration

To overcome the platform hindrance, more research efforts are also put in the area of image post processing. The popular solutions, motion blurred image restoration, can be mainly classified into two categories: non-blind deblurring [130–134] and blind deblurring [135–138]. The difference between them lies in the motion blur kernel or point spread function (PSF), which can be known or computed in non-blind cases, and unknown in blind cases.

In scenario of non-blind image deblurring, the motion blur kernel or PSF need to be obtained from elsewhere, e.g., an extra assistant imaging system. Fig. 2.28 illustrates a hybrid imaging system for non-blind deblurring [133]. The light from the object is reflected by the *plane mirror* 1, and converged onto the focal plane by the objective lens. Two cameras, one TDI camera and another high speed camera, are both placed on the equivalent focal planes A and B. Part of the light reflected by *plane mirror* 2 directs to the TDI camera, while, the rest light is reflected by the *plane mirror* 3 and directs to the high speed camera. Then the TDI image can be achieved by the TDI camera, and the motion trajectory can be recorded by the image sequence captured by the high speed camera. Afterwards the blur motion kernel and PSF can be calculated from the corresponding motion trajectory using fast Fourier transforms (FFT) [139]. Finally the image restoration can be carried out applying suitable algorithms, such as Richardson-Lucy (RL) deconvolution [131] and Wiener filtering [130].

While the blind image deblurring is usually initialized with an estimate kernel, for instance Gaussian kernel [135] and wavelet transform [136, 137], based on which, the motion blur kernel is calculated. Thus the noise could be a worse scenario in blind cases. Generally speaking, non-blind image deblurring can achieve higher accuracy than blind cases owing to noise and ring artifacts. However, non-blind cases require the assistance of

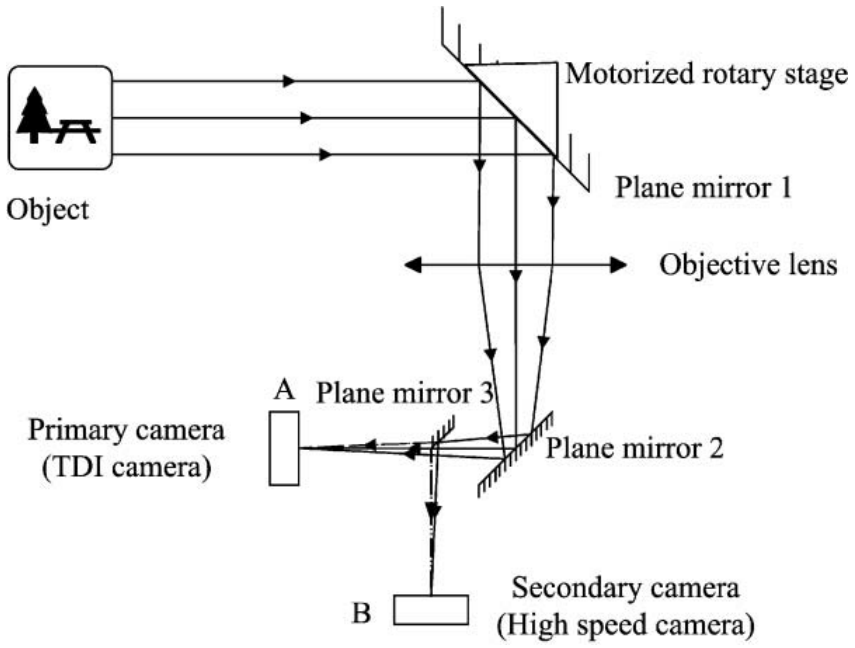

Figure 2.28: A hybrid imaging system for non-blind deblurring [111].

extra imaging system and even complicated optical system with heavy weight and large volume, which is why they are not suitable for small remote imaging system.

Chapter 3

An Anti-Vibration TDI CIS with Dynamic Signal Transfer

3.1 Introduction

Aiming at the vibration-induced blur, in this chapter, a TDI CMOS image sensor with dynamic pipeline signal transfer is proposed for remote image sensing system. The TDI function is implemented by 8-stage adjacent pixel signal transfer architecture, where the photo signals are transferred by in-pixel unity-gain buffers in pipeline. To compensate for the vibration-induced blur, a dynamic charge transfer path similar to the electrical vibration compensation introduced in Section 2.4.4 is proposed. If vibration is detected, the stage shifter would control the photo signal transferred to its left or right neighbors in the next stage, so as to make the photo signals move with the image motion and further compensate for the image blur. Another feature is tunable well capacity achieved by pixel bypassing operation, which would be executed when the average ambient light brightness is detected as high.

In this chapter, the proposed TDI CMOS image sensor with dynamic pipeline signal transfer is introduced in detail with the rest of the chapter is set out as follows. Section 3.2 illustrates the image sensor design as well as the operations; Section 3.3 presents the noise analysis for the signal path; Section 3.4 details the image sensor implementation and Section 3.5 draws some conclusions.

3.2 Image Sensor Design

3.2.1 Sensor Architecture

The architecture diagram of the proposed TDI image sensor is shown in Fig. 3.1. The sensor consists of four parts: a two-dimensional pixel array of 1536 × 8 pixels, a stage shifter, a column scanner and a set of global output buffer. Among them, for the pixel array, the 1536 columns define the spatial resolution of the image and all the pixels in each

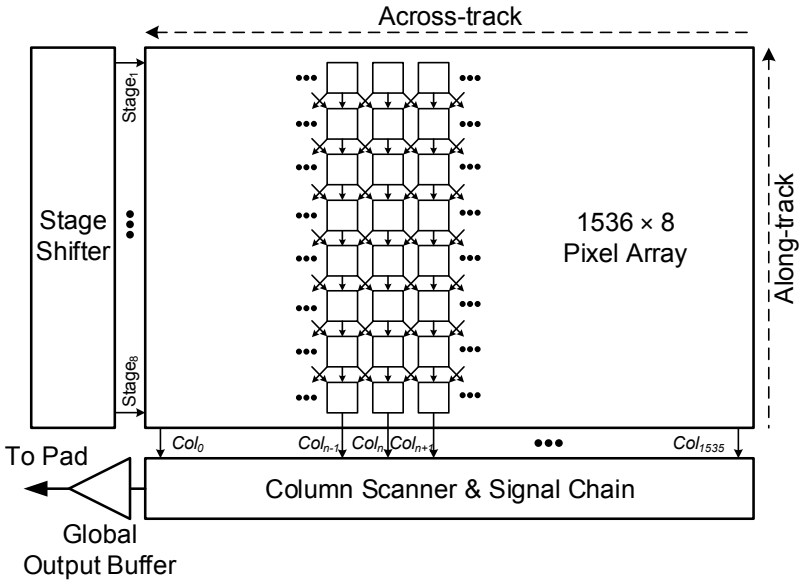

Figure 3.1: Architecture diagram of the proposed anti-vibration TDI image sensor with dynamic pipeline signal transfer.

column comprise a chain of 8 TDI transfer stages, $Stage_1 \sim Stage_8$. The stage shifter provides control signals to transfer the intermediate integration signal to the next stage at a fixed time interval, i.e., the time for the satellite travailing one ground resolution pixel, herein it is named as line period or line time. There is a switch network between TDI stages, enabling various transfer paths. The final integration results presented at the end of the integration chain are sequentially accessed by the column scanner. The selected column is then read out by a gain amplifier for signal amplification, and a global output buffer, which is constructed by a two-stage OP-AMP to drive the analog pad.

3.2.2 TDI Signal Path

The whole signal path from the pixel to the global output buffer is shown in Fig. 3.2. In the first stage ($Stage_1$), a pixel is comprised of a reset transistor (RST_1), a photodiode with configurable integration capacitors(C_{INT}), mode-selected switches (S_{A1}, S_{B1} and S_{C1}), a sample-hold capacitor (C_{SH1}) and a unity-gain buffer. PMOS transistor is applied to reset the photodiode voltage to VDD without the threshold voltage drop, so it can achieve higher photodiode voltage swing than NMOS reset transistor. The rest stages ($Stage_2 \sim Stage_8$) have a similar structure to the first one, but the PMOS reset transistor is changed into transmission gates to pass low voltage, and the integration capacitor is removed. Between stages, three direction-selected switches allow the pixel in Col_m ($m = 1,\ 2\ ...\ 1536$) to transfer the intermediate photo signal either to its direct next stage pixel in the same column via switch S_{Dn}, or its left neighbor Col_{m-1} via switch S_{Ln} ($n = 1,\ 2\ ...\ 8$), or the right one Col_{m+1} through switch S_{Rn}, respectively. Under the strong ambient illumination condition, there is no need to extend the integration time and hence the integration stages should be programmable. By-passing a stage can be implemented using mode-selected switches. If the light intensity is higher, the integration capacitor C_{int} will be enabled by switch S_{int}. In each stage, the unity-gain buffer only

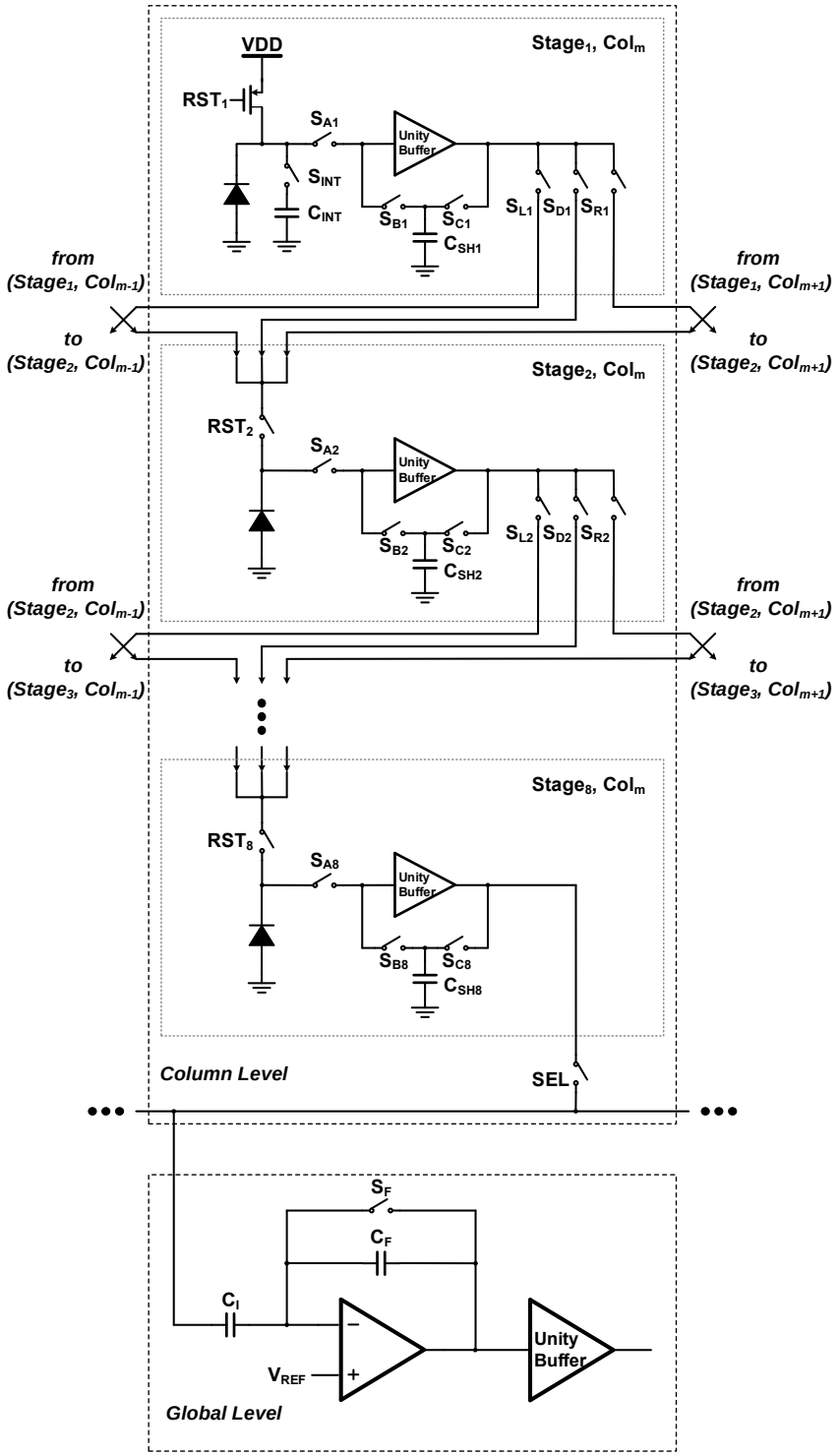

Figure 3.2: Signal path schematic of the proposed anti-vibration TDI image sensor with dynamic pipeline signal transfer.

works during the short period of charge transfer, and is turned off in the long integration time for power saving.

3.2.3 TDI Operation

The TDI function contains three basic operations: integration, sample-hold, and reset (for $Stage_1$) / signal transfer (for $Stage_2 \sim Stage_8$).

3.2.3.1 Integration

During the integration period, all the switches are turned off to isolate the photodiodes from the other in-pixel circuits, the pixel configuration is shown in Fig. 3.3(a). At the same time, all the in-pixel unity-gain buffers are turned off to reduce power consumption.

3.2.3.2 Sample-Hold

Till the end of each line period, the integration phase is finished. Then the pixels will carry out a sample-hold operation to store the photo signals. For each stage, the intermediate photo signal will be temporarily sampled and held by an analog memory C_{SHn} ($n = 1,\ 2\ ...\ 8$). The whole process is completed by turning on the mode-selected switches S_{An} and S_{Cn}, as shown in Fig. 3.3(b).

3.2.3.3 Reset/Transfer

After the sample-hold operation, switches S_{An} and S_{Cn} are turned off, on the contrary S_{Bn} is turned on, which will enable the photo signal transfer path from C_{SHn} to the next stage photodiode through the unity-gain buffer from the last stage to the first one, so the photodiode is reset as the voltage stored in the previous sample-hold capacitor $C_{SH(n-1)}$. Apparently, pixels in the first stage are reset by an initial VDD voltage. The corresponding circuit configuration is illustrated in Fig. 3.3(c).

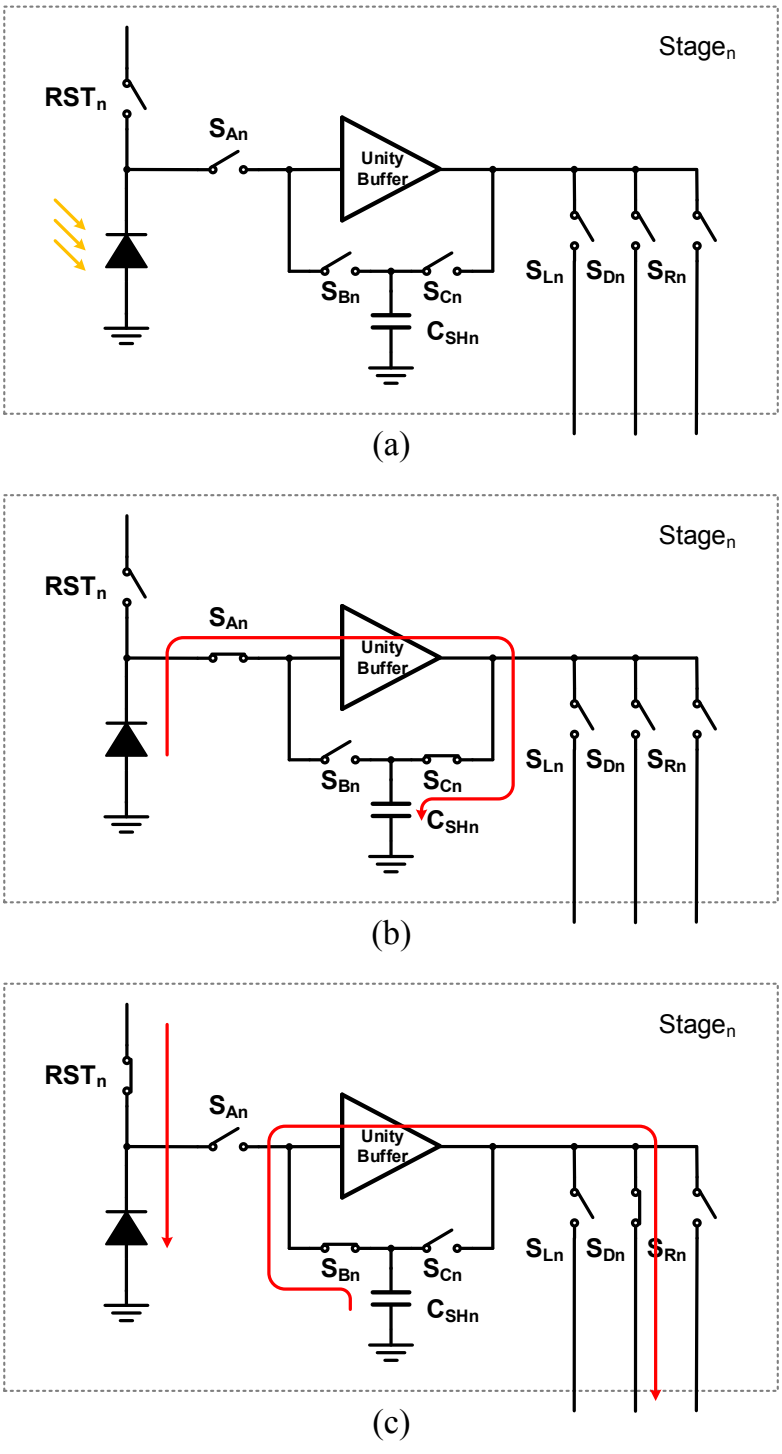

Figure 3.3: Pixel configurations for (a) Integration, (b) Sample-hold and (c) Reset/Transfer in the dynamic pipeline signal transfer scheme.

3.2.4 Dynamic Transfer Modes

In addition to the basic TDI operations, this design can also perform two additional modes: configurable integration stages and configurable signal transfer directions. An external system with a high speed camera and an on-board image processor similar to the one shown in Section 2.4.3 will sense the illumination level and the direction of the satellite motion in the whole imaging flow. Then the switches in the TDI stages can be controlled by the stage shifter to implement different signal transfer modes. Three scenarios are given in Fig. 3.4. The first example is the conventional TDI operation, in which all stages contribute to the integration time and the partial integration charges are summed stage by stage in the same column until it reaches last row.

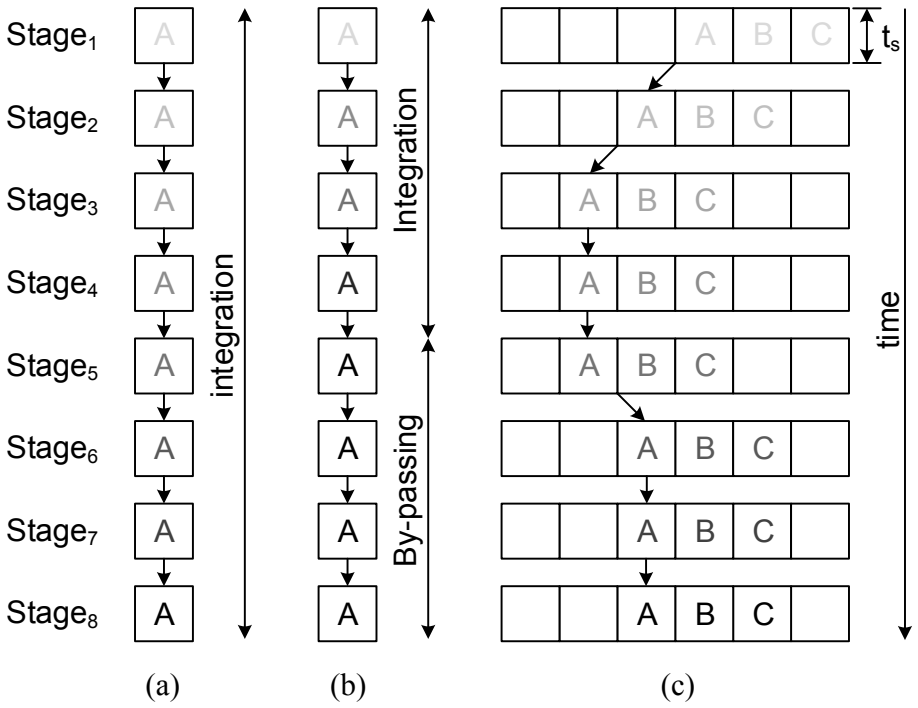

Figure 3.4: TDI operation scenarios in the dynamic pipeline signal transfer scheme: (a) Straight integration, (b) Integration and bypass stages, and (c) Integration with direction control.

3.2.4.1 Configurable Integration Stages

In Fig. 3.4 (b), the last four stages are bypassed to adapt the sensor under strong ambient illumination condition to avoid photo signal saturation. The configuration is shown in Fig. 3.5, a signal path is enabled to make the input signal directly transferred to the output through in-pixel unity-gain buffer, so the stage is bypassed. Under extreme bright condition, only the first stage takes the integration with additional integration capacitor C_{INT} and all the other stages are by-passed.

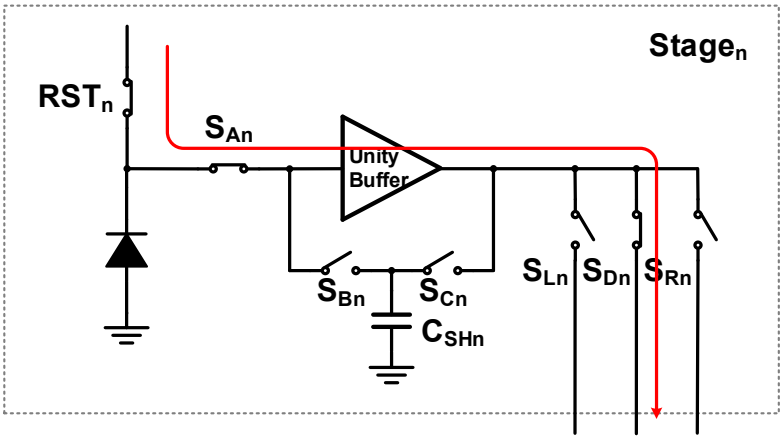

Figure 3.5: Pixel configuration for bypass in the dynamic pipeline signal transfer scheme.

3.2.4.2 Configurable Signal Transfer Directions

If the satellite suffers from vibrations in the across-track direction, direction-selected switches (S_{Ln} and S_{Rn}, $n = 1,\ 2\ ...\ 8$) will activate the dynamic signal transfer paths, as shown in Fig. 3.4 (c). Since the satellite motion is monitoring by a high speed camera and an on-board image processor, the path can be updated in real time during the integration. This will effectively address the image smear caused by flight fluctuations, and the real time operation does not require extra image post processing.

3.3 Noise Analysis

In this section, two important figures for integration mode images sensor, dynamic range and signal-to-noise ratio, are investigated. A sensor model in [2] is extended to suit the proposed TDI architecture, intending to analytically relate the sensor response with the photo current signal, dark current signal, and the noise for sensor output in the integration mode as well as integration stages. The sensor model of the proposed TDI image sensor is illustrated in Fig. 3.6. There are n pixel stages in the model, and the integration time in each stage is t_s so the total integration time is $(n \cdot t_s)$. Assuming the integration does not saturate throughout all the n-stage TDI operation, the partial accumulated charge Q_n in stage n are added together to form the final output charge Q_o. The photocurrent and the dark current in stage n are i_{ph} and $i_{dc,n}$, respectively, with the assumption that the photo current is constant for all the TDI integration stages. $N_{i,n}$ denotes the equivalent zero-mean input referred noise introduced in each stage and the average power of which is given by

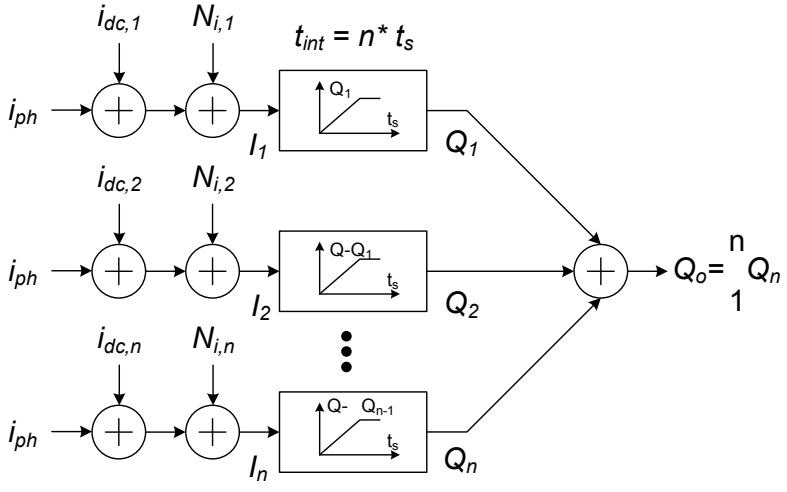

Figure 3.6: Sensor model of the proposed anti-vibration TDI image sensor with dynamic pipeline signal transfer.

$$\sigma_{N_{i,n}}{}^2 = \frac{q\left(i_{ph} + i_{dc,n}\right) t_s + \sigma_{r,n}{}^2}{t_s{}^2} \qquad \text{(Eq. 3.1)}$$

where $q = 1.6 \times 10^{-19}$ C, and $q(i_{ph} + i_{dc,n})t_s$ is the output referred noise due to the shot noise caused by photo and dark currents and $\sigma_{r,n}{}^2$ is the variance of the noise charge caused by the readout circuit in the pixel, including reset noise of the photodiode, offset noise in the in-pixel amplifier as well as fixed pattern noise between stages.

Assume q_{max} is the full well capacity, so the corresponding DR and SNR in single stage n can be expressed as

$$DR_n = 20\log\left(\frac{q_{max} - i_{dc,n}t_s}{\sqrt{qi_{dc,n}t_s + \sigma_{r,n}{}^2}}\right) \qquad \text{(Eq. 3.2)}$$

$$SNR_n = 20\log\left(\frac{i_{ph}t_s}{\sqrt{q\left(i_{ph} + i_{dc,n}\right)t_s + \sigma_{r,n}{}^2}}\right) \qquad \text{(Eq. 3.3)}$$

To find out the relation of both DR and SNR regarding to the number of TDI stages, with the assumption that the dark current $i_{dc,n}$ is constant for all the TDI stages, similar to i_{dc}, the corresponding DR and SNR as functions of number of TDI stages are given by

$$DR(n) = 20\log\left(\frac{q_{max} - i_{dc}nt_s}{\sqrt{qi_{dc}nt_s + \sum_1^n \sigma_{r,n}{}^2}}\right) \qquad \text{(Eq. 3.4)}$$

$$SNR(n) = 20\log\left(\frac{i_{ph}nt_s}{\sqrt{q\left(i_{ph} + i_{dc}\right)nt_s + \sum_1^n \sigma_{r,n}{}^2}}\right) \qquad \text{(Eq. 3.5)}$$

The noises due to readout circuits, $\sigma_{r,n}{}^2$, introduced in all stages are uncorrelated and are assumed to have the same variance, $\sigma_{r,}{}^2$. Then the above equations can be simplified as

$$DR(n) = 20\log\left(\frac{q_{max} - n \cdot i_{dc}t_s}{\sqrt{n} \cdot \sqrt{qi_{dc}t_s + {\sigma_r}^2}}\right) \quad \text{(Eq. 3.6)}$$

$$SNR(n) = 20\log\left(\frac{\sqrt{n} \cdot (i_{ph}t_s)}{\sqrt{q\,(i_{ph} + i_{dc})\,t_s + {\sigma_r}^2}}\right) \quad \text{(Eq. 3.7)}$$

A sensor example is applied to evaluate the senor model and the two performance figures. The relevant sensor parameters are chosen as $q_{max} = 125000$ e$^-$, $Nr = 20$ e$^-$, $i_{ph} = 1$ pA, $i_{dc} = 1$ fA and $t_{int} = 1$ ms [2]. The simulation results are shown in Fig. 3.7. On one hand, DR drops with the number of stages, which introduce more input referred noises and dark current, adding to noise floor and thus the minimum detectable photo current. On the other hand, SNR increases with the square root of the number of stages, thanks to the fact that signal increases more quickly (linearly) than the input referred noises with integration time.

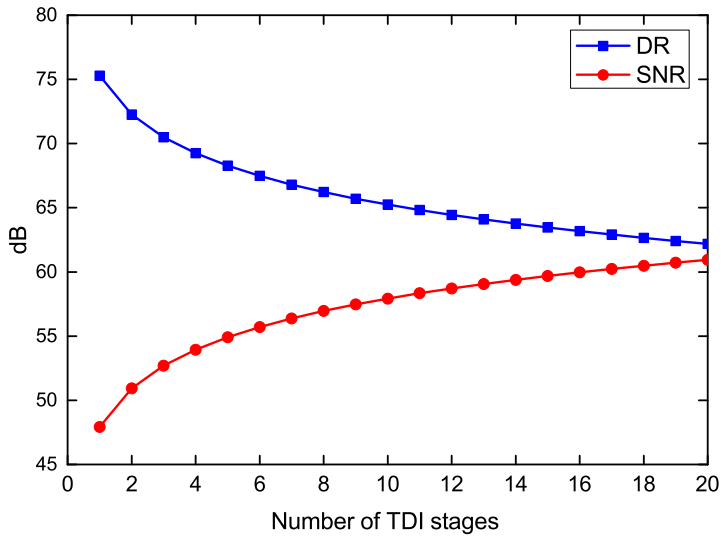

Figure 3.7: Simulated DR and SNR with regard to stage number based on the proposed TDI sensor model.

3.4 Sensor Implementation

A prototype chip of 1536 × 8 pixels was designed using TSMC 0.18 μm CIS technology (1P6M). In order to achieve higher ground resolution, efforts were made to optimize the layout of the chip as shown in Fig. 3.8 (a), and a portion of the pixel array is highlighted in Fig. 3.8 (b). Photodiode and other in-pixel circuits are floor-planned in different arrays to achieve a high resolution. The top off-array pixel circuits are dedicated to the first four stages and the bottom for the last four, the second metal layer to the fifth metal layer are used for the top four stages and bottom four stages separately, the sixth metal layer are used to connect the fourth and the fifth stages. Fig. 3.8 (c) gives a single column of the photodiodes, with each occupying 3.25 × 3.25 μm^2. This physical

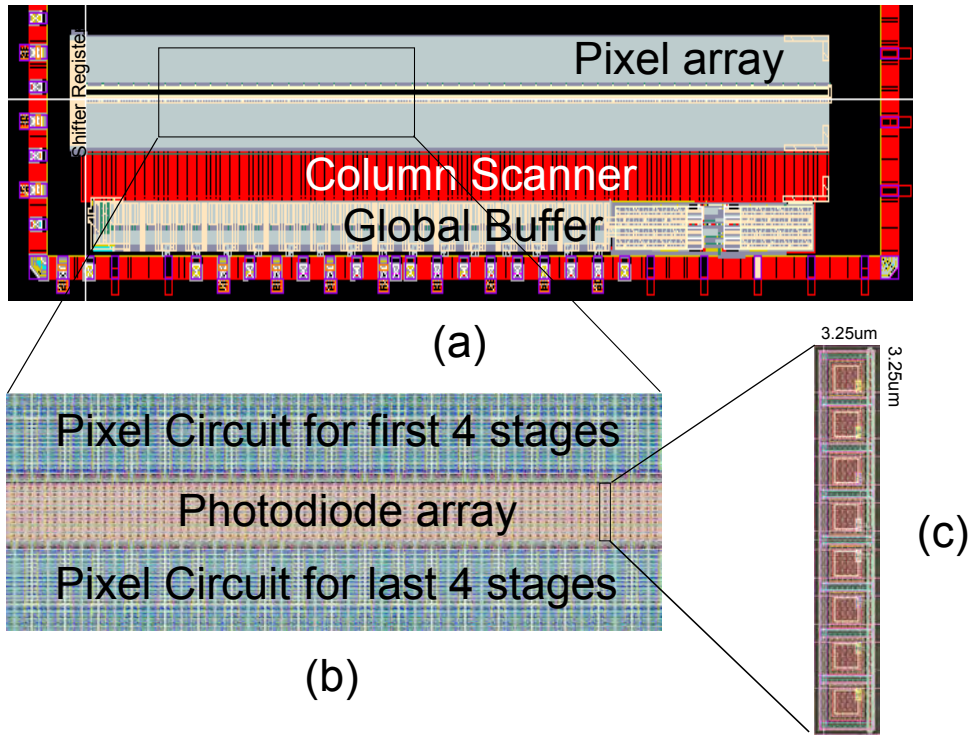

Figure 3.8: Layout of the proposed anti-vibration TDI image sensor with dynamic pipeline signal transfer.

implementation strategy allows to minimize the pixel pitch (3.25 μm) and maximize the fill factor (57 %).

3.5 Design Summary

In this design, a TDI CMOS image sensor is proposed as such, equipped with a highly programmable pipeline adjacent pixel signal transfer architecture. The main benefits are listed as below.

(1) The configurable signal transfer directions can compensate for the image motion caused by the satellite vibrations to raise the image quality.

(2) The configurable integration stages can avoid the integration saturation, so as to increase the DR.

(3) The separate photodiode array placement can achieve a high resolution.

(4) The pipeline signal transfer path can increase the ratio of integration time to line period, so as to prolong the effective integration time.

While, it also suffers from shortcomings as follows.

(1) The configurable signal transfer directions can only make the signal go in 45° or 90° angles, which constrains the compensation accuracy.

(2) Due to the narrow column pitch limitation imposed on the routing resource, an individual unity-gain buffer per stage, which consumes more area, is necessary to implement and distribute the complicated switch network.

(3) The separate photodiode array leads to the complexity of routing, and it is restricted by the number of metal layers provided by the CMOS fabrication process.

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Chapter 4

A TDI CIS with Column-Parallel Single-Ended Accumulators

4.1 Introduction

Because the achievable stage number of the adjacent pixel transfer method is seriously restricted by the routing resource, i.e. the total metal layers, provided by the CMOS fabrication technologies. In this chapter, a new TDI CMOS image sensor equipped with column-parallel single-ended signal accumulators is proposed. The united single-ended accumulators, which operates the TDI functions, can achieve a smaller column pitch than the full differential structures, as well as a shorter column stripe than the sperate TDI accumulators. Since the TDI operation is carried out off pixel array, the standard 4T-APS structure is applied. The rest of the chapter is laid out as follows. Section 4.2 describes the image sensor design; Section 4.3 discusses the noise created along with the TDI signal path; Section 4.4 introduces the chip implementation; Section 4.5 elaborates on the measurement result and Section 4.6 summarizes this chapter.

4.2 Image Sensor Design

4.2.1 Sensor Architecture

A TDI CMOS image sensor with column-parallel single-ended signal accumulators is proposed. Fig. 4.1 describes the system architecture. The main functional blocks consist of a standard 4T-APS pixel array, 256 column-parallel single-ended signal accumulators, a stage shifter, a set of two-stage global pipeline output buffer, a timing controller and an analog reference generator. The pixel array is controlled by the stage shifter for standard operation, and the photo signals are transferred to the column-parallel single-ended signal accumulators for TDI processing. Due to the silicon budget, a two-stage global pipeline output buffer is utilized instead of column-parallel ADCs. The timing controller generates all the control signals from the external reset, clock and exposure setting signals. An the analog reference generator including a bandgap is applied here to provide on-chip biasing and reference voltages for low noise purpose.

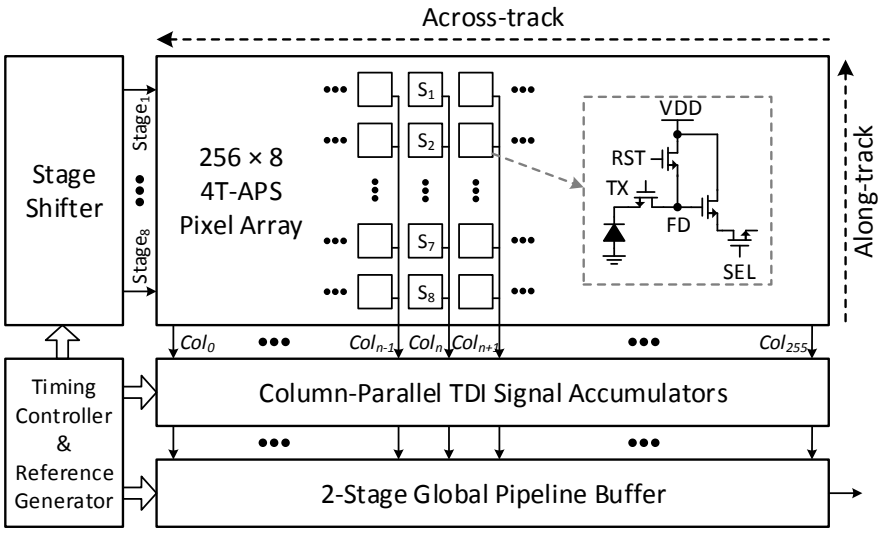

Figure 4.1: Architecture diagram of the proposed TDI CIS with column-parallel single-ended signal accumulators.

4.2.2 TDI Signal Path

Fig. 4.2 depicts the signal path schematic from the pixel array to the column-parallel TDI signal accumulator, which is founded on a single-end gain amplifier. The TDI accumulation signals generated by the 8 TDI stages will be stored in the 8 TDI accumulation capacitors, $C_{A1} \sim C_{A8}$, following the principle that the signals from the same object are stored in the same capacitor. This benefits of this structure are summarize as follows:

(1) the signal accumulator can add the photo signals to the feedback capacitors to perform the TDI function;

(2) the reset noise and the noise caused by charge injection and clock feed-through during tuning off the *RST* transistor of 4T-APS can be eliminate by the CDS operation together with the TDI operation;

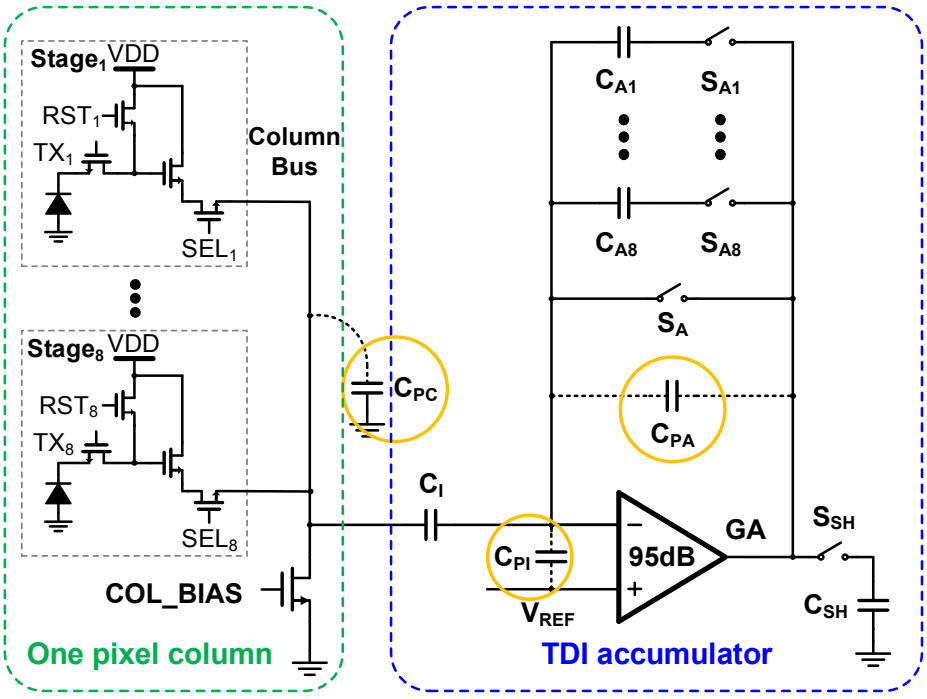

Figure 4.2: Signal path schematic of the proposed TDI CIS with column-parallel single-ended signal accumulators.

(3) the signal accumulator can amplify the effective photo signal by a factor as $\sqrt{C_I/C_{Ai}}$ ($i = 1,\ 2\ ...\ 8$) to further increase the SNR and DR;

(4) the united accumulator structure can save area of the column slices and reduce the corresponding power consumption and mismatch.

The circled capacitor C_{PC} is the parasitic capacitance between column bus and ground, C_{PI} is the parasitic capacitance between the two input terminals of the OP-AMP, and C_{PA} is the feedback parasitic capacitance between the negative input terminal and output terminal of the OP-AMP. These parasitic factors would introduce amplification error and increase the noise, so the open loop gain of the OP-AMP is designed to be as high as 95 dB to eliminate the negative effects.

4.2.3 TDI Operation

As shown in Fig. 4.2, all the pixels share the same column bus and the united TDI signal accumulator, thus after integration, the pixels in the same column would be read out one by one, similar to the roller shouter operation in conventional CMOS image sensor. Fig. 4.3 shows a simplified timing diagram of the 8-stage TDI operation. After integration, the stage shifter starts rolling from $Stage_8$ until $Stage_1$, enabling read-out of photo signals. For $Stage_1$, which is exposed to a new object, prior to readout, the correlated accumulation capacitors C_{Ai} ($i = 1,\ 2\ ...\ 8$) are reset by turning on S_A and a correlated switch S_{Ai}. Meanwhile, the pixel reset signal is sampled on C_I. After a two cycle delay from turning off S_A, CDS and TDI operations are performed by turning on TX_1. The delay is to avoid simultaneous capacitor reset and photo signal readout, which gives rise to noise and signal loss. The first stage TDI operation is completed by turning off S_{Ai} followed by TX_1. Then the stage shifter switches to $Stage_2$, of which the correlated capacitor C_{Aj} ($j = 1,\ 2\ ...\ 8$) already stored the photo signal from $Stage_1$ during last time integration. Therefore, C_{Aj} does not need to be reset, and S_{Aj} is turned

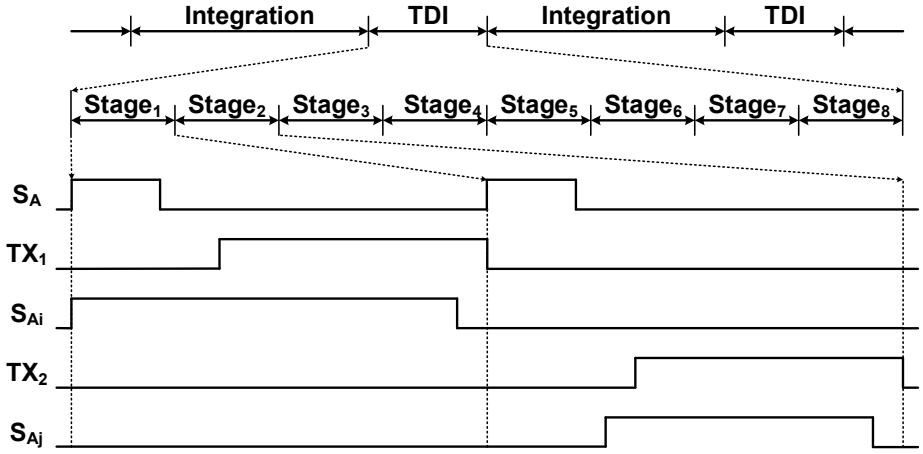

Figure 4.3: Simplified timing diagram of the proposed TDI CIS with column-parallel single-ended signal accumulators.

on after turning off S_A and before turning on TX_2 to avoid noise and signal loss. The second stage operation is completed by turning off S_{Aj} followed by TX_2. In line with the sequential order, the same operation is is repeated till all the 8 stages are completed.

In the TDI signal accumulator, the accumulation capacitors ($C_{A1} \sim C_{A8}$) are controlled by a TDI shifter, following the principle of adding photo signals generated from the same scene into the same capacitor. Fig. 4.4 shows the principle of 8-stage TDI operation and the correlated pixel-to-capacitor arrangement rule. $G_1 \sim GP_{10}$ are the ground scenes to be imaged (on a single line along with the camera movement direction), $P_1 \sim P_8$ are the 8 TDI stages (pixels) in one column, $C_{A1} \sim C_{A8}$ are the accumulation capacitors to store the TDI signals, and $T_1 \sim T_{10}$ are the time instances when the pixel is performing integration. At time T_1, only P_1 is exposed to G_1. After integration, the photo signal is read to C_{A1}, then at T_2, after the sensor has advanced by a pixel, P_1 finishes imaging G_2 and P_2 finishes imaging G_1, and the signals are transferred into C_{A2} and C_{A1}, respectively. The same process then repeats till a given ground scene (G_1) has been exposed to all the TDI stages, in this case which happens at T_8. C_{A1} now holds the complete photo signal corresponding to the integration of G_1 by all the TDI stages.

This signal is read out and C_{A1} is reset, allowing the integration signal produced from a new ground scene to be stored in it (at T_9). This process continues till the desired scene is imaged.

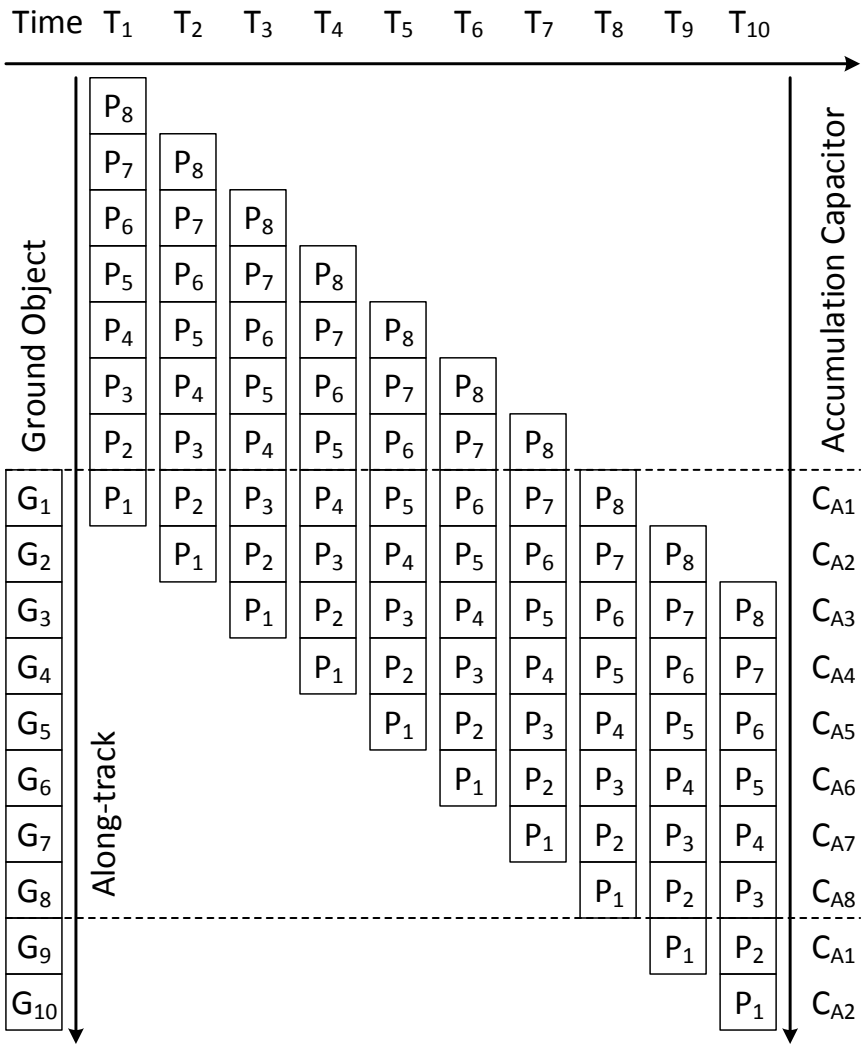

Figure 4.4: Principle of 8-stage TDI operation and the correlated pixel-to-capacitor arrangement rule.

4.3 Noise Analysis

TDI operation in CCDs can be treated as noise free, unlike CMOS, in which noise is a major challenge. The time invariant noise, known as the FPN, can be easily cancelled post image processing; the reset noise, frequency-related noise and noise due to charge injection and clock feed-through during switching off the *RST* transistor can also be eliminated by CDS operation. On the other hand, thermal noise, a predominant temporal noise which varies with the signal level and temperature is a limiting factor in CMOS TDI image sensors and will be discussed in detail in this section [36]. Thermal noise increases with the number of TDI stages and is a major factor that limits the design of TDI sensors with sizeable number of stages. In this design there are two major thermal noise sources: in-pixel source follower and OP-AMP in the TDI accumulator.

4.3.1 Source Follower

During TDI operation, thermal noise of the source follower will be sampled into the feedback capacitors of the TDI accumulator. Assuming the gain of the source follower is G_{SF}, the mean square noise voltage at the output node of the source follower can be written as [52]

$$\overline{v_{SF}{}^2} \cong {G_{SF}}^2 \xi_{SF} \frac{k_B T}{g_{m,SF}} \omega \qquad \text{(Eq. 4.1)}$$

where k_B is the Boltzmann constant, T is the absolute temperature, ξ_{SF} is the excess noise factor of the source follower, and $g_{m,SF}$ is the transconductance of source follower. ω is the cut-off angular frequency, depending on the circuit configuration.

4.3.2 TDI Accumulator

In the physical layout of the column-parallel TDI accumulator, all the circuits are placed within a narrow region, which lead to large routing parasitism that cannot be ignored. As highlighted in Fig.4.2, three parasitic capacitances should be taken into account: column bus parasitic capacitance C_{PC}, operational amplifier input parasitic capacitance C_{PI} and TDI accumulator feedback parasitic capacitance C_{PA}.

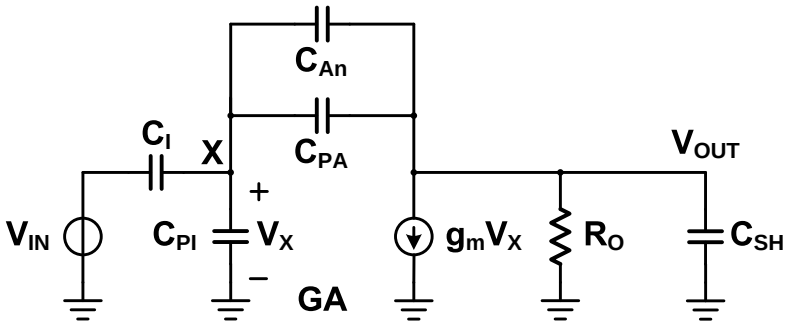

Figure 4.5: Equivalent schematic for TDI accumulator in the amplification phase.

Fig.4.5 shows the equivalent schematic diagram for TDI accumulator in the amplification phase, where C_{An} is one of the accumulation capacitors ($n = 1,\ 2\ ...\ 8$). The gain of the TDI accumulator can be given by

$$G_T \cong \frac{C_I}{C_{An} + C_{PA}} \qquad \text{(Eq. 4.2)}$$

During the TDI operation, each accumulation capacitor will sample the thermal noise of the source follower n times when reading out the pixel reset signal and n times when reading out the pixel photo signal.

For each stage, when reading out the pixel reset signal, the thermal noise is sampled into the column bus parasitic capacitor C_{PC} and the input capacitor C_I, therefore the cut-off angular frequency can be expressed as

$$\omega_{AR} \cong \frac{g_{m,SF}}{G_{SF}} \frac{1}{C_I + C_{PC}} \quad \text{(Eq. 4.3)}$$

Thereafter the noise will be transferred and sampled to the accumulation capacitor, and the mean square noise voltage can be given by [36]

$$\overline{v_{SF,AR}{}^2} \cong {G_T}^2 G_{SF} \xi_{SF} \frac{k_B T}{C_I + C_{PC}} \quad \text{(Eq. 4.4)}$$

While in the photo signal read out phase, the thermal noise will be directly sampled into one of the accumulation capacitors after being amplified by the gain amplifier. Under such circumstances, the cut-off angular frequency can be given as

$$\omega_{AO} \cong \frac{g_{mT} {C_{An}}'}{C_{SH} {C_I}' + C_{SH} {C_{An}}' + {C_I}' {C_{An}}'} \quad \text{(Eq. 4.5)}$$

where ${C_I}' = C_I + C_{PI}$, ${C_{An}}' = C_{An} + C_{PA}$, and g_{mT} is the transconductance of the OP-AMP in the gain amplifier. So the mean square noise voltage can be given by

$$\overline{v_{SF,AOn}{}^2} \cong {G_T}^2 {G_{SF}}^2 \xi_{SF} \frac{k_B T}{g_{m,SF}} \omega_{AO} \quad \text{(Eq. 4.6)}$$

During the amplification, the OP-AMP also contributes to thermal noise, which will be also sampled into the accumulator capacitor, as given by

$$\overline{v_{OPA,An}{}^2} \cong \left(1 + \frac{{C_I}'}{{C_{An}}'}\right)^2 \xi_T \frac{k_B T}{g_{mT}} \omega_{AO} \quad \text{(Eq. 4.7)}$$

where ξ_T is the excess noise factor of the OP-AMP which includes the noise of all the internal transistors. Therefore, the input referred noise in the floating diffusion caused by the TDI accumulator can be expressed as

$$\overline{v_{A,total}{}^2} \cong \sum_1^n \frac{\overline{v_{SF,AR}{}^2} + \overline{v_{SF,AOn}{}^2} + \overline{v_{OPA,An}{}^2}}{{G_{SF}}^2 {G_T}^2} \quad \text{(Eq. 4.8)}$$

4.4 Sensor Implementation

A prototype chip of the proposed TDI CMOS image sensor with column-parallel single-ended signal accumulator was fabricated applying TSMC 0.18 μm CIS technology (1P6M). As shown in the microphotograph in Fig. 4.6, without pad ring, the functional blocks occupy a total area of 2230 × 1945 μm^2. The pixel array is placed on the top, followed by the column parallel TDI accumulators with the same pitch as 6.5 μm. The global pipeline buffer is placed at the bottom with the output terminal close to the bonding pad for impedance reduction. Besides, the stage shifter, timing controller and reference generator are arranged globally on the right side for signal broadcasting.

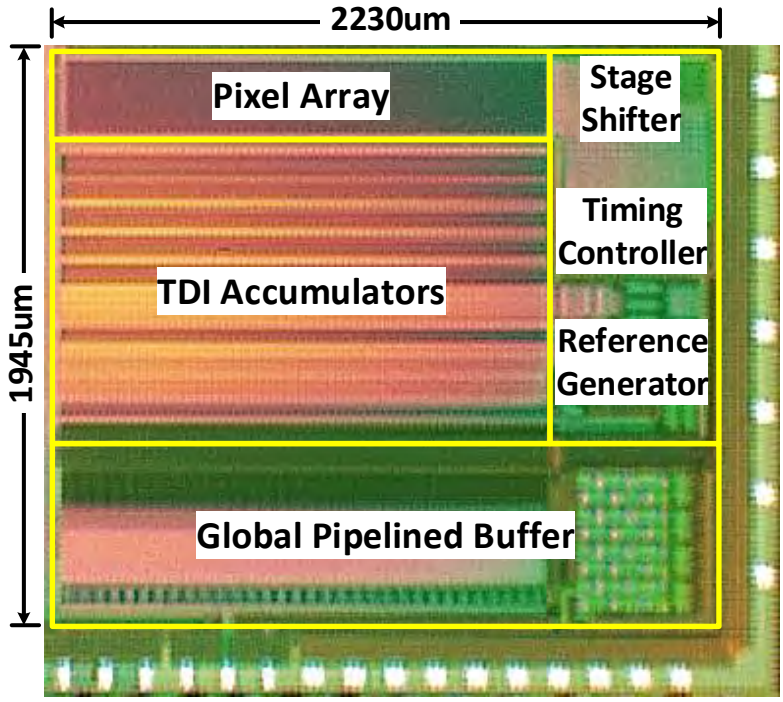

Figure 4.6: Microphotograph of the proposed TDI CIS with column-parallel single-ended signal accumulators.

4.5 Measurement Result

Fig. 4.7 shows the test platform used for carrying out the experiments. The TDI sensor board as well as the lens is mounted on top of a linear motor which provides necessary motion to mimic the satellite movement. The entire setup is based in a dark room and is on top of an optical table. The DC light source provides constant illumination for testing to avoid the difference caused by the alternating current (AC) ceiling light. The linear motor aids in the horizontal movement of the sensor, enabling the capture of a complete scene as shown in Fig. 4.8.

Fig. 4.8 shows the sample images photographed by the proposed TDI image sensor. All the images are captured under the same illumination condition, and with the same single-stage integration time. Captured from the same scene, (a) is taken by single-stage line scanning, while (b) is taken by 8-stage TDI. Similarly, (c) and (d) are taken by single-stage line scanning and 8-stage TDI, respectively, from the same scene. It can be

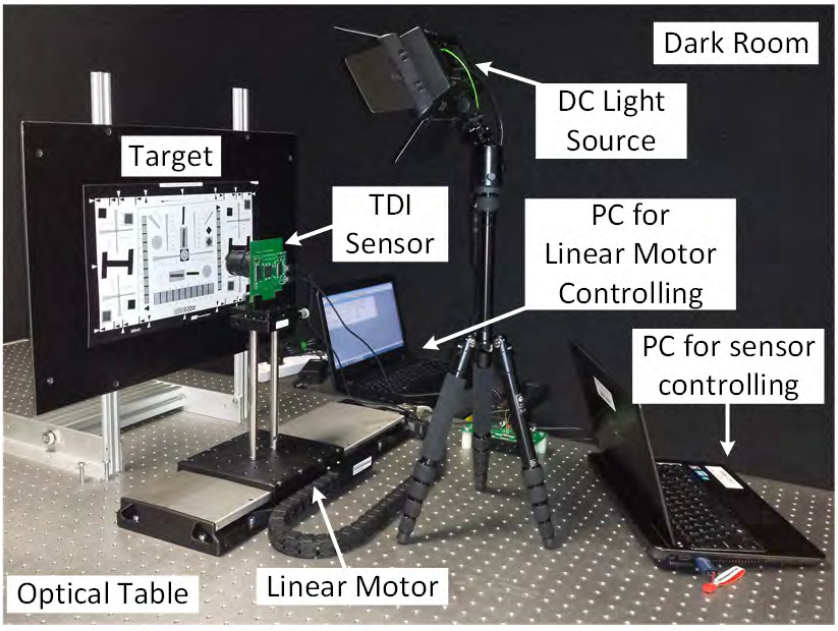

Figure 4.7: Test platform for the proposed TDI CIS with column-parallel single-ended signal accumulators.

seen that (b) and (d) are brighter than (a) and (c), that means the signal strengthes in (b) and (d) are higher than those in (a) and (c). In order to further characterize this feature, uniform light from a diffusing light sphere is utilized as the target. The results indicate that by applying the 8-stage TDI operation in this image sensor can achieve a DR of 52.3 dB and 8.8 dB SNR improvement comparing to single-stage line scanning.

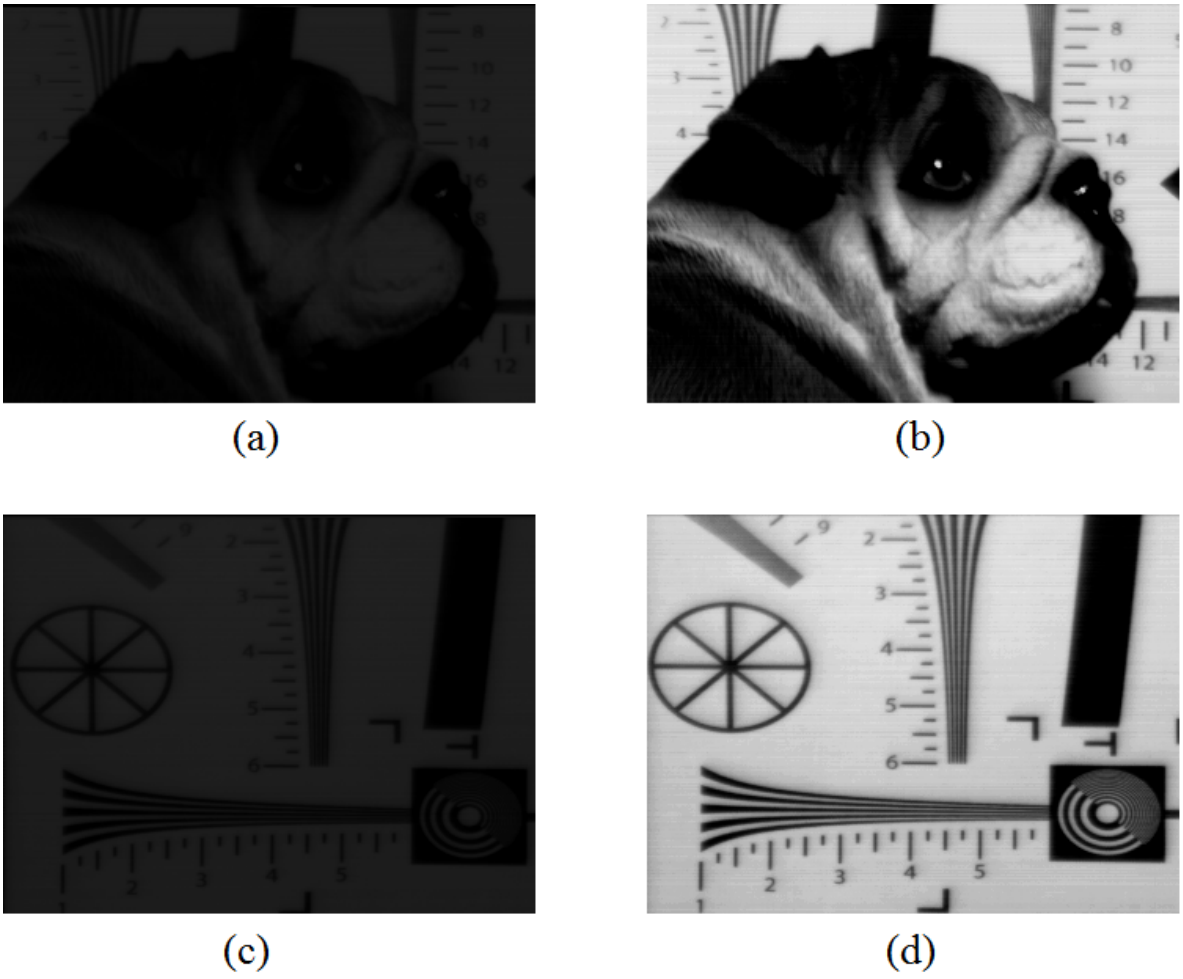

Figure 4.8: Sample TDI images taken by the proposed TDI CIS with column-parallel single-ended signal accumulators, (a) and (c) are taken by single-stage line scanning, (b) and (d) are taken by 8-stage TDI.

4.6 Design Summary

Throughout this chapter we have been proposing a TDI CMOS image sensor with column-parallel single-ended signal accumulators. Differing from the conventional TDI image sensor, it can

(1) achieve smaller pixel pitch and high resolution with the usage of standard 4T-APS pixel and column-parallel single-ended TDI signal accumulators;

(2) achieve a DR of 52.3 dB and 8.8 dB SNR improvement comparing with the single-stage line scanner with the high gain OP-AMP used in the accumulator.

Finally, the preliminary characterization results are summarized in Table 4.1.

Table 4.1: Performance summary of the proposed TDI CIS with column-parallel single-ended signal accumulators

Parameters	Performance
Technology	0.18 μm CIS (1P6M)
Resolution	256×8×5
Pixel Size	6.5×6.5 μm^2
Fill Factor	28 %
Max. Line Rate	1.74 kHz
Single-Stage Sensitivity	14769 e-/lux·s
Dark Current	55 e-/lux·s
FPN	0.39 %
FD-Referred Noise	40 e-
SNR Boost to Single Stage	8.8 dB
DR	52.3 dB
Power Consumption	119 μW/line

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Chapter 5

An Anti-Vibration TDI CIS with Online Deblurring Algorithm

5.1 Introduction

In this chapter, a second anti-vibration TDI image sensor is proposed with an online deblurring (ODB) algorithm that can compensate for the image shift on the focal plane. Unlike conventional TDI schemes, which shifts the photo signal from one pixel to its neighbor in next stage with the same column, and unconditionally accumulate their signals, the ODB algorithm can separate the photo signal portion belonging to "left" or "right" column and prevent them from mixing with the current signal. This method allows producing a sharp image even in scenarios involving complicated vibrations. The ODB algorithm can be fully integrated into the column-parallel TDI accumulators and operate the TDI function and image motion compensation without any other supporting circuits, payload or post image processing.

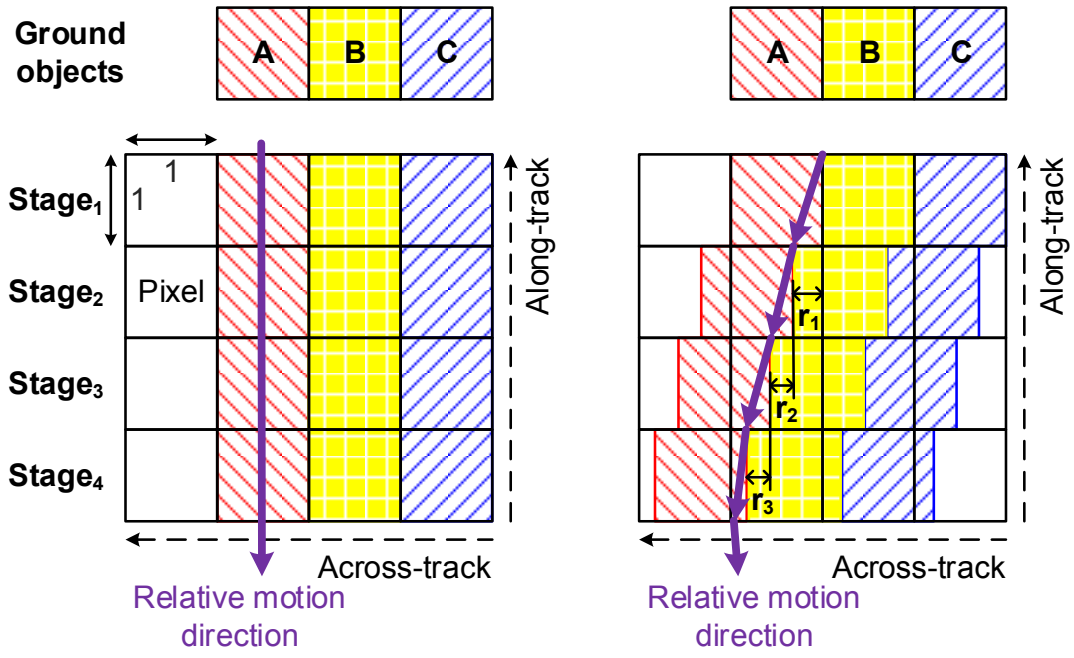
The rest of this chapter is fleshed out as follows. Section 5.2 introduces the principle of the ODB algorithm; Section 5.3 presents the TDI image sensor design with the signal

path design highlighted; Section 5.4 discusses the noise introduced by the TDI signal path; Section 5.5 elaborates on the chip implementation; Section 5.6 describes the measurement results, and Section 5.6 draws some conclusions.

5.2 Online Deblurring Algorithm

5.2.1 Algorithm Derivation

For the sake of clarity, a 4-stage TDI structure is used here to explain the algorithm. As can be seen in Fig. 5.1, A, B and C are three objects placed close to each other on the ground, and each one is projected onto one pixel on the sensor's focal plane. In fact, the three objects are identified by the first stage of pixels (after integration, whatever in



(a) Ideal TDI without vibration

(b) TDI with vibration

Figure 5.1: TDI images without (a) and with (b) vibration on the focal plane.

imaged in the first stage), and their brightness signals are treated as a reference in the following stages. In an ideal TDI, the subsequent stages should always image the same sets of objects and accumulate their photo signals. Fig. 5.1(a) shows this scenario.

Assuming the photo signal densities on the focal plane after optical system are evenly distributed, since the integration time in each TDI stage is split equally, the photo signal can be directly calculated by photo signal density and pixel area. For the second column, which is supposed to image object A, the photo signal captured by each TDI stages can be expressed as

$$Y_{A1} = Y_{A2} = Y_{A3} = Y_{A4} = a \tag{Eq. 5.1}$$

where a is the photo signal captured by the first stage. Under this condition, the final photo signal is listed as below,

$$Y_{A,ideal} = \sum_{i=1}^{4} Y_{Ai} = 4 \times a \tag{Eq. 5.2}$$

However, due to the aforementioned vibrations, the subsequent stages would have column-wise misalignment. Like what Fig. 5.1 (b) illustrates, one pixel could sense two objects together. In other words, photo signals of different objects are mixed. Assuming pixel size is one unit, the relative image shifts in the following TDI stages are r_1, r_2 and r_3, respectively. For the same column, the photo signals captured from each TDI stage can be expressed as:

$$Y_{A1} = a \tag{Eq. 5.3}$$

$$Y_{A2} = Y_{A1} + r_1(-a + b) \tag{Eq. 5.4}$$

$$Y_{A3} = Y_{A2} + r_2(-a + b) \tag{Eq. 5.5}$$

$$Y_{A4} = Y_{A3} + r_3(-a + b) \tag{Eq. 5.6}$$

where b stands for the signal strength of object B, which is captured by the pixel in the first stage, third column. Under such circumstances, if conventional TDI protocol is followed and all the photo signals are summed unconditionally, the final photo signal can be written as,

$$\begin{aligned} Y_{A,real} &= Y_{A1} + Y_{A2} + Y_{A3} + Y_{A4} \\ &= 4 \times a + (-a + b)\,(3r_1 + 2r_2 + r_3) \end{aligned} \tag{Eq. 5.7}$$

Apparently, the result is neither the pure signal from object A nor that from B, but rather a mixture of both, thus it would lead to a blurred image and cause serious damages to image quality.

The signal differences between each two neighboring stages can be calculated from Eq. 5.3 $\sim$ Eq. 5.6, and the total signal difference can be calculated as

$$\begin{aligned} \Delta Y &= 3 \times r_1(a - b) + 2 \times r_2(a - b) + 1 \times r_3(a - b) \\ &= 3(Y_{A1} - Y_{A2}) + 2(Y_{A2} - Y_{A3}) + (Y_{A3} - Y_{A4}) \\ &= \sum_{i=1}^{3} (4 - i)\big[Y_{Ai} - Y_{A(i+1)}\big] \end{aligned} \tag{Eq. 5.8}$$

One can note that ΔY is expressed as a weighted summation of the signal differences of each two neighboring stages, implying a compensation algorithm.

By accumulating the signal differences between each two neighboring stages in the same column and associating them with appropriate gains, the expected "clean" photo signal can then be derived by conventional TDI accumulation and an auxiliary stage-differential calculations. This method can be generalized to an n-stage TDI image sensor, the general expression of the "clean" signal being

$$Y = \sum_{i=1}^{n} Y_{Ai} + \sum_{i=1}^{n-1} (n - i)\big[Y_{Ai} - Y_{A(i+1)}\big] \tag{Eq. 5.9}$$

This expression clearly suggests that the algorithm can be implemented by two sets of gain amplifiers.

5.2.2 Algorithm Simulation Result

A model of a TDI image sensor was built with Matlab, and used to compare the performance of a conventional TDI scheme with that of the ODB algorithm. Fig. 5.2 shows the simulation results for a map of black-white line pairs (an 8-bit monochrome image) with

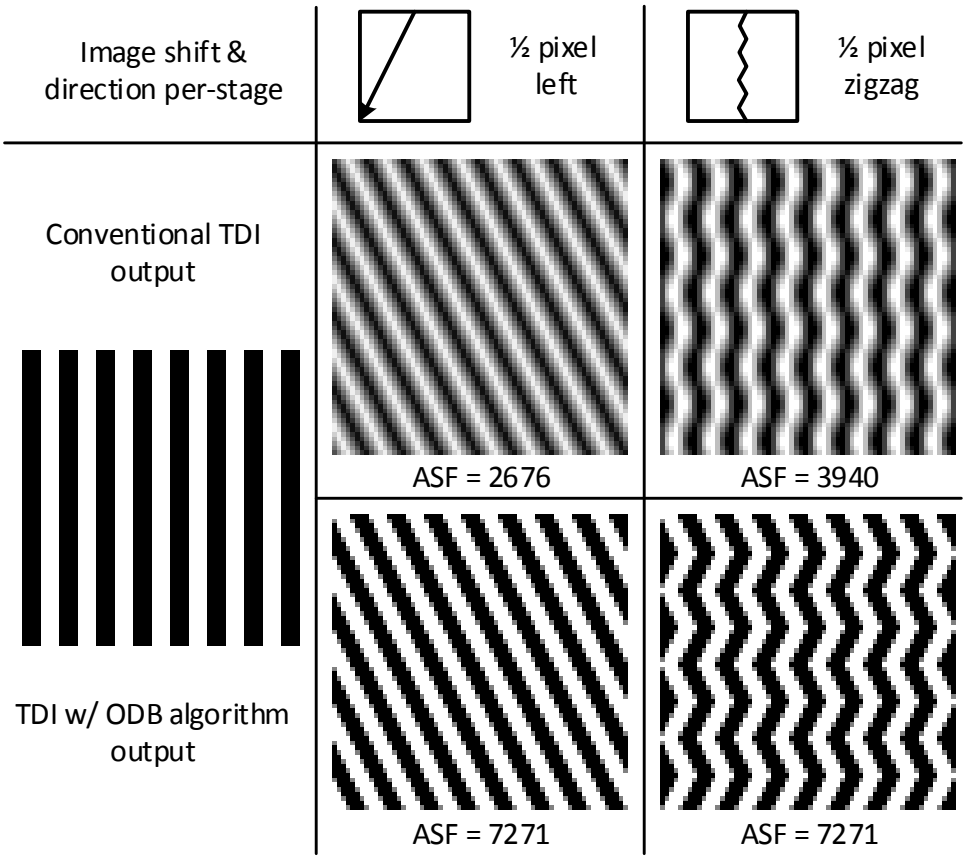


Figure 5.2: Simulation results for a map of black-white line pairs. Column 1 is the original image, Column 2 and 3 represent the output images under unidirectional and bidirectional vibration scenarios respectively. For each vibration mode, two sets of output images produced by both conventional TDI scheme and the ODB algorithm are obtained.

an 8-stage TDI model. The number of TDI stages selected was 8, taking into account the trade-off between SNR and DR [2]. The simulation followed the assumption that with the number of TDI stages, the output would be well integrated without being saturated. Since the same vibration amplitude could cause different image shifts on the focal plane with different optical systems, focal plane image shift was directly applied here as a metric of vibration level. For a given optical system, a higher vibration level leads to larger image shift. Unidirectional and bidirectional vibration scenarios were simulated, each with a half-pixel shift per stage. It was clearly shown that the ODB algorithm is capable of generating a sharp output image while the conventional TDI produces a blurred one. To further quantify the performance, we applied an average sharpness function (ASF) that is widely used in auto-focus algorithms as a figure of merit [140]. The ASF is defined as the average squared-gradient over the whole image, and can be expressed as

$$ASF = \left(\sum_{j=1}^{C} \sum_{i=1}^{R} |y(i+1,j) - y(i,j)|^2 \right) / CR \qquad \text{(Eq. 5.10)}$$

where, $y(i,j)$ denotes the luminance or grey level of an image of resolution $R \times C$.

To further evaluate the efficiency of the ODB algorithm, the algorithm performance with respect to variable image shifts per stage and different numbers of TDI stages is also simulated. Fig. 5.3 shows the simulation results with vibration level as a variable (while the number of TDI stages is fixed as 8). It is clear that the conventional TDI scheme is very sensitive to vibration. The sharpness of the output images decreases with more image shift, or equivalently higher level of vibrations. To the contrast, the ODB algorithm can retain the output images with high ASF values, even at very high level of vibration.

Fig. 5.4 shows the simulation results for the same input image with variable numbers of TDI stages. When the number of TDI stages is 1 (i.e., single-stage line scanner), the performances of the two solutions are the same, making the ASF values of the outputs

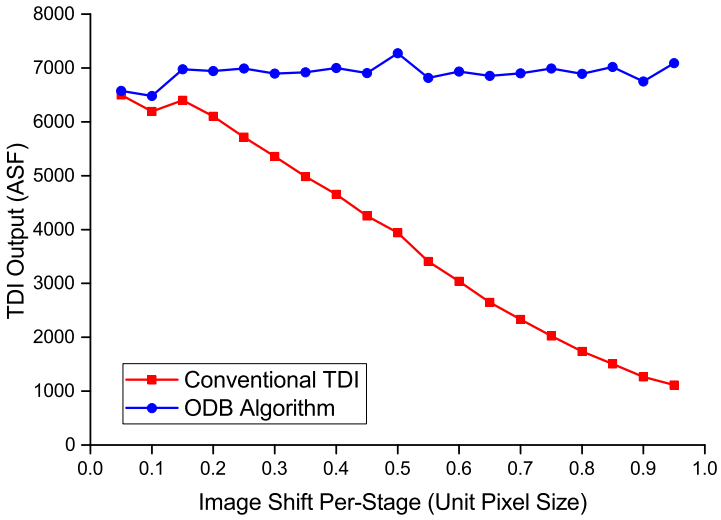


Figure 5.3: TDI output comparison between conventional TDI scheme and the ODB algorithm with variable image shifts (number of TDI stages = 8).

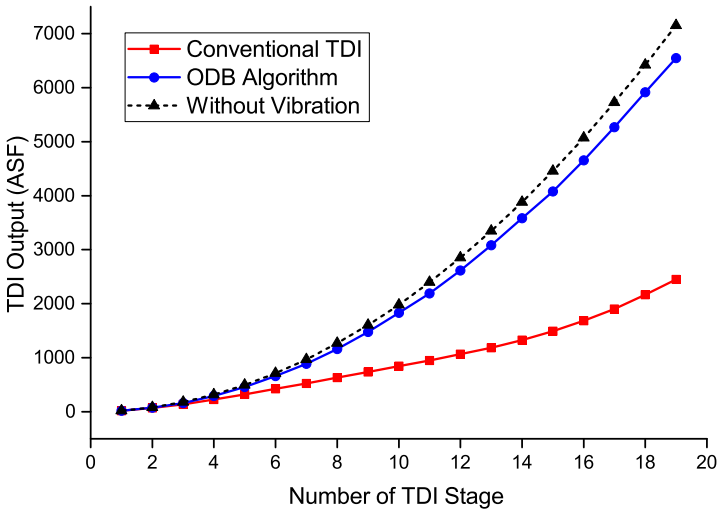


Figure 5.4: TDI output comparison between conventional TDI scheme and the ODB algorithm with variable numbers of TDI stages.

identical. As the number of TDI stages increases, the corresponding integration time also rises, as do the signal level of the outputs. Without vibration, the sharpness should increase in square with the number of TDI stages. The result clearly shows that the proposed ODB algorithm allows the sharpness grows much faster than the conventional

TDI scheme. Moreover, the ODB algorithm requires no prior knowledge of the variation, and is applicable to unidirectional left or right shifts, bidirectional motion, or even complicated zigzag variations, and suitable for any amount of image shifts (whether less or more than one pixel).

5.3 Image sensor Design

5.3.1 Sensor Architecture

The architecture diagram of the anti-vibration TDI CMOS image sensor is described in Fig. 5.5. The sensor mainly consists of seven principle modules. The first one is a 4T-APS pixel array with 256 × 8 resolution, in which the 256 columns define the spatial resolution of the image, and the 8 pixel rows facilitate the 8 TDI stages. The second part

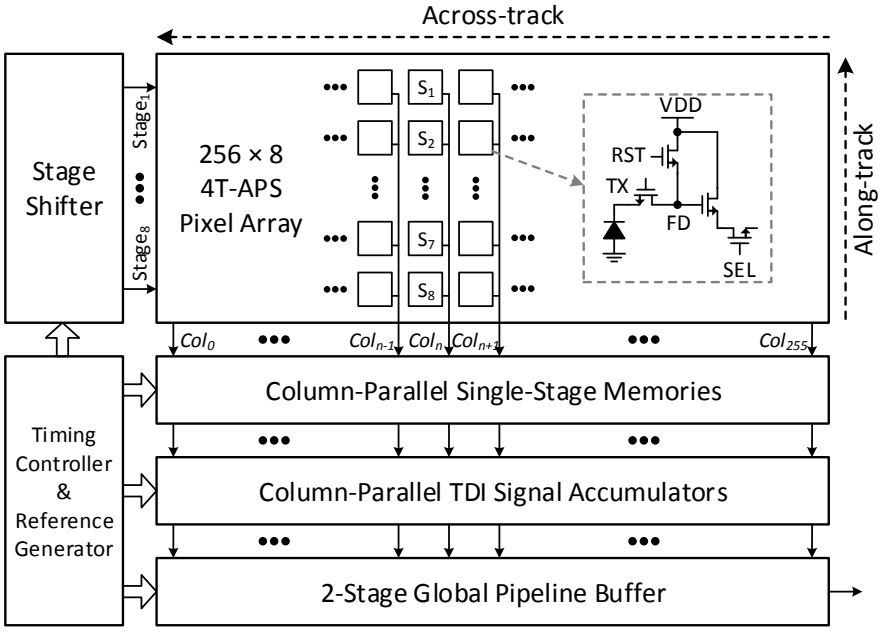


Figure 5.5: Architecture diagram of the proposed anti-vibration TDI image sensor with ODB algorithm.

is a column-parallel TDI accumulator array that execute the conventional TDI operation, and the third one is a 256 column-parallel single-stage memory array for ODB operation. The fourth component, the stage shifter, provides the pixel control signals; the fifth module, a 2-stage global pipeline output buffer, reads out the final photo signals after TDI operation; and the sixth and seventh parts are basic digital timing controller and analog reference generator, respectively. To minimize the noise and the mismatch, all the biasing voltages, analog reference currents and voltages are generated on chip.

5.3.2 TDI Signal Path

Fig 5.6 manifests the whole signal path from pixel to output buffer. The 8 pixels in a given column, marked in green, act as the 8 TDI stages. The column-parallel TDI circuits are integrated with two blocks: a TDI accumulator (marked in blue) and a single-stage memory (marked in red). The elements circled in orange are the critical parasitic capacitances, C_{PC} is the parasitic capacitance between column bus and ground, C_{PIN1} and C_{PIN2} are the parasitic capacitances between the two input terminals of the OP-AMPs, and C_{PA} and C_{PD} are the feedback parasitic capacitances between the negative input terminal and output terminal of the OP-AMPs. Since the standard 4T-APS is applied here, reset noise cannot be neglected and the gain amplifier is therefore chosen as the basic structure, which also allows CDS operations. The single-stage memory will read out the single-stage photo signal of each pixel with CDS operation, and the compensation capacitors ($C_{C1} \sim C_{C7}$), the different capacitance values of which implement the weight parameters (gain) in Eq. 5.9, will separately store the signals for subsequent neighboring stage signal difference calculation. The TDI accumulator is designed to operate both conventional TDI accumulation operation and neighboring stage difference accumulation. First, it reads out the single-stage photo signals with CDS and performs a conventional TDI accumulation with the C_{IA} as the input capacitor and one of the accumulation

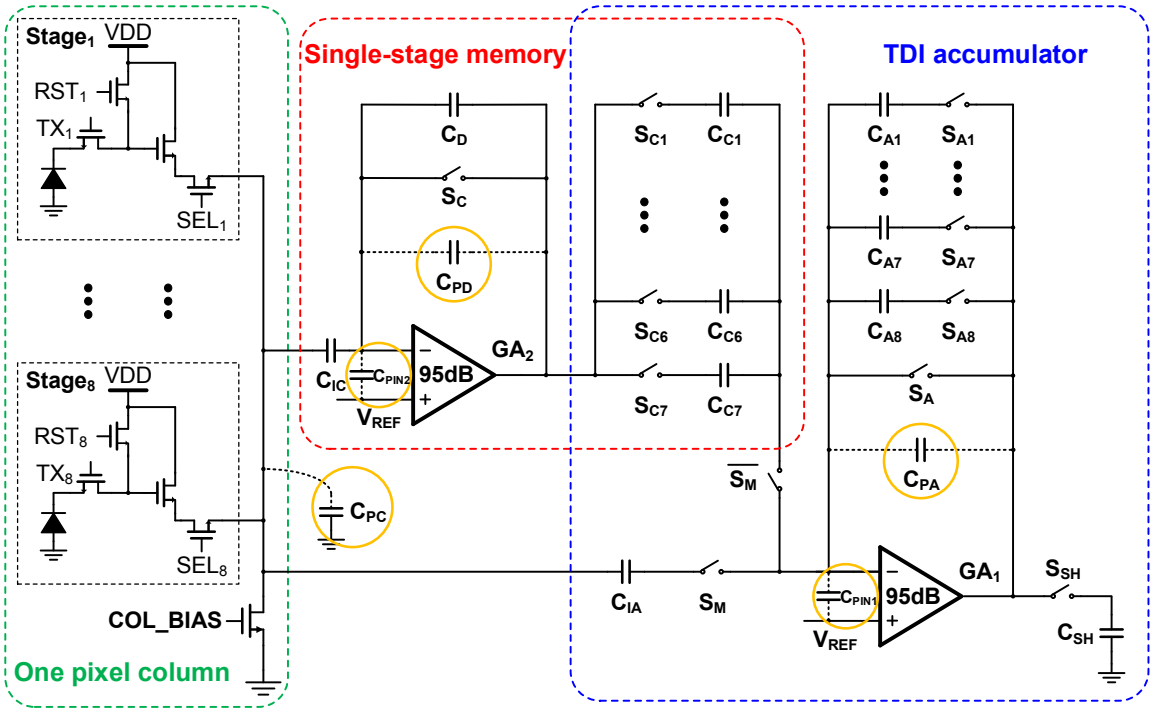


Figure 5.6: Signal path schematic of the proposed anti-vibration TDI image sensor with ODB algorithm.

capacitors ($C_{A1} \sim C_{A8}$) as the feedback capacitor (which also stores the TDI accumulation signal). The TDI accumulator then calculates the photo signal difference and adds it to the same accumulation capacitor, with one of the compensation capacitors as the input capacitor and the same accumulation capacitor as feedback.

5.3.3 TDI Operation

The proposed anti-vibration TDI image sensor has two operations, TDI accumulation and image motion compensation. To verify the algorithm, the image motion compensation is designed optional, with or without which the result images can be compared. The TDI accumulation and pixel-to-capacitor arrangement rule are the same as that introduced in Section 4.2.3.

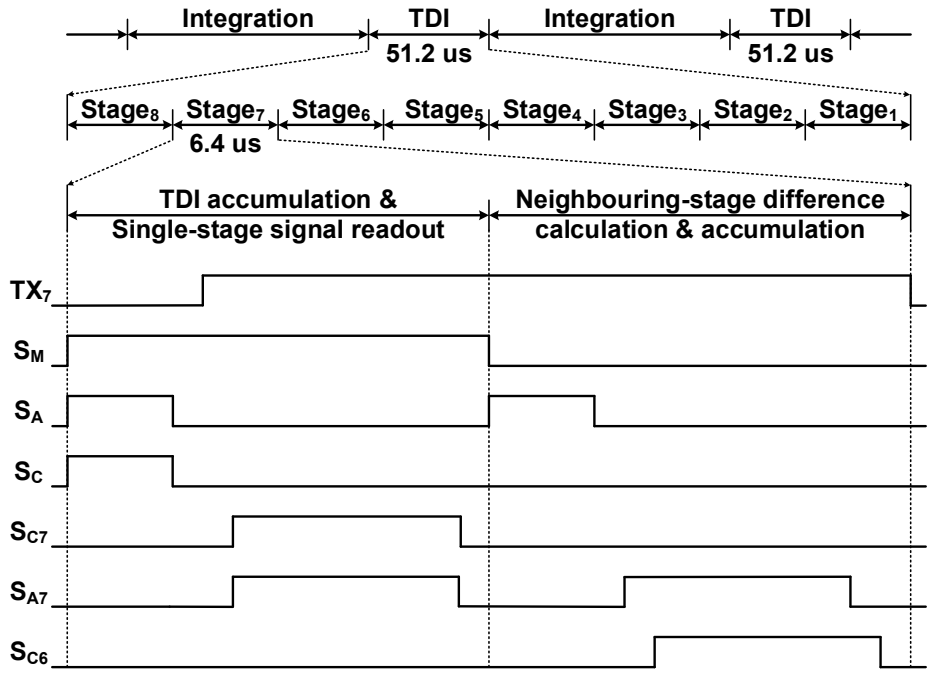


Figure 5.7: Simplified timing diagram of the proposed anti-vibration TDI image sensor with ODB algorithm.

Fig. 5.7 illustrates the simplified TDI timing diagram. After each integration, the stage shifter starts rolling in reverse order from $Stage_8$, which represents an object running out of the TDI stages. The TDI operation for each stage can be divided into two steps: the first step comprises conventional TDI accumulation and single-stage photo signal read out, and the second one comprises neighboring stage difference calculation and accumulation (available to $Stage_8 \sim Stage_2$). In the first step in $Stage_8$, the single-stage photo signal is added to the corresponding accumulation capacitor, and is also read out by the single-stage memory, but does not need to be stored because it is the last signal from a given object and there is no more subtraction. In the second step, the current signal is subtracted by the previous-time integration result stored in C_{C7}, and the difference is added to the same accumulation capacitor; it is then available to be read out to the output buffer. After $Stage_8$, the stage shifter then switches to $Stage_7$. In the first

step, the single-stage photo signal is added to another corresponding accumulation capacitor, and is also read out by the single-stage memory. Then a new difference between the photo signal of $Stage_7$ and that stored in C_{C6} is produced and added to the same corresponding accumulation capacitor in the second step. Since C_{C7} is now free, it can be used to store the current $Stage_7$ photo signal for the neighboring stage signal difference calculation after the next integration. Following this reverse order, the same operations are carried out from $Stage_6$ to $Stage_2$. In $Stage_1$, where the neighboring stage signal difference is not available, only the first step is carried out. After $Stage_1$'s operation, all the TDI accumulation and image motion compensation for current exposure is finished, and then a new integration would begin.

5.4 Noise Analysis

In this design, all the photo signals will be summed up, and both TDI accumulator and single-stage memory are implemented using gain amplifier, with many sampling operations involved. Therefore, the noise issue should be taken into consideration. Time invariant noise, commonly known as fixed pattern noise, can be easily cancelled by image processing. This section therefore focuses on temporal noise, such as shot noise, thermal noise, flicker noise and RTS noise, which may vary with the signal level and temperature [141–143]. Fig. 5.8 illustrates the temporal noise model for this anti-vibration TDI CMOS image sensor, from the photodiode to ADC. Because the delay between the two sampling of CDS is short, so the frequency-related noise, i.e., flicker noise and RTS noise, can be also removed. From Fig. 5.8, it can be seen that thermal noise is a predominant noise source during TDI operation, and increases the more TDI stages there are. Thermal noise is explained in detail in the next section.

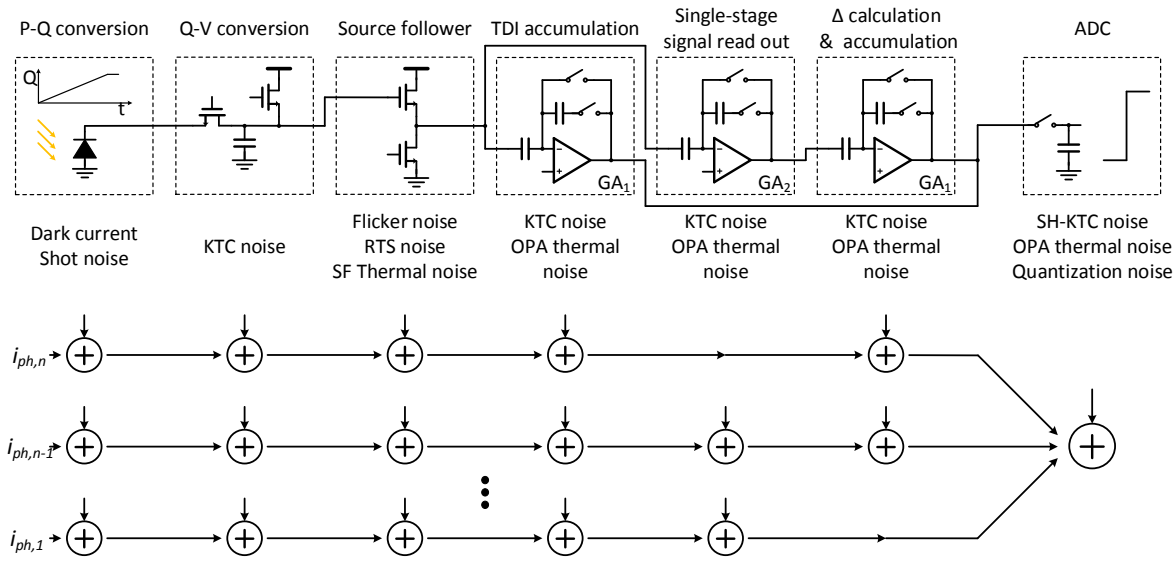


Figure 5.8: Noise model of the proposed anti-vibration TDI image sensor with ODB algorithm.

5.4.1 Source Follower

In the source follower, the gate-to-source capacitor (C_{GS}) acts as a feedback, assuming the gain of the source follower is G_{SF} [36, 142]. In the TDI operation, the thermal noise of the source follower will be sampled in the capacitors in the TDI circuits, so the mean square noise voltage in the source follower output can be expressed as [52]

$$\overline{v_{SF}{}^2} \cong {G_{SF}}^2 \xi_{SF} \frac{k_B T}{g_{m,SF}} \omega \qquad \text{(Eq. 5.11)}$$

where, k_B is the Boltzmann constant, T is the absolute temperature, ξ_{SF} is the excess noise factor of the source follower, and $g_{m,SF}$ is the source follower transconductance. ω is the cut-off angular frequency, depending on the circuit configuration.

5.4.2 TDI Accumulator

In this design, all the TDI circuits are floor planned as column-parallel type circuits, with a long, narrow layout. Given such characteristics, the parasitic capacitance of the

routing metal cannot be neglected. Five parasitic capacitances need to be taken into account: column bus parasitic capacitance C_{PC}, TDI accumulator feedback parasitic capacitance C_{PA}, single-stage memory feedback parasitic capacitance C_{PD}, and OP-AMP input parasitic capacitances C_{PIN1} and C_{PIN2}, as shown in Fig. 5.6.

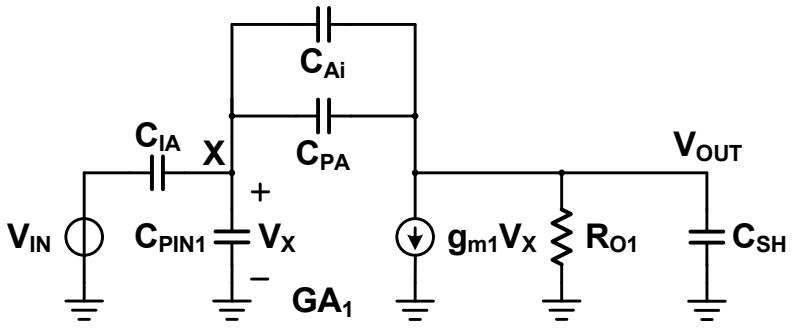


Figure 5.9: Equivalent schematic for TDI accumulator in the amplification phase of conventional TDI operation.

Fig. 5.9 shows the equivalent schematic diagram for the TDI accumulator in the amplification phase of a conventional TDI operation, where C_{Ai} is the accumulation capacitor ($i = 1, 2 \ldots 8$), and C_{IA} is the input capacitor. The gain of the TDI accumulator is thus given by

$$G_{1i} \cong \frac{C_{IA}}{C_{Ai} + C_{PA}} \qquad \text{(Eq. 5.12)}$$

Throughout the TDI operation, a given accumulation capacitor will sample the thermal noise of the source follower 8 times when reading out the pixel reset signal and 8 times when reading out the pixel photo signal. During the pixel reset signal read out, the thermal noise is sampled into the column bus parasitic capacitor C_{PC} and the input capacitors C_{IA} and C_{IC}, so the cut-off angular frequency is

$$\omega_{AR} \cong \frac{g_{m,SF}}{G_{SF}} \frac{1}{C_{IA} + C_{IC} + C_{PC}} \qquad \text{(Eq. 5.13)}$$

The noise is then transferred and sampled to the accumulation capacitor, and the mean square noise voltage is [36]

$$\overline{v_{SF,ARi}{}^2} \cong {G_{1i}}^2 G_{SF} \xi_{SF} \frac{k_B T}{C_{IA} + C_{IC} + C_{PC}} \quad \text{(Eq. 5.14)}$$

During the reading out of the pixel photo signal, thermal noise will be directly sampled into the accumulation capacitor after being amplified by GA_1. In this case, the cut-off angular frequency is

$$\omega_{AOi} \cong \frac{g_{m1} {C_{Ai}}'}{C_{SH} {C_{IN1}}' + C_{SH} {C_{Ai}}' + {C_{IN1}}' {C_{Ai}}'} \quad \text{(Eq. 5.15)}$$

where ${C_{IN1}}' = C_{IA} + C_{PIN1}$, ${C_{Ai}}' = C_{Ai} + C_{PA}$, g_{m1} is the transconductance of the operational amplifier in GA_1, and the mean square noise voltage is given by

$$\overline{v_{SF,AOi}{}^2} \cong {G_{1i}}^2 {G_{SF}}^2 \xi_{SF} \frac{k_B T}{g_{m,SF}} \omega_{AOi} \quad \text{(Eq. 5.16)}$$

Another source of thermal noise during amplification is the operational amplifier. This contribution is also sampled, and is given by

$$\overline{v_{OPA,Ai}{}^2} \cong \left(1 + \frac{{C_{IN1}}'}{{C_{Ai}}'}\right)^2 \xi_1 \frac{k_B T}{g_{m1}} \omega_{AOi} \quad \text{(Eq. 5.17)}$$

where ξ_1 is the excess noise factor of the operational amplifier, including the noise of all the internal transistors. The input-referred noise (or floating diffusion (FD) referred noise) caused by the TDI accumulator in the conventional TDI phase can therefore be expressed as

$$\overline{v_{A,total}{}^2} \cong 8 \left(\frac{\overline{v_{SF,ARi}{}^2} + \overline{v_{SF,AOi}{}^2} + \overline{v_{OPA,Ai}{}^2}}{{G_{SF}}^2 {G_{1i}}^2} \right) \quad \text{(Eq. 5.18)}$$

5.4.3 Single-Stage Memory

Synchronized by the TDI accumulation, the single-stage memory will read out the single-stage photo signal. The operation is similar to that of the TDI accumulator, the only

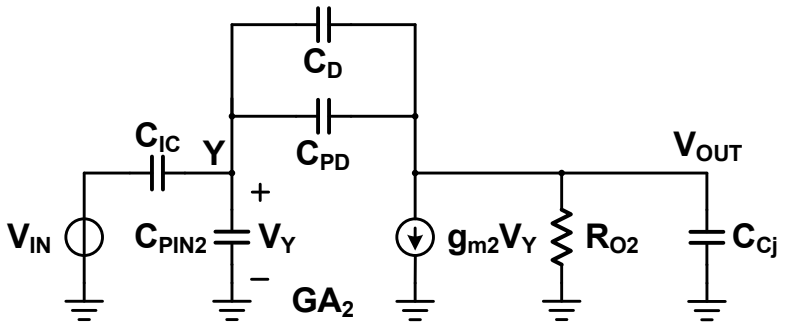


Figure 5.10: Equivalent schematic for single-stage memory in the photo signal read out phase.

differences being that the signal is read out only once, and then stored in a compensation capacitor rather than 8 times in the feedback capacitor. The equivalent schematic diagram for this phase is shown in Fig. 5.10, where C_{IC}, C_D and C_{Cj} (j = 1, 2 ... 7) are the input capacitor, feedback capacitor and load capacitor, respectively. And the gain of GA_2 is

$$G_2 \cong \frac{C_{IC}}{C_D + C_{PD}} \qquad \text{(Eq. 5.19)}$$

The mean square thermal noise voltages generated by the source follower during the pixel reset signal can be expressed as [36]

$$\overline{v_{SF,DR}{}^2} \cong {G_2}^2 G_{SF} \xi_{SF} \frac{k_B T}{C_{IA} + C_{IC} + C_{PC}} \qquad \text{(Eq. 5.20)}$$

The mean square thermal noise voltages generated by the source follower during the pixel photo signal are given as

$$\overline{v_{SF,DOj}{}^2} \cong {G_2}^2 {G_{SF}}^2 \xi_{SF} \frac{k_B T}{g_{m,SF}} \omega_{DOj} \qquad \text{(Eq. 5.21)}$$

Assuming that ${C_{IN2}}' = C_{IC} + C_{PIN2}$, ${C_D}' = C_D + C_{PD}$, and the transconductance of the operational amplifier in GA_2 is g_{m2}, then the cut-off angular frequency can be written as

$$\omega_{DOj} \cong \frac{g_{m2}{C_D}'}{C_{Cj}{C_{IN2}}' + C_{Cj}{C_D}' + {C_{IN2}}'{C_D}'} \quad \text{(Eq. 5.22)}$$

The mean square thermal noise voltage contributed by the operational amplifier in GA_2 is

$$\overline{{v_{OPA,Dj}}^2} \cong \left(1 + \frac{{C_{IN2}}'}{{C_D}'}\right)^2 \xi_2 \frac{k_B T}{g_{m2}} \omega_{DOj} \quad \text{(Eq. 5.23)}$$

where ξ_2 is the excess noise factor including the noise of all the internal transistors inside the operational amplifier.

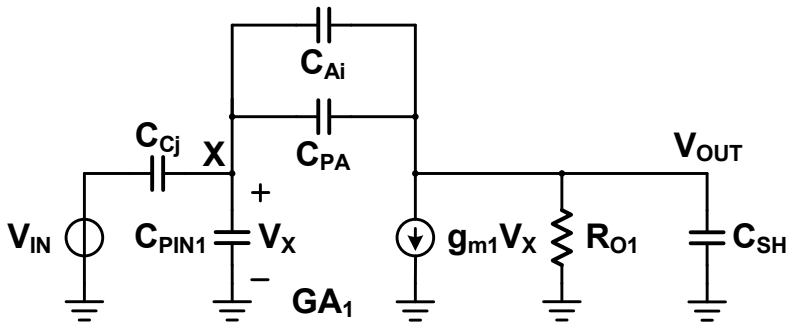


Figure 5.11: Equivalent schematic for TDI accumulator in the compensation phase.

After the single-stage signal read out, the neighboring stage signal difference is calculated and accumulated to the accumulation capacitors. Fig. 5.11 shows the equivalent schematic diagram for the TDI accumulator in this phase, in which three types of noise are introduced. The first noise source is the source follower, the thermal noise of which is amplified by the gain amplifiers in both the single-stage memory (GA_2) and the TDI accumulator (GA_1). The mean square noise voltage is thus given by

$$\overline{{v_{SF,DAj}}^2} \cong {G_{DAj}}^2 {G_2}^2 {G_{SF}}^2 \xi_{SF} \frac{k_B T}{g_{m,SF}} \omega_{DAj} \quad \text{(Eq. 5.24)}$$

where G_{DAj} is the weight parameters in Eq. 5.9, and can be defined as

$$G_{DAj} \cong \frac{C_{Cj}}{C_{Ai} + C_{PA}} \tag{Eq. 5.25}$$

And the cut-off angular frequency is

$$\omega_{DAj} \cong \frac{g_{m1} {C_{Ai}}'}{(C_{SH} + {C_{Ai}}')(C_{Cj} + C_{PIN1}) + C_{SH} {C_{Ai}}'} \tag{Eq. 5.26}$$

The second noise source is the operational amplifier in GA_2. Its noise will be amplified by the GA_1, then sampled into an accumulation capacitor. Here, the mean square noise voltage is given by

$$\overline{{v_{OPA,DAj}}^2} \cong {G_{DAj}}^2 \left(1 + \frac{{C_{IN2}}'}{{C_D}'}\right)^2 \xi_2 \frac{k_B T}{g_{m2}} \omega_{DAj} \tag{Eq. 5.27}$$

The last noise source is the operational amplifier in GA_1. The mean square noise voltage is given by

$$\overline{{v_{OPA,ADj}}^2} \cong \left(1 + \frac{C_{Cj} + C_{PIN1}}{{C_{Ai}}'}\right)^2 \xi_1 \frac{k_B T}{g_{m1}} \omega_{DAj} \tag{Eq. 5.28}$$

Considering the circuit operation, the noise generated during the pixel reset signal read out, shown in Eq. 5.20, can be partially removed during neighboring stage difference accumulation, as in the CDS operation, and the total input-referred thermal noise in a given accumulation capacitor can be expressed as

$$\begin{aligned} \overline{{v_{D,total}}^2} \cong & \sum_{j=1}^{7} \frac{\overline{{v_{SF,DAj}}^2} + \overline{{v_{OPA,DAj}}^2} + \overline{{v_{OPA,ADj}}^2}}{{G_{SF}}^2 {G_{1i}}^2} \\ & + \sum_{j=1}^{7} \frac{{G_{DAj}}^2 \left(\overline{{v_{SF,DOj}}^2} + \overline{{v_{OPA,Dj}}^2}\right)}{{G_{SF}}^2 {G_{1i}}^2} \\ & + 8 \left(\frac{\overline{{v_{SF,DR}}^2}}{{G_{SF}}^2 {G_{1i}}^2}\right) \end{aligned} \tag{Eq. 5.29}$$

According to the analysis detailed above, $\overline{{v_{A,total}}^2}$ is the thermal noise introduced by the conventional TDI operation, and $\overline{{v_{D,total}}^2}$ is the thermal noise caused by the ODB

algorithm. From Section 5.3.3, it can be seen that the conventional TDI scheme only has one operation after each integration, while, the ODB algorithm carries out two extra operations. Since the operations are executed by the gain amplifiers, the noise of one extra operation (adding neighboring stage signal difference to accumulation capacitor) could be removed. And the total thermal noise of the ODB algorithm is about twice of that of the conventional TDI scheme. These can also be verified in Eq. 5.18 and Eq. 5.29. Therefore applying the ODB algorithm would increase the noise level and decrease the dynamic range and the signal-to-noise ratio. With the number of TDI stage increases, the gain expressed in Eq. 5.9 grows, so the corresponding noise expressed in Eq. 5.28 increases. This would limit the number of TDI stages using the ODB algorithm.

5.5 Sensor Implementation

A prototype chip of 256 × 8 pixels is implemented using TSMC 0.18 μm CIS technology (1P6M). As shown in the microphotograph in Fig. 5.12, without pad ring, the functional blocks occupy a total area of 2230 × 3000 μm^2. Since many capacitors are employed per column circuit, one column would inevitably occupy a long stripe area in physical implementation. For the concern of improved column-wise matching, the column-parallel single-stage memories (gain amplifier GA_1 with the associated capacitors in Fig. 5.6) and the TDI accumulators (gain amplifier GA_2 with associated capacitors in Fig. 5.6) are placed on the top and bottom sides of the pixel array, respectively. Moreover, the stage shifter, timing controller and reference generator are arranged globally on the left side to provide the signals horizontally for the column slices. The sensor is designed with a programmable exposure time between 1 ∼ 3 ms, and readout speed of 40 M (change accordingly) pixels/second.

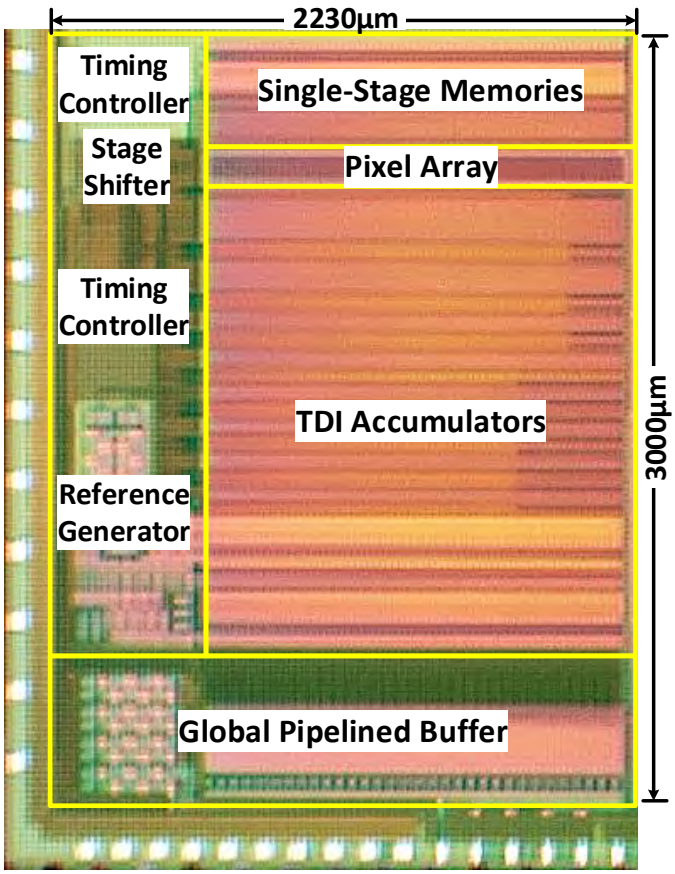


Figure 5.12: Microphotograph of the proposed anti-vibration TDI image sensor with ODB algorithm.

5.6 Measurement Result

Fig. 5.13 illustrates the vibration test platform. The whole setup is placed on an optical table in a dark room. The proposed TDI CMOS image sensor is mounted on a motor-based vibration generator, capable of making the sensor vibrate in the across-track direction with tunable frequency and amplitude. The vibration generator was fixed to a linear motor that provided uniform motion for the camera movement. During operation, the TDI sensor moves in the along-track direction at a constant speed and zigzag vibrates in the across-track direction. The target is scanned during the sensor movement,

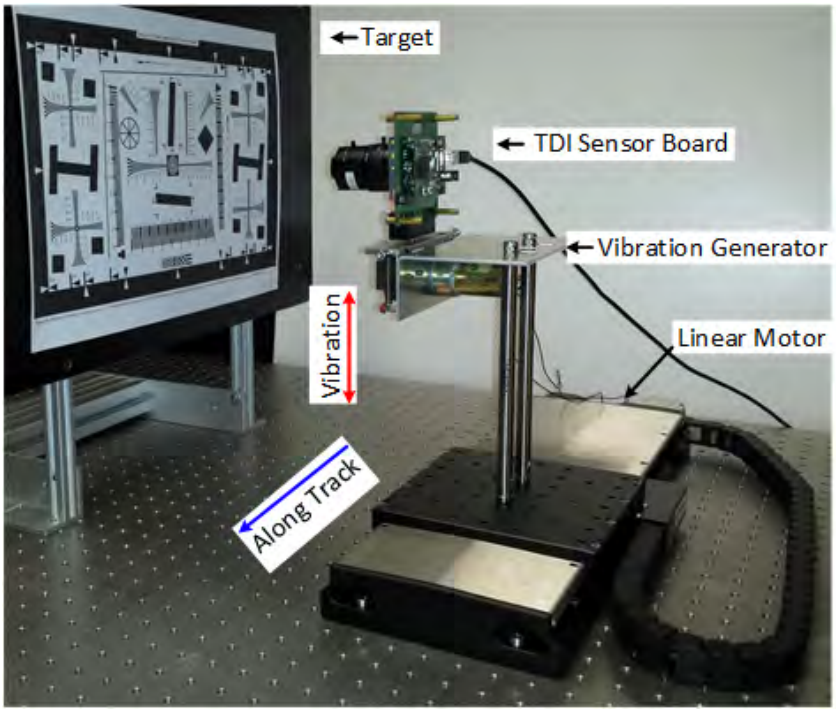


Figure 5.13: Vibration test platform for the proposed anti-vibration TDI CMOS image sensor with ODB algorithm.

and the images produced are collected by the computer.

Fig. 5.14 shows a sample image taken by the proposed 8-stage TDI image sensor in conventional mode, and Fig. 5.15 shows sample TDI images with and without vibration in the across-track direction. In accordance with the problem statement in Section 2.4.1, two mid-range vibration frequencies (50 Hz and 100 Hz), and two image shifts (1/2 pixel and 1/4 pixel) were used. The image without vibration seemed to have the best image quality ($ASF = 297$). When subject to vibration, the images manifested different levels of degradation. The images without the ODB algorithm (Fig. 5.15(c)(e)(g)) had the worst image quality: the corners and edges were blurred, and some small details, like the dash in the "f", were lost. In contrast, the images produced using the ODB algorithm (Fig. 5.15(b)(d)(f)), despite displaying geometric distortion in the across-

Figure 5.14: Sample TDI image in conventional mode without vibration.

track direction, had clear corners, sharp edges and better image quality. With the same vibration frequency, larger vibration level led to worse sharpness. In the conventional TDI scheme (Fig. 5.15(c)(e)), larger vibration made the image shifts of each TDI stage bigger, producing a blurred output image (Fig. 5.15(e)). In the ODB solution (Fig. 5.15(b)(d)), however, larger vibration levels led to wider geometric distortion, with the associated lower gradient: this explains why the ASF value of Fig. 5.15(d) is lower than that of Fig. 5.15(b). Similarly, with the same vibration level, higher vibration frequency leads to more blur, because a higher vibration frequency in a given field of view (FOV) results in a larger image shift in each TDI stage. Thus, in the conventional TDI scheme, Fig. 5.15(g) is more blurred than Fig. 5.15(e), whereas with the ODB algorithm, the ASF value of Fig. 5.15(f) is lower than that of Fig. 5.15(d). In conclusion, with vibration the conventional TDI scheme produces blurry images and lacks details, whereas the ODB algorithm, despite containing geometric distortion, can capture all the details and obtain sharp images without the help of any other devices or equipment.

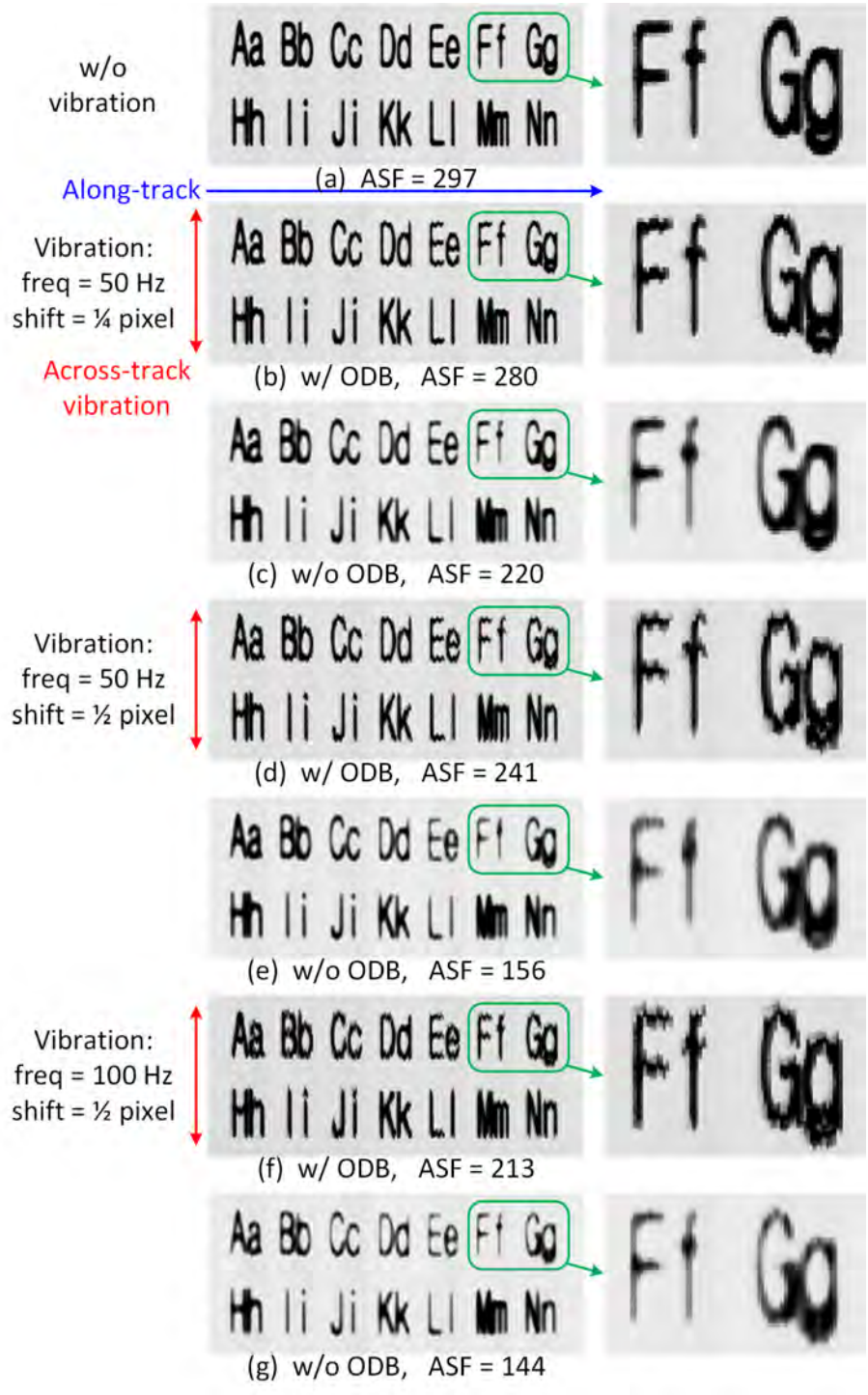


Figure 5.15: Sample TDI images without vibration and with vibration (including variable levels and frequencies).

Table 5.1: Performance summary of the proposed TDI CISes with accumulator and comparison with other design

Parameters	Chapter 5		Chapter 3	Ref. [106]	Ref. [105]	Ref. [104]	Ref. [101]
	w/o ODB	w/ ODB					
Technology	0.18 μm CIS 1P6M		0.18 μm CIS 1P6M	0.18 μm CMOS 1P4M	0.18 μm CMOS 1P4M	0.18 μm CMOS 1P4M	0.35 μm CMOS
TDI Architecture	TDI accumulator with ODB		TDI accumulator	2-step TDI accumulator	TDI accumulator	TDI accumulator	TDI accumulator
Pixel Type	4T-APS		4T-APS	-	4T-APS	4T-APS	3T-APS
Resolution	256 × 8		256 × 8 × 5	64 stages	1024 × 128	128 × 32	8000 × 25
Pixel Size	6.5 × 6.5 μm^2		6.5 × 6.5 μm^2	-	15 × 15 μm^2	15 × 15 μm^2	13 × 13 μm^2
Fill Factor	28 %		28 %	-	67 %	67 %	48 %
Max. Line Rate	1.74 kHz		1.74 kHz	-	3.875 kHz	3.875 kHz	-
Max. Data Rate	40 MHz		40 MHz	-	-	-	-
Sensitivity [1]	14769 e^-/lux·s (1.79 V/lux·s)		14769 e^-/lux·s (1.79 V/lux·s)	-	15.8 V/lux·s	3.2 V/lux·s	-
Dark Current	54.9 e^-/lux·s (6.65 mV/s)		55 e^-/lux·s (6.66 mV/s)	-	-	-	-
FPN	0.45 % (9.0 mV)	1.82 % (36.4 mV)	0.39 % (7.8 mV)	-	-	1.34 ∼ 1.98 LSB	24 ∼ 60 mV
FD-Referred Noise	42.4 e^-	91.6 e^-	40 e^-	-	-	-	-
SNR Boost to 1 Stage	8.6 dB	1.9 dB	8.8 dB	17.278 dB	9.2 ∼ 16.6 dB	11.9 ∼ 14.2 dB	-
DR	51.8 dB	45.1 dB	52.3 dB		-	40.5 ∼ 44.8 dB	-
Power Consumption	460 nJ/pixel		267 nJ/pixel	17.16 μW/pixel	129 μW/line	28 μW/line	-

[1] The numbers listed in this row are the sensitivities for single stage.

Table 5.6 summarizes the benchmark results of the prototype image sensor against a few recently reported TDI CMOS image sensors. Despite the main merits of this work that can correct the blurred image, the noise performance is not as good as the prior works. We believe that this is mainly due to the complexity of the algorithm, which involves many stages of signal amplification and addition, sample and hold, and each of which was polluted by noise. The physical implementation of the analog path results in a silicon area of 2265×6.5 μm^2 per column. The parasitic capacitance associated with the long metal bus brings in plenty of mismatch, which degrades its permanence in terms of FPN as well as noise. Leakage currents, including channel leakage of the switch transistors (e.g., S_{A1}, S_{A2} ... S_{A8}) and the leakage of the capacitors themselves, also cause loss to the stored signals. Finally, it can be noticed that this design has a higher energy dissipation (460 nJ/pixel) under the max line rate, among which, the global analog buffer consumes 47 % of the total.

5.7 Design Summary

Vibrations in the flight path can easily cause conventional TDI image sensors to lose sight of details and produce only blurry images. To solve this problem, in this chapter, an anti-vibration TDI CMOS image sensor with ODB algorithm is proposed. Differing from the conventional TDI image sensor, it can

(1) compensate for the image motion on the focal plane, and allows producing sharp TDI images without detail loss, even in complicated variation scenarios;

(2) achieve small pixel pitch and high resolution with the usage of standard 4T-APS pixel and column-parallel single-ended TDI circuits;

(3) save the capacitor quantity with the back-to-front pipeline readout methodology.

However, the online image deblurring operation is carried out by the single-stage memory, i.e., a gain amplifier. It also brings out disadvantages as follows.

(1) In the image deblurring mode, two more amplifications are needed, which would churn out more noise. Therefore, it will reduce the SNR and DR;

(2) With the TDI stage quantity rising, more capacitors are required to satisfy the weight parameter in Eq. 5.9, which will also cause more parasitic capacitance, and further undermine the performance.

Finally, the proposed method opens a door to facilitate the design of remote imaging systems by alleviating most of the design constraints associated with pointing accuracy, vibration modelling and cancellation.

Chapter 6

An Anti-Vibration TDI CIS with Low-Power Prediction ADC Scheme

6.1 Introduction

Nowadays, power consumption is turning into a serious concern, which hinders the performance of image sensors, especially, in the remote or mobile applications, such as satellite imaging, mobile devices and biomedical devices. In this chapter, a two-step prediction ADC scheme is proposed to achieve a low-power column-parallel ADC system by leveraging the spatial likelihood of natural scenes. Because in most of the natural scenarios the neighboring pixel values are similar, and therefore, a selected pixel value can be predicted by its neighbors. With the proposed prediction ADC scheme, in a given row after the first one of a frame, the MSBs of each pixel are predicted by several neighboring pixels in the previous row. Thus the original A/D conversion steps for the MSBs can be bypassed, followed by the corresponding energy saved.

The proposed two-step prediction ADC scheme has been verified in a frame-based CMOS image sensor, and then integrated into an anti-vibration TDI sensor similar to

that one introduced in Chapter 5. To avoid the photo signal saturation caused by bright scenes, the ADC structure is modified together with the TDI accumulator to perform adaptive TDI stages, as well as the adaptive integration time.

In this chapter, Section 6.2 introduces the two-step prediction ADC scheme in detail firstly. After that Section 6.3 describes the frame-based CMOS image sensor design for ADC scheme verification, then Section 6.4 and Section 6.5 discuss the implementation and measurement result for the frame-based CMOS image sensor. Next, an improved anti-vibration TDI CMOS image sensor design with the proposed prediction ADC scheme is described in 6.6. Finally, 6.7 sums up this whole chapter.

6.2 Two-Step Prediction ADC Scheme

Compared to conventional ADC designs, the proposed two-step prediction ADC design saves power by taking advantage of the limited spatial frequency of natural images. To implement the two-step prediction ADC in image sensors, a system-level low power design method is proposed and characterized.

6.2.1 Algorithm Background

In images of natural scenes, the spatial frequency is often limited because a group of pixels in the image can be occupied by the same object. This means that most of the pixels in the image could have similar values to their neighboring pixels. For example, in a satellite image for remote sensing applications, a group of pixels usually have similar values. In reality, in such cases sometimes most of the pixel values have very small differences. Moreover, the difference of neighboring pixel values could be reduced by the limited optical systems or resolution of a camera. To verify this, hundreds of images were simulated to calculate the differences between neighboring pixels using MATLAB

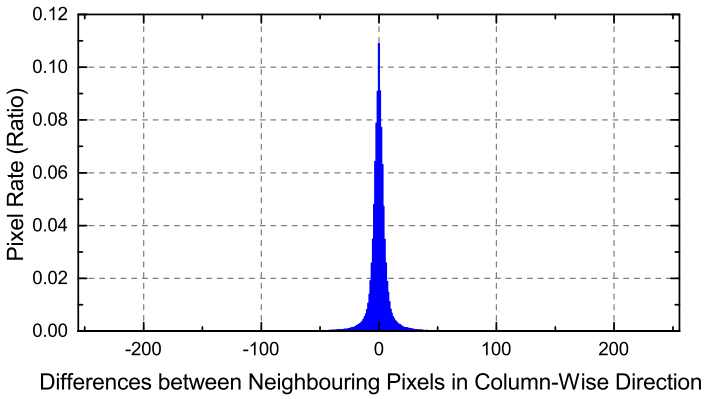


Figure 6.1: Distribution graph of neighboring pixel difference in column-wise direction for Lena (resolution 512 × 512).

program. The result shows that there is a high percentage of pixels having similar values to their neighboring pixels. For instance, the result of a *Lena* image with a resolution of 512 × 512 is shown in Fig. 6.1. Although the image contains a mixture of detail, flat regions, shading and texture [144], Fig. 6.1 shows that most of the neighboring pixel value differences in the column-wise direction distribute in the range between -50 to +50 out of the range of [-255, +255]. Therefore, the digital pixel value differences in the image are mainly attributed to the LSBs.

However, conventional ADC structures in CMOS image sensors do not consider the aforementioned image property. For example, in conventional SAR ADC operation, the capacitor array of the DAC needs to be reset (discharged) between every two conversions. Similarly, in conventional single-slope ADC operation, after one conversion, the DAC also needs to be reset (charged or discharged depends on the specific design) to the edge in order to start the next conversion. The operations of a SAR ADC and a single-slope ADC are shown in Fig. 6.2. Unfortunately, with such operations, when the neighboring pixels in the same column have the similar values, the charging/discharging energy between the two consecutive comparisons are wasted. This unnecessary discharge energy can be avoided if the consecutive conversions share several MSB values. Also, in such scenarios,

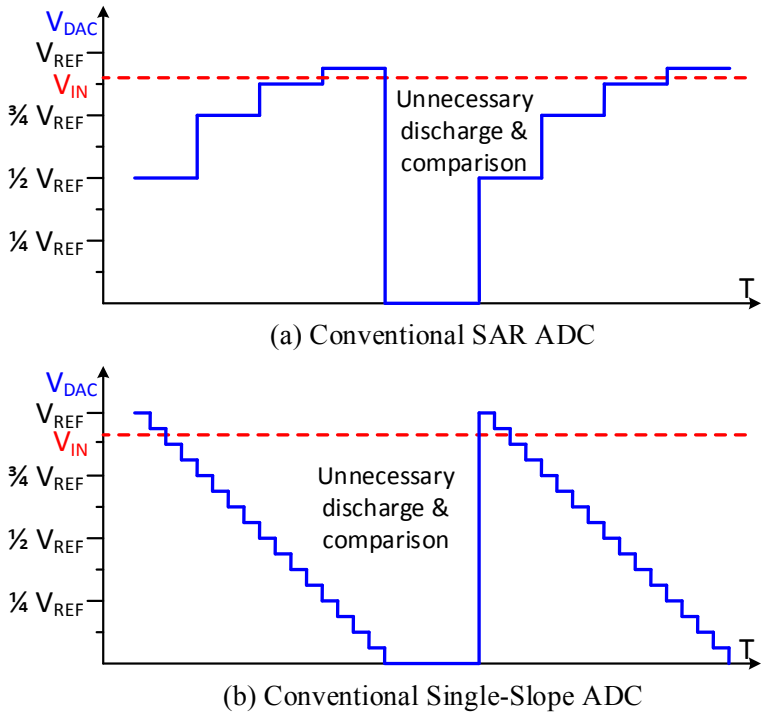


Figure 6.2: 4-bit DAC voltage outputs of (a) Conventional SAR ADC and (b) Conventional single-slope ADC between two neighboring conversions.

the comparison energy of these MSBs can also be saved. Based on these considerations, the two-step prediction ADC scheme for image sensors is proposed.

6.2.2 Algorithm Description

The proposed two-step prediction ADC scheme is based on the strong correlation between consecutive pixels of the same column in the natural scenes to reduce conversion steps and avoid unnecessary discharge between conversions by predicting some MSB values of each conversion. As illustrated in Fig. 6.3, the proposed two-step conversion algorithm processes the pixel array by rows. In *Step* 1, the pixel values of each row serve as references for predicting pixel values of the subsequent row. In other words, the common MSBs of several neighboring pixels from the previous row are generated as the prediction for an individual pixel in the next row. For instance, the prediction process starts on

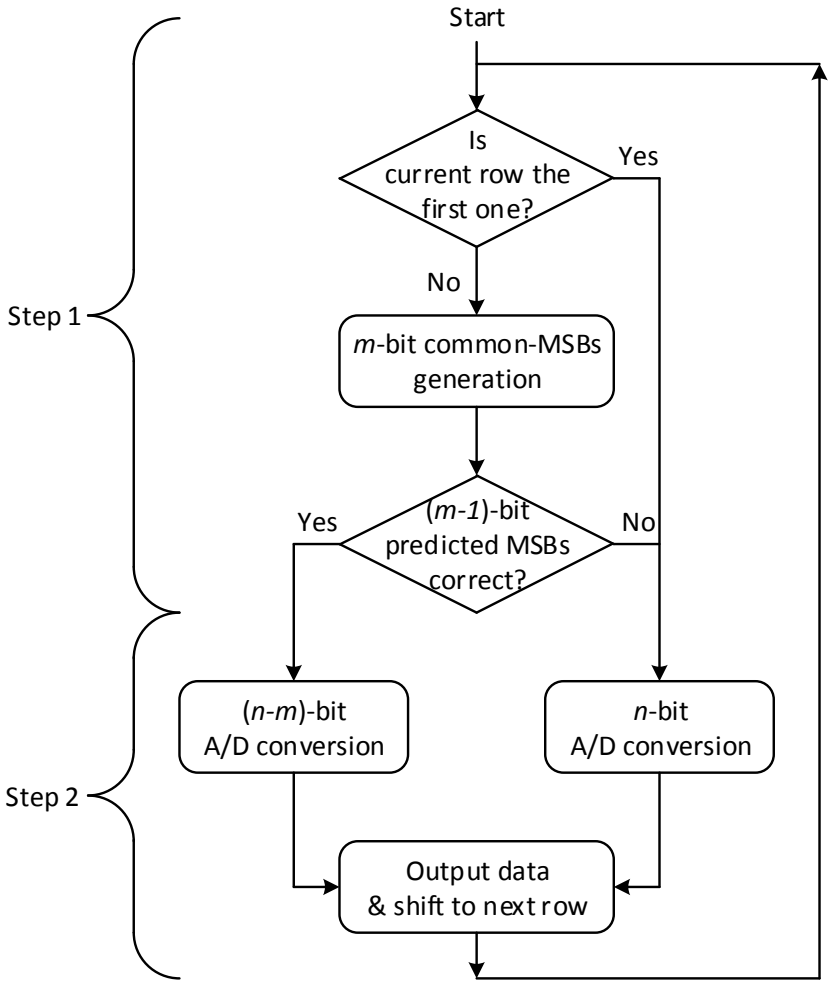
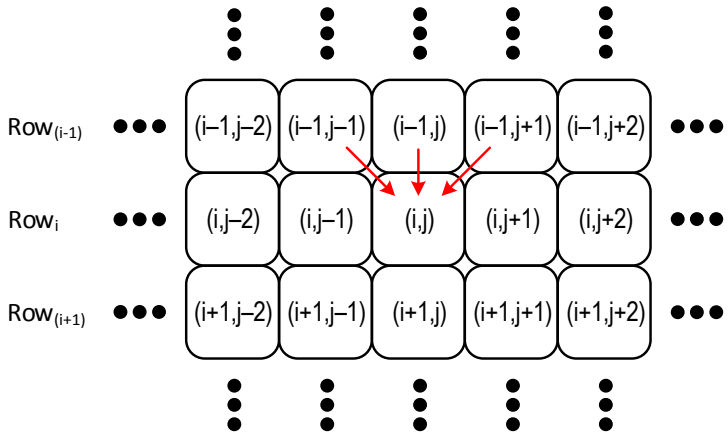


Figure 6.3: Operation procedure of the proposed two-step prediction ADC scheme.

the second row while the first row pixel values are used as references. In *Step* 2, if the predicted MSB values are correct, only a partial A/D conversion is required, and the conversion energy of the MSB processes can be saved. Otherwise, a full A/D conversion of the current pixel is necessary.

A detailed example of the first step process is described in Fig. 6.4. In order to obtain the digital value of *Pixel* (i, j) at Row_i Col_j, the available digital values of its three neighboring pixels from the previous row (Row_{i-1}) are selected as references. The three pixels are $(i-1, j-1)$, $(i-1, j)$, and $(i-1, j+1)$. For m-bit common MSBs in



Pixel (i–1, j–1)	1	0	1	0	1	1	0	0	0	1
Pixel (i–1, j)	1	0	1	0	0	1	0	1	0	0
Pixel (i–1, j+1)	1	0	1	0	1	0	1	1	1	1
m-bit Common MSBs	1	0	1	0	×	×	×	×	×	×
(m-1)-bit Predicted MSBs	1	0	1	×	×	×	×	×	×	×

Figure 6.4: Prediction example of the proposed two-step prediction ADC scheme.

the reference, only (m-1)-bit common MSBs are used for the prediction. In this example, the three reference pixels share 4-bit common MSBs, only the first 3 bit common MSBs is taken as the prediction for the MSB values of the *Pixel* (i, j). For instance, as shown in the lower part of Fig. 6.4, the common MSBs of the three pixels are "1010" while the prediction bits are "101". This design is for avoiding the prediction error caused by a small difference between neighboring pixels due to FPN, non-uniformity or other noise as well as increasing the prediction accuracy. This has been verified by MATLAB simulations with a number of natural images.

After obtaining the predicted MSB values, a DAC is used to judge whether the predicted MSB values are correct or not. This is done by comparing the pixel's analog value with two boundary voltages generated by the DAC. The predicted MSB values are considered as correct if

$$V_P < V_{IN} < V_P + \frac{1}{2^m} V_{REF} \quad \text{(Eq. 6.1)}$$

where V_{IN} is the analog value of the pixel, V_P is the analog value generated by the DAC based on the predicted MSB digital values, V_{REF} is the DAC reference voltage as well as the full analog input value range, and m is the number of the predicted MSBs. Since the pixel digital value is expressed in binary form, if the predicted MSB values are correct, V_{IN} must be in the range between V_P and $(V_P + 1/2^m \times V_{REF})$. Taking a 5-bit ADC as example, assuming that the prediction is "01XXX", the allowable range of the input would be $(1/4V_{REF},\ 1/2V_{REF})$. Otherwise, the prediction is wrong. This prediction judgement result concludes the first step of conversion.

In the second step of the conversion, the final conversion result is obtained based on the prediction judgement result. If the prediction is correct, then only (n-m)-bit LSB A/D conversions are applied to obtain the remaining quantization values, where n is the number of bits of the ADC and m is the number of bits of the predicted MSBs. Otherwise, a full conventional n-bit A/D conversions are performed to obtain the digital values of the pixel. After conversion, the final digital values are stored in a data memory for predicting the MSB values of pixels in the next row.

6.2.3 Algorithm Implementation

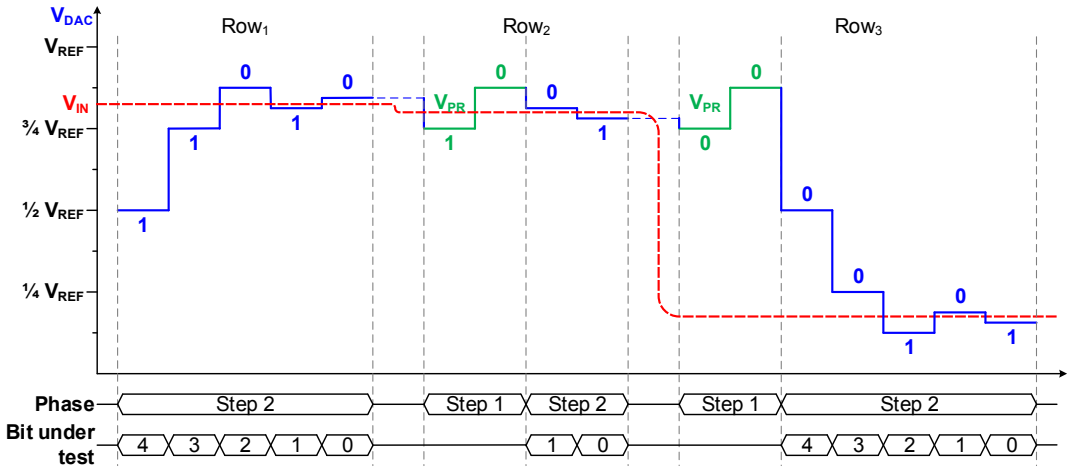
The proposed prediction ADC algorithm contains three key procedures: prediction, judgement, and final conversion. At the beginning, the prediction circuit generates common MSBs from the data memories that store the digital results of the pixels in the previous row. Then the judgement circuit creates two analog boundary voltages based on the predicted MSB values and check whether the current pixel's analog value is between the two boundary voltages based on Eq. 6.1. Finally, if the predicted MSB values are correct, the ADC only performs the LSB conversions. Otherwise, the ADC performs

a full A/D conversion. This algorithm can be implemented with various time-domain ADC structures, e.g., single-slope ADCs or SAR ADCs. Also different data structures can be applied in the data memory.

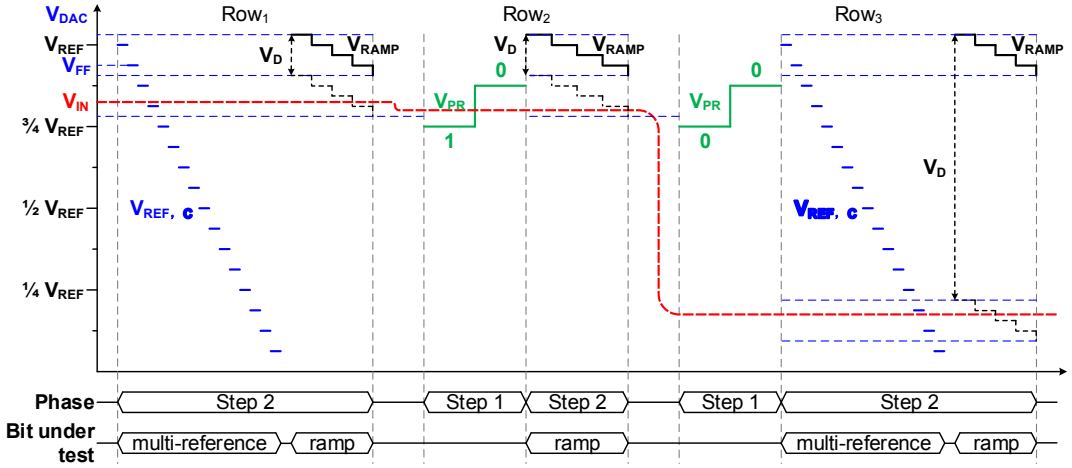
There are two options for implementing the proposed algorithm, local DAC implementation and global DAC implementation for coarse conversion and prediction judgement. When choosing the implementation options, speed, circuit area, and power consumptions are the main considerations. For the prediction circuit, since the input pixel value varies column by column, the circuit should be implemented locally. Another reason for doing this is that the prediction circuit is fully digital and does not occupy too much silicon area. In the case of the judgement circuit, it can be implemented either locally or globally depends on the specific design requirements. In a local implementation, the DAC can be combined with the column ADC, while in a global implementation, multiple reference voltages can be applied and broadcasted to all the column slices globally. This can be achieved by using a voltage scaling DAC.

Examples of implementation options with different ADC types are shown in Fig. 6.5. In these examples, a 5-bit conversion is applied with the same input signal and the same scenario: (1) In Row_1, since there are no previous rows, the prediction is not available, the conversion starts with the second step, which is a complete A/D conversion. (2) In Row_2, the first step prediction is successful. So in the second step, only a partial A/D conversion needs to be performed. (3) In Row_3, the first step prediction is failed and thus a complete A/D conversion is performed in the second step.

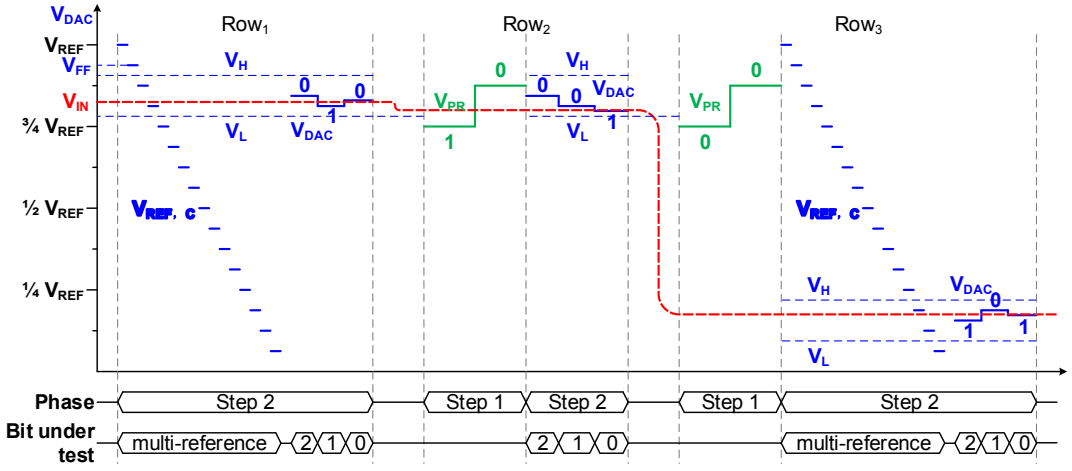
In the first example of Fig. 6.5(a), a local DAC is applied to the judgement circuit for *Step* 1 and an SAR ADC is used for *Step* 2. In the conversion of Row_1, a full SAR A/D conversion is performed. A simplified schematic of the SAR ADC is shown in Fig. 6.6. At the beginning of the conversion, switch S_R is turned on and switches S_0, S_1, S_2, S_3, and S_4 are connected to GND to reset the capacitor array. Then S_R is turned off,



(a) Step 1: local DAC for coarse conversion and prediction judgement, Step 2: local SAR ADC for fine conversion



(b) Step 1: global DAC for coarse conversion and prediction judgement, Step 2: local single-slope ADC for fine conversion



(c) Step 1: global DAC for coarse conversion and prediction judgement, Step 2: local SAR ADC for fine conversion

Figure 6.5: Examples of the proposed algorithm with different implementations.

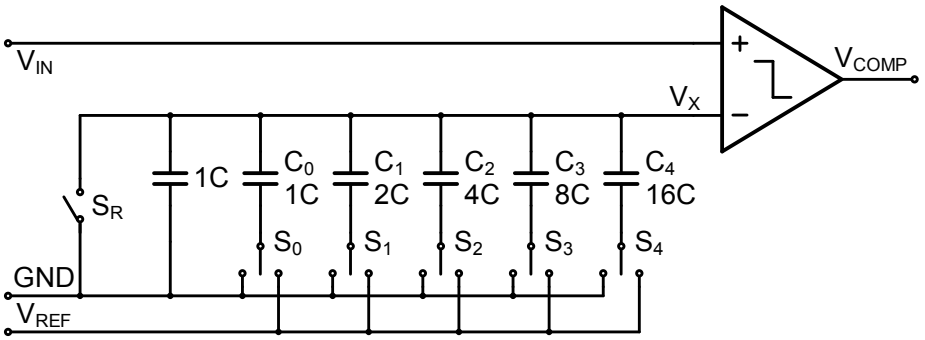


Figure 6.6: Simplified schematic of SAR ADC for local DAC implementation with the proposed prediction scheme.

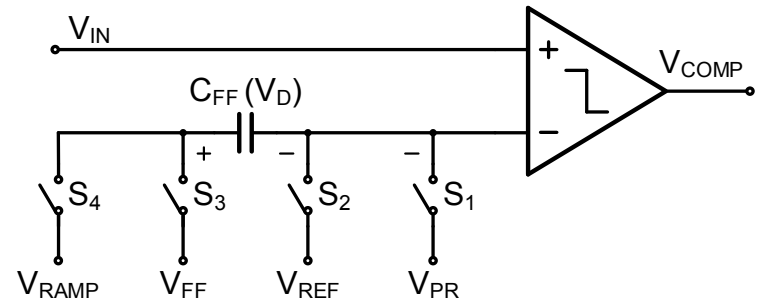
and $S_4 \sim S_0$ are sequentially switched to V_{REF}. During this process, if V_{COMP} is 1 then the switch remains at V_{REF}, otherwise, it turns back to GND. The final position of $S_4 \sim S_0$ is the conversion result.

Next, in the conversion of Row_2, assume the prediction circuit picks up the first three MSB values from Row_1 as a prediction (in this case "110XX"), the judgement is performed by keeping S_2 (the third bit) to GND to generate the lower boundary voltage at V_X, and switching S_2 to V_{REF} to generate the high boundary voltage at V_X. And During the judgement process, if V_{COMP} toggles, i.e., the first result is "1" and the second result is "0", then it means V_{IN} is within the window between the high boundary and the low boundary. And thus, the prediction is correct. So a partial conversion starts from the fourth bit, which means only S_1 and S_0 need to be adjusted to complete the A/D conversion. After that, in the conversion of Row_3, the same prediction and judgement processes are performed, however as shown in Fig. 6.5(a), the judgement results are "0" and "0", which means the prediction is failed. Thus, a complete A/D conversion has to be performed. Although there are two extra switchings and comparisons due to the failed prediction, viewing from the whole image the total energy can be greatly saved because of the limited spatial frequency of the natural scene. Moreover, if a higher resolution ADC is required, power could be further reduced due to a higher number of MSBs saved

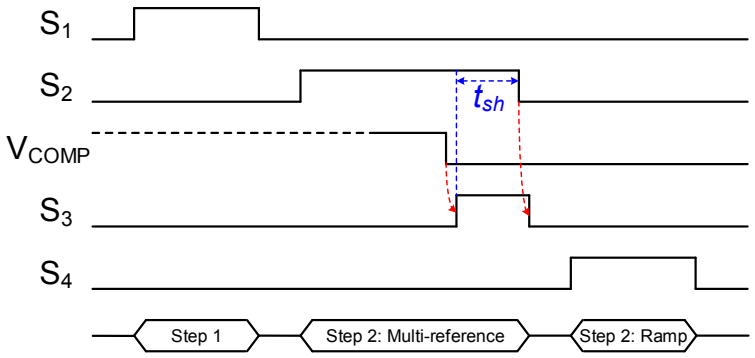
in the prediction.

Besides SAR ADCs, single-slope ADCs can also be used in the proposed two-step prediction scheme. In the example illustrated in Fig. 6.5(b), a single-slope ADC is combined with a global DAC. Similarly to the previous example, in Row_1 a complete single-slope A/D conversion is performed. The single-slope A/D conversion is divided into two parts: a coarse conversion and a fine conversion [145]. Both the coarse conversion and fine conversion use a linear search protocol. In the coarse conversion, a global multi-reference generator generates the comparison reference $V_{REF,C}$ which contains 16 voltages coming in serial. These voltages are compared to the input signal one by one to obtain the coarse conversion results, which represent the MSB values. After the coarse conversion, the fine conversion is performed by comparing a ramp signal V_{RAMP} to the input voltage. V_{RAMP} is generated by a global ramp signal generator. In this example, V_{RAMP} is shifted to the input signal based on the result of the coarse conversion. Fig. 6.7 illustrates the simplified schematic and the corresponding timing diagram. Here V_{FF} is a voltage following V_{REF}, V_{FF} equals to $15/16V_{REF}$ ($(2^n-1)/(2^n) \times V_{REF}$ for n-bit coarse resolution). V_{PR} is the analog boundary voltage for judgement, and is selected from the global multiple references by the predicted MSBs. The global ramp generator and multi-reference generator can be turned off after A/D conversion for power saving.

The operation of the two-step prediction single-slope ADC is described as follows with Fig. 6.7 illustrating the simplified schematic and corresponding timing diagram. To perform the coarse quantization, switch S_2 is turned on, S_1, S_3 and S_4 are turned off. So the capacitor C_{FF} is floating and the 16 global reference voltages are connected to $V_{REF,C}$ sequentially to compare with the input voltage (V_{IN}). During this linear searching and comparison process, once the comparator V_{COMP} is triggered, S_3 is turned on so the C_{FF} can store the voltage difference (V_D) between the current reference voltage $V_{REF,C}$ and V_{FF}. After the coarse quantization, S_2 and S_3 are turned off sequentially. Then the



(a) Simplified schematic of the global DAC implementation



(b) Timing diagram of the global DAC implementation

Figure 6.7: (a) Simplified schematic and (b) Timing diagram of the single-slope ADC for gllobal DAC implementation with the proposed prediction scheme.

fine quantization begins. A global ramp voltage V_{RAMP} is connected to C_{FF} by turning on S_4. The global ramp voltage covers a 1-bit voltage range of coarse quantization. To avoid the missing code around the boundaries, in this example, the quantization range for the fine part is extended twice, half to the upper boundary and half to the lower boundary. The final quantization result for Row_1 can be calculated by the combination of the coarse quantization and the fine quantization. In conversions for Row_2, since quantization of Row_1 has been completed, the prediction result V_P for Row_2 is available from the prediction circuit. Then the judgement circuit judges whether the prediction is correct or not. This is done by turning on S_1 while S_2, S_3, and S_4 are turned off. During this time, V_P and $(V_P + 1/8 \times V_{REF})$ are connected to V_{PR} sequentially to compare with V_{IN}. Here the comparison results are "1" and "0", which means the prediction is correct.

So only a partial A/D conversion is necessary. In this case, this means only the fine quantization is required for Row_2. A similar judgement process is performed for Row_3. However with the judgement result to be "0" and "0", the prediction is failed. Thus a full A/D conversion in performed. Compared to the SAR ADC implementation, in this example the number of bits in the coarse quantization, which is the same number of bits for prediction, is fixed. This lost the flexibility of prediction. So the power efficiency cannot be improved with an optimized number of prediction bits when a single-slope ADC and the linear search protocol are used in the two-step prediction architecture.

In addition to the single-slope ADC, the global DAC solution is also suitable for other local ADC architectures, which is easier to be implemented without much modification. For instance, Fig. 6.5(c) describes the DAC voltages for a global DAC solution with local SAR ADC in column slices. The prediction generation, judgment and the coarse quantization are the same as that in the single-slope structure. The only difference is the fine quantization step. In the previous example of the single-slope ADC, C_{FF} is used to provide a DC shift of V_{RAMP} so it can be compared to V_{IN} in each column slice. While in this example, the DAC voltage is generated locally by the switched-capacitor array. Since the input voltage range of an SAR ADC is determined by the reference voltages, the capacitor array can be connected to various reference voltages depends on the coarse MSBs to perform further fine quantization, that means V_{REF} and GND terminals in Fig. 6.6 are connected to V_H and V_L in Fig. 6.5(c), respectively. In this example, the number of coarse MSBs (the number of global reference voltages) is important to optimize the total power consumption. In addition, since the average power consumption depends on the column resolution of an image, a higher resolution can reduce the shared power consumption of one single column ADC.

Comparing with the global DAC solution, the energy consumed by the global DAC and buffer can be saved in the local DAC solution. This means that the local implementation of the two-step prediction ADC scheme is more energy efficient.

6.2.4 Algorithm Simulation

The power consumption of the proposed two-step prediction ADC has been simulated using MATLAB. According to the aforementioned discussion, the local SAR ADC topology shown in Fig. 6.5(a) is selected because of a lower power consumption. Based on the circuit shown in Fig. 6.6, the power cost in this topology can be divided into three parts: the switched-capacitor array, the comparator, and the digital circuits. Since the comparator and digital circuits consume almost the same energy for different bits of the ADC code, leaving only the switching energy of the capacitor array is to be simulated.

Power analysis of the switched-capacitor array is based on the charging and discharging energy during A/D conversion. Referring to Fig. 6.6, before conversion, the capacitors are reset to GND. The conversion starts when S_R is turned OFF. In the first bit conversion, the bottom plate of capacitor C_4 is switched to V_{REF}, and V_X is charged to $1/2V_{REF}$. This switching energy is $8CV_{REF}{}^2$. At this moment, if $V_{IN} > V_X$, then C_4 is kept to V_{REF} and C_3 is switched to V_{REF}, so V_X is charged to $3/4V_{REF}$. In this case, the switching energy of this step is $2CV_{REF}{}^2$. Else if $V_{IN} < V_X$, C_4 is switched back to

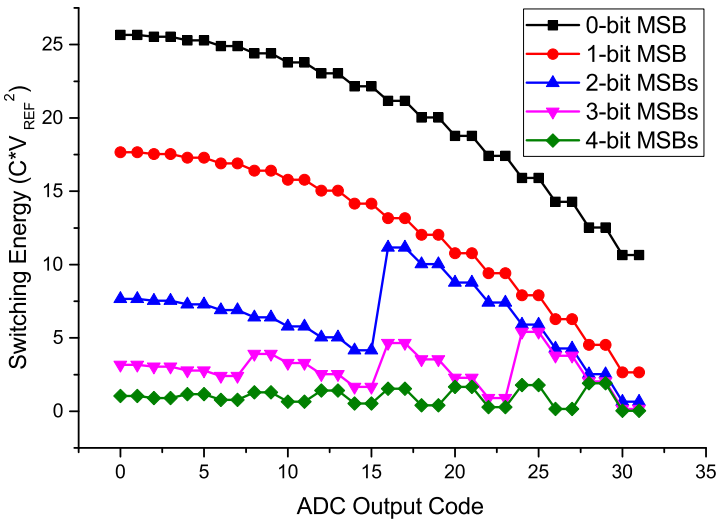


Figure 6.8: Switching energy versus ADC output code for a conventional SAR ADC shown in Fig. 6.6.

GND and C_3 is switched to V_{REF}, so V_X becomes $1/4V_{REF}$. In this case, the switching energy of this step is $10{CV_{REF}}^2$. Then the next step is to compare V_X and V_{IN} to decide the following bits. With this analysis, the switching energy of all the ADC output code is simulated with various numbers of predicted MSBs. The simulation result of this 5-bit conversion is shown in Fig. 6.8. From top to bottom, the five curves represent the switching energy with no prediction, 1-bit, 2-bit, 3-bit, and 4-bit MSB predictions. The simulation results shown that the switching energy can be reduced with more numbers of predicted MSBs.

6.3 Image Sensor Design

6.3.1 Sensor Architecture

A prototype CMOS image sensor was designed using AMS 0.35 μm CIS technology implementing the proposed prediction algorithm with local SAR ADCs in column slices. Fig. 6.9 shows the sensor architecture diagram, which mainly contains six principal components: a 3T-APS pixel array with 384 × 256 resolution, a column-parallel DDS and sample-hold circuit array, a column-parallel SAR ADC array, two sets of column-parallel memories, a row scanner and a basic timing and reference generator.

In the operation, the basic timing and reference generator would provide all the timing signals and analog biasing and reference voltages to the other building blocks. The exposure time is controlled by the basic timing generator and external exposure control signals. After the exposure, the row scanner would start to scan the pixel array row by row from the first one for photo signal reading out.

The signals in the photodiode would be first processed by a DDS circuit to remove the FPN and low frequency noise [46–48], then be sampled for further quantization. Before

the quantization, the logic circuit in each column would generate the predicted MSBs from the previous-row data stored in *Memeory* 2. Then the prediction correctness would be decided by comparison between the prediction boundaries and the sampled photo signal, based on the result of which a full (with wrong prediction) or partial (with right prediction) A/D conversion is then executed. Finally, the quantization results would be stored into *Memory* 1 for output, and into *Memory* 2 for next-row prediction generation. After that, the row scanner would shift to the next row until the full image is digitized.

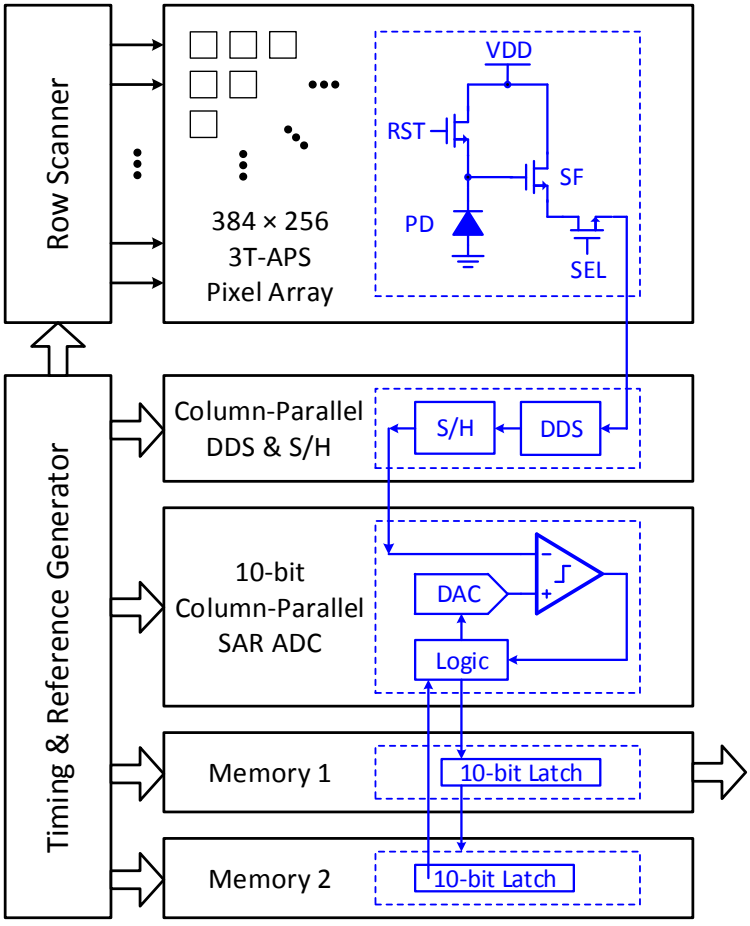
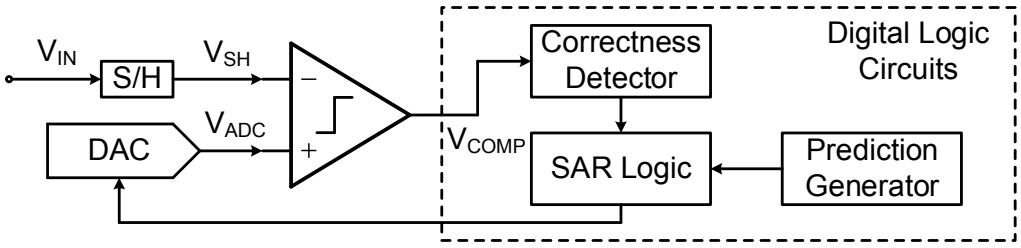


Figure 6.9: Architecture diagram of the frame-based CMOS image sensor with the proposed two-step prediction ADC scheme.

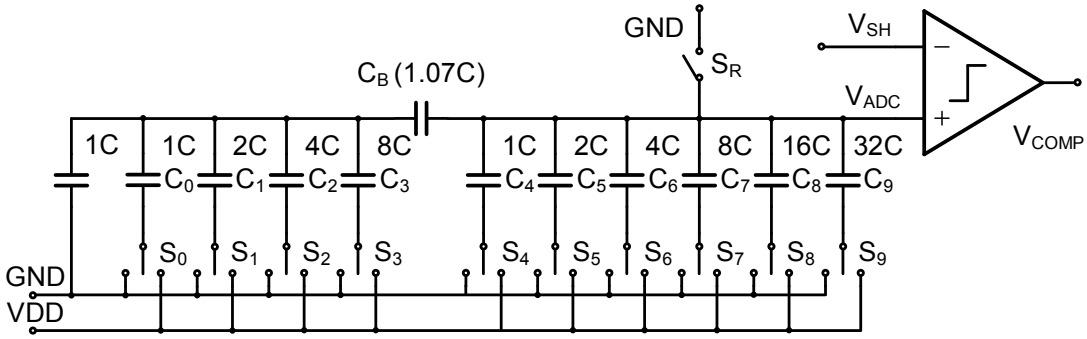
6.3.2 ADC Architecture

SAR ADCs are used in the image sensor with small modifications to implement the proposed two-step prediction algorithm. Fig. 6.10 shows the simplified architectures diagram of the proposed SAR ADC cell and switched-capacitor DAC with prediction scheme. Fig. 6.10(a) shows the architecture diagram of the SAR ADC cell. In this design, the prediction generating and judgment circuits are combined with the SAR logic cell, and only two more digital logic blocks (prediction generator and correctness detector) are added, which bring minimum effect to the original ADC after applying the prediction scheme. The prediction generator will calculate the common MSBs from the three neighboring pixels' digital data in the previous row. During the prediction verification, the prediction generator controls the DAC to generate the corresponding voltages through the SAR logic. After the comparison, the correctness detector will pass the result to the SAR logic circuit. If the prediction succeeds, then the prediction generator will write the 1-bit less common MSBs to the SAR logic; else, if the prediction fails, the prediction generator will reset the SAR Logic. Then, the SAR logic would take over the controlling of the DAC and finish the quantization. Since the remaining A/D conversion still works with binary search protocol, the SAR logic circuit remains the same as the conventional one.

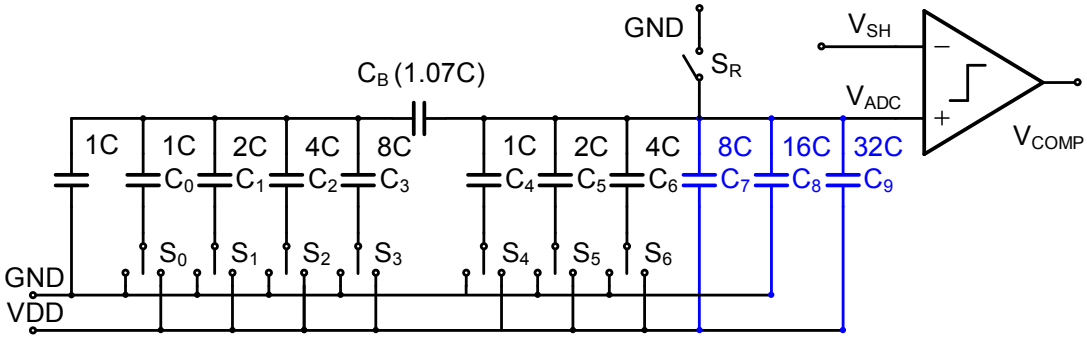
In order to reduce power consumption, a single-ended split switched-capacitor array rather than a fully differential one is employed in the ADC with a dynamic comparator. The schematic of the switched-capacitor array with the comparator is shown in Fig. 6.10(b). The 10-bit split-capacitor structure is applied with 6-bit MSBs and 4-bit LSBs. Thus, the capacitor array contains total 80.07 unit capacitors. In this design, a unit capacitor C is 43.688 fF. The maximum equivalent capacitor observed between the top and the bottom plates of capacitor array is $64C$. The split-capacitor structure reduces power consumption and silicon area compared to a regular capacitor array. On the other



(a) Architecture diagram of the SAR ADC cell



(b) Schematic of the switched-capacitor DAC and the comparator



(c) Schematic of the switched-capacitor DAC with 3-bit Prediction (101XXXXXXX)

Figure 6.10: Architecture diagram of the column-parallel SAR ADC cell and the detailed schematic.

hand, to reduce circuit complexity and power consumption, reference voltage generators are removed [79],and the reference voltages in the SAR ADC are directly connected to the power supply, i.e., $V_{REF} = VDD$.

Since both the prediction and judgement circuits are fully digital and no other extra analog or digital circuits are added into the ADC, the two-step prediction ADC only brings negligible extra circuit complexity and silicon area compared to the conventional SAR ADC. Fig. 6.10(c) shows an example of a successful prediction "101XXXXXXX", within which the three capacitors C_9 ($32C$), C_8 ($16C$) and C_7 ($8C$) are pre-assigned to "101" after the prediction and judgement. So these three capacitors are excluded from the remaining binary searching steps, and the corresponding switching energy introduced by charging or discharging these three capacitors can be eliminated from the system power consumption. Since these capacitors take most of the capacitance in the capacitor array, the proposed prediction method could significantly reduce the switching energy.

6.4 Sensor Implementation

The image sensor with the two-step prediction ADC scheme was fabricated using AMS 0.35 μm CIS process (2P4M). Fig. 6.11 shows a microphotograph of the prototype chip, whose area is 7380×6840 μm^2. The sensor has a resolution of 384×256 and one slice of ADC for each pixel column. One column slice contains DDS circuit, S/H circuit, SAR ADC and two sets of memories. The pixel pitch, as well as the column slice pitch, is 15 μm, which is a big size for image sensor. This is because that the image sensor is targeted for optical applications, and the big-size photo detector can grantee large fill factor as well as enough photo-detective area. Moreover, to achieve higher SNR, configurable gains 2, 4 and 8 are implemented to the DDS circuit.

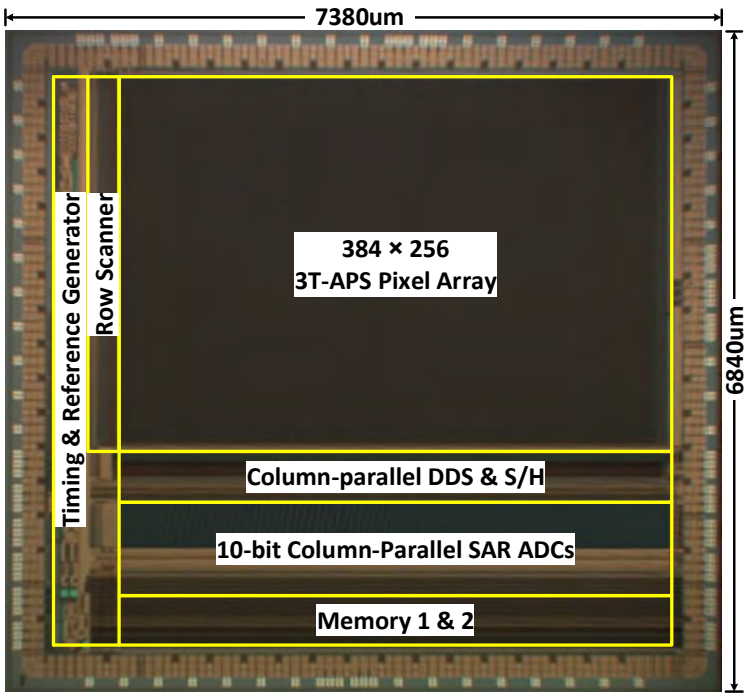


Figure 6.11: Microphotograph of the frame-based CMOS image sensor with the proposed two-step prediction ADC scheme.

6.5 Measurement Result

6.5.1 Sensor Performance

Table 6.1 lists the basic performance summary of the proposed image sensor. The listed frame rate is decided by the readout speed. For the optical requirement, the effective exposure time should be longer, thus in real applications, the main clock frequency and frame rate can be lower. The 0.35 μm CIS process only provides 3.3 V power supply, which is a high voltage for digital circuit and would lead to higher digital circuit power consumption. The power consumption could be further reduced when a low digital power voltage is available.

Table 6.1: Performance summary of the frame-based CMOS image sensor

Technology	0.35 μm CIS 2P4M
Pixel Type	3T-APS
Resolution	384 × 256
Pixel size	15 × 15 μm^2
Fill Factor	49 %
Clock Frequency	50 MHz
Frame Rate	381 fps
Sensitivity	686 mV/lux·s
Dark Current	26 mV/s
FPN	0.79 %
Read Noise	2.77 mV_{rms}
Dynamic Range	58 dB
Supply Voltage	3.3 V
Energy Consumption	463 pJ/pixel

6.5.2 ADC Performance

The column-parallel ADC unit in this design are characterized in Table 6.2. The ADC effective input range which is the output range of the DDS circuit is 0.8V $\sim$ 3.1 V. Since the reference voltages of the capacitor array is directly connected to the power supply voltage (3.3V) and ground in order to avoid the extra power consumption caused by the reference generator and reference buffers, nearly 30% of the ADC input range is wasted. The linearity of the ADC in terms of DNL and INL is measured and illustrated in Fig. 6.12. The DNL and INL measurement results are given in Fig. 6.12. The adopted split-capacitor DAC although reduces the number of the total capacitors to a great extent,

Table 6.2: Performance summary of the column-parallel SAR ADC

Resolution	10 bits
Sample Rate	1.79 MHz
Effective Input Range	0.8 $\sim$ 3.1 V
DAC reference	0.0 / 3.3 V
Unit capacitance	43.688 fF
DNL	+0.73/-0.60 LSB
INL	+2.60/-2.43 LSB

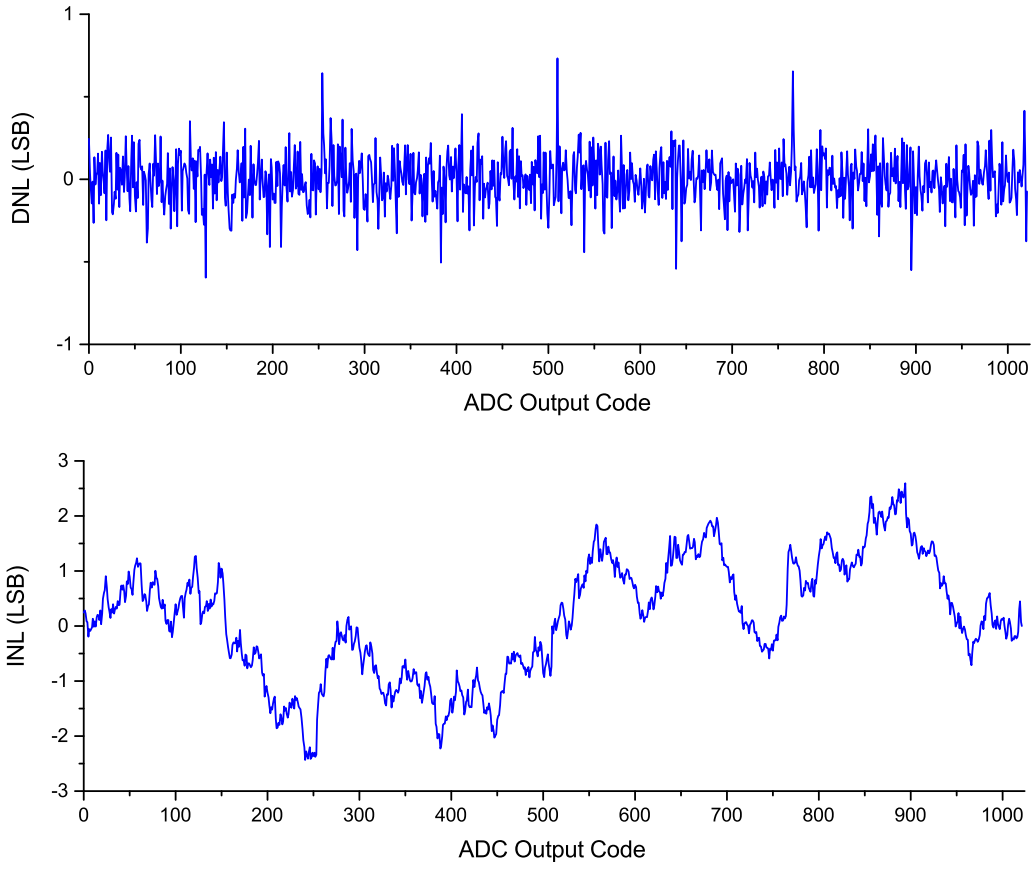


Figure 6.12: DNL and INL (normalized to the LSB) of the column-parallel SAR ADC.

it makes the ADC more vulnerable to the random capacitor mismatches as well as the parasitic capacitances associated with the LSB node and the split capacitor. These non-idealities are even worse when the whole ADC must be placed into a very narrow column slice in the layout. As a result, the linearity of the ADC is restricted to about 2.6 LSB INL.

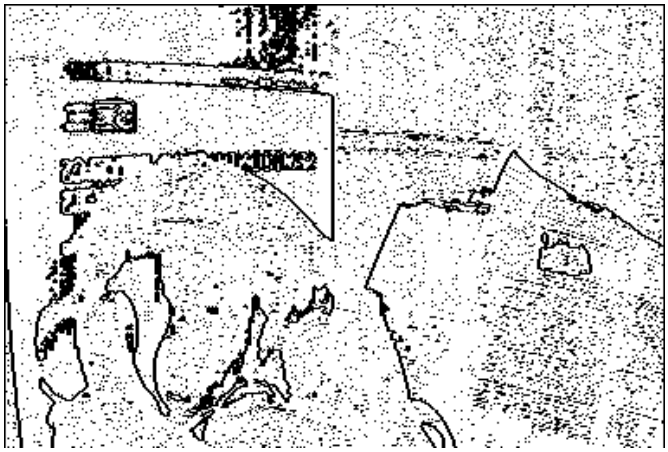
6.5.3 Power Consumption

As discussed in Section 6.2, the total saved power consumption using the two-step prediction ADC scheme depends on the specific image, especially the spatial gradient distribution. Fig. 6.13(a) shows a sample image taken by the prototype chip. Since the FPN of the pixels is removed by the DDS circuit, the vertical lines in the image are mainly caused by the different types of pixel structures and the FPN of the other readout circuits. Fig. 6.13(b) shows the failed prediction pixels, they are mainly located in the object edges (with a high spatial gradient), in this image, the failure prediction rate is 20.14 %. To avoid the wrong prediction caused by small pixel difference and noise, the maximum bit number of the prediction is set as 5. Fig. 6.13(c) shows the prediction distribution, a lighter color means more bit predictions are successful. Table 6.5.3 gives its statistic summary. The result shows that the switching steps for MSBs are significantly reduced, and for this image the switching energy is reduced by 29.05 %. To further minimize the

Table 6.3: Power consumption statistic of the sample image

Failure	Successful Prediction Ratio				
	D9	D8	D7	D6	D5
20.14%	79.86%	68.91%	52.01%	28.41%	10.59%

6.13.a:



6.13.b:

6.13.c:

Figure 6.13: (a) Sample image of the prototype chip, (b) Failed prediction pixels, (c) Prediction distribution.

system power consumption, in the prototype chip, the DDS circuit, S/H circuit and ADC are powered off when they are not in use.

6.6 Improved TDI CIS with Prediction ADC Scheme

Based on the previous designs, a new low-power anti-vibration TDI CMOS image sensor with adaptive TDI stages is proposed. The new sensor contains the features as follows,

(1) An online image deblurring function to compensate for the image shift on the focal plane and produce sharper TDI images;

(2) Adaptive TDI stages to prevent the photo signal saturation and increase the dynamic range;

(3) Prediction-based column-parallel ADCs to achieve the low power consumption for signal conversion and output.

6.6.1 Sensor Architecture

Fig. 6.14 shows the architecture diagram of the improved anti-vibration TDI CMOS image sensor, which consists of seven main functional blocks: a standard 256×8 4T-APS pixel array, 256 column-parallel single-stage memories, 256 column-parallel TDI accumulators, 256 column-parallel SAR ADCs, a stage shifter, a basic timing controller and an analog reference generator. Similarly to the design in Chapter 5, the column-parallel TDI accumulator are for conventional TDI operation and the column-parallel single-stage memories are for image shift compensation together with the TDI accumulators. The column-parallel SAR ADCs are equipped with the prediction scheme for power saving, and the final data is shifted out in parallel pixel by pixel. The TDI accumulator and the ADC are modified for dynamic range improvement, which is introduced in Section 6.6.3. The timing controller's task is to generate all the control signals from the external reset,

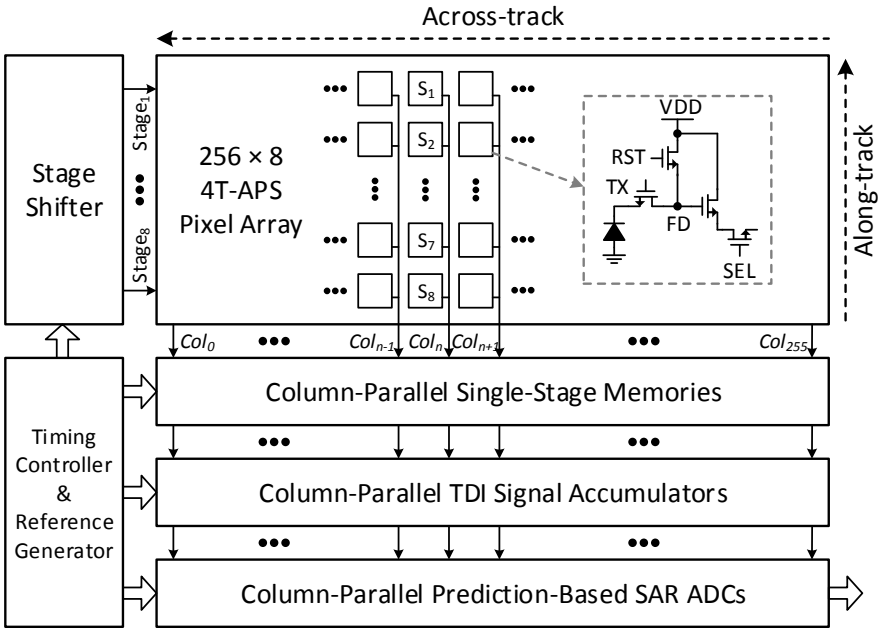


Figure 6.14: Architecture diagram of the improved anti-vibration TDI CMOS image sensor.

clock and exposure setting signals. An analog reference generator including a bandgap is applied here to provide on-chip biasing and reference voltages for low noise purpose.

6.6.2 TDI Signal Path

Fig 6.15 manifests the entirety of signal path from pixel to ADC. Each column contains 8 pixels (marked in green) for 8 times exposure to the same target with standard operation. One set of TDI circuits contains two modules: a TDI accumulator (marked in blue) and a single-stage memory (marked in red). With $\overline{S_M}$ disabled, the photo signal of each pixel would be read out and accumulated to an accumulation capacitor C_{An} ($n = 1,\ 2\ ...\ 8$) following each exposure, thus only the conventional TDI function is performed. With $\overline{S_M}$ enabled, the single-stage memory would calculate the signal difference of each two neighboring pixels, and add the difference back to the corresponding accumulator to

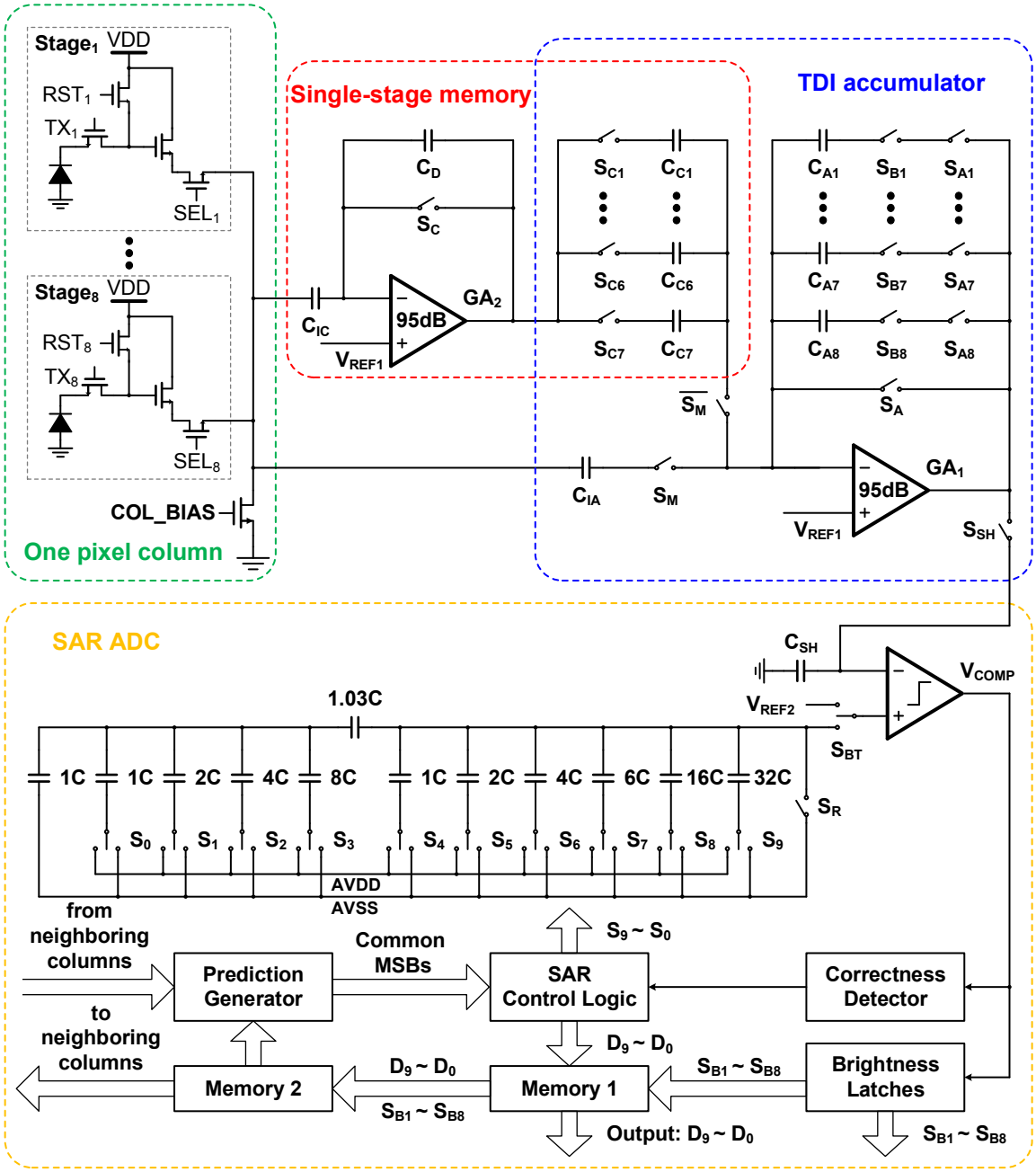


Figure 6.15: Signal path schematic of the improved anti-vibration TDI CMOS image sensor.

compensate for the signal mixture. After all the 8-stage TDI operation is completed, the signal will be sampled and quantized by the SAR ADC. In the first step, the SAR control logic would write the predicted MSBs to the switched-capacitor array to generate the two boundaries for prediction judgement; in the second step, the SAR control logic would convert the rest LSBs (with an accurate prediction) or start a new A/D conversion (with an inaccurate prediction). The digital results would be transferred to $Memory$ 1 for data output and $Memory$ 2 for the next prediction.

6.6.3 Adaptive TDI stages

TDI is a useful solution for low illumination scenes, however, the bright objects would lead to photo signal saturation and inevitable loss of details. In order to solve this problem, the adaptive gains of the gain amplifier for CDS and signal amplification is an effective solution for standard frame-based CMOS image sensors [40–42]. However, the signal strength judgement circuit and feedback control circuit are too complicated for the TDI accumulator, specifically, each accumulation capacitor would be outfitted with an optional capacitor and feedback control circuit. In a column stripe with narrow pitch, it is considered as a near impossible mission. Therefore, in this design, the adaptive TDI stages (1 stage for bright objects, 8 stages for others), i.e., the adaptive integration time, is proposed.

To implement the adaptive TDI stages, the TDI accumulator as well as the SAR ADC are modified. As shown in Fig. 6.15, a brightness switch S_{Bn} ($n = 1,\ 2\ ...\ 8$) is inserted between the accumulation capacitor C_{An} and its control switch S_{An}, and controlled by the brightness latches. Initially, S_{Bn} is turned on for a fresh TDI operation. After the first stage exposure, a comparison will be executed, in order to check if the photo signal reaches 10 % of the TDI signal swing. This specific action is to sample the first stage photo signal into C_{SH} after readout, and compare it to V_{REF2}, which equals to V_{REF1}

(the lower boundary of the TDI signal swing) plus 10 % of the TDI signal swing. If the signal is stronger than 10 % of the TDI signal swing, which indicates the object is bright enough, then the corresponding brightness latch would be written into a "0", and further turn off the brightness switch S_{Bn}. Thus the following TDI operations will not add photo signals to the accumulation capacitor any more. After the 8-stage TDI operation has been completed, the first stage signal would be quantized by the ADC, with the result being output together with the brightness latch value. Based on the first stage signal value and brightness latch value, the final signal value can be easily calculated. The brightness latch value will also be included into the prediction scheme, and will be granted a high priority. It is only with the same brightness latch values, that the common MSBs can be generated. Otherwise, the prediction judgement will not be carried out, and a conventional A/D conversion will be initiated.

With regards to the online image deblurring function, the first stage value is set as the reference for the following stages compensation. A strong photo signal of the first stage (with high brightness) is adequate for the TDI image, and the following TDI and compensation operations are not required any more. Consequently, the adaptive TDI stages is additionally suitable to the ODB algorithm. With this feature, the adaptive integration time is achieved, the details of the bright objects could be also imaged, and the DR is improved.

6.6.4 Sensor Implementation

A prototype chip of the improved TDI CMOS image sensor is implemented using TSMC 0.18 μm CIS technology (1P6M). As shown in the layout in Fig. 6.16, the chip occupies a total area of 2460×4440 μm^2. The signal path shown in Fig. 6.15 is implemented in column-parallel style for better matching. The single-stage memories (gain amplifier GA_1 with the associated capacitors in Fig. 6.15) and the TDI accumulators (gain amplifier

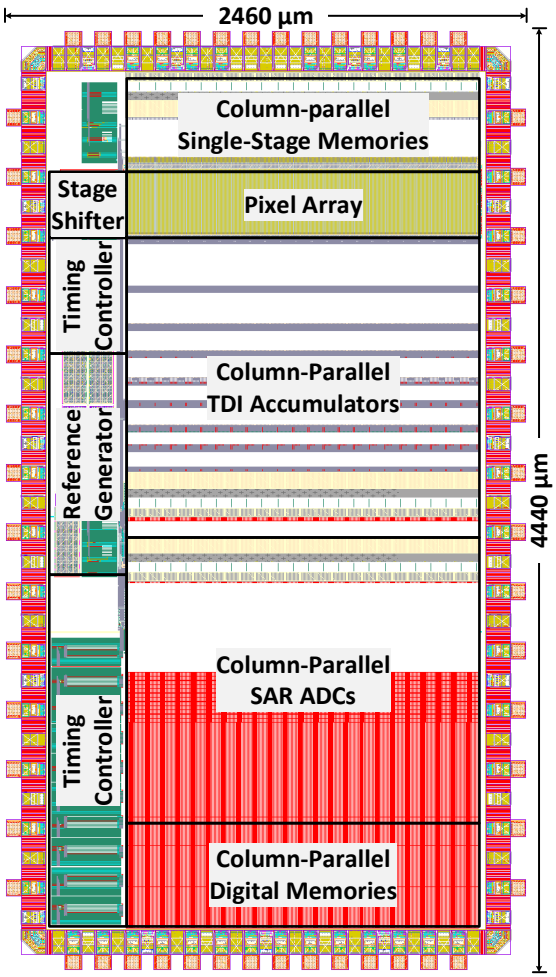


Figure 6.16: Layout of the improved anti-vibration TDI CMOS image sensor.

GA_2 with associated capacitors in Fig. 6.15) are placed on the top and bottom sides of the pixel array, respectively. The SAR ADCs are placed next to the TDI accumulators, with analog components on the top and digital components on the bottom, allowing for less crosstalk and coupling noise. The column slices are directly powered by the pads on the right side to eliminate the dynamic voltage drop (IR drop). Additionally the stage shifter, timing controller and reference generator are placed on the left side to broadcast the signals for the column slices.

6.7 Design Summary

This chapter first proposes a two-step prediction ADC scheme for low-power column-parallel ADCs in image sensors. By finding out the common MSBs of some pixels of previous row, the MSBs of the current pixel can be predicted, so the corresponding switching energy can be effectively saved. A prototype CMOS image sensor was designed and fabricated with column-parallel SAR ADCs applying the proposed scheme, and the measurement result shows that the switching power can be significantly reduced.

Based on the proposed ADC scheme, an improved anti-vibration TDI CMOS image sensor is then proposed, with the features as follows.

(1) The ODB algorithm can compensate for the image shift on the focal plane and produce sharp TDI images.

(2) The adaptive TDI stages can achieve short integration time for bright objects to refrain the photo signal from saturation and extend the dynamic range.

(3) The prediction-based column-parallel SAR ADCs can achieve the low power consumption for signal conversion and output.

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Chapter 7

Conclusions and Recommendations

7.1 Conclusions

This thesis expounds the research framework for the designing of the TDI CMOS image sensors utilized for space application. Through the investigation on the issues that occur in the remote image sensing system, the vibrations which may bring about the image motion on the focal plane and produce blurred images, are highlighted and subsequently become the principle focus. After the fundamental review of the image sensors, the readout technologies of CMOS image sensors, TDI CMOS implementations and the exiting solutions for the vibrations, a serial of TDI CMOS image sensors are proposed to effectively address the issues.

The initial design focuses on the anti-vibration TDI CMOS image sensor, employing a dynamic pipeline adjacent pixel signal transfer protocol to deal with the vibration-caused blurred images. This structure is capable of performing the conversion TDI operation, the configurable signal transfer directions and configurable integration stages. The configurable signal transfer directions can compensate for the image motion caused by the satellite vibrations, remove the image blur and maximise the image quality. As there

are limitations caused by the CMOS fabrication process, the signals can only be transferred in 45° or 90° angles, which restricts the compensation accuracy. The configurable integration stages can circumvent the photo signal saturation and achieve a higher DR. However, the number of achievable TDI stages is limited by the routing resource provided by the CMOS fabrication process.

The primary objective of the second design establishes a TDI CMOS image sensor with column-parallel single-ended signal accumulators based on the gain amplifier to extend the effective integration time, which will enhance the photo signal strength and proliferate the SNR. The measurement result of the fabricated sensor specifies that the 8-stage TDI operation can achieve a DR of 52.3 dB and 8.8 dB SNR improvement comparing to the single-stage line scanner with the high gain OP-AMP utilized in the accumulator.

The third design endeavours to present a solution for the vibration-caused image blur with the innovative online deblurring algorithm, which can be fully implemented using circuits. The ODB algorithm could separate the photo signal belonging to the "left" or "right" column and preclude mixing, and could be integrated into the TDI accumulator founded on the gain amplifier. In a signal path, a TDI accumulator can manage the conventional TDI operation, and a single-stage memory can compute the disparities amid each pair of neighboring pixels and augment it to the TDI accumulation signal, Consequently compensating for the image shift. The measurement result of the fabricated sensor details the ODB implementation to successfully compensate for the image motion on the focal plane, and produce sharp TDI images without detail loss, even under the complicated variation scenarios. However, through the employment of additional signal sampling and amplification, the online image deblurring operation may reduce the SNR and DR.

Preceding the fourth design, a two-step prediction scheme for low-power column-parallel ADCs in the image sensors is proposed. It is observed the occurrence that pixels

in a given image feature similar values to their neighbors based on the spatial likelihood of natural scenes. Therefore, by establishing the common MSBs of some pixels of the previous row, the MSBs of the current pixel can be predicted and the corresponding switching energy can be effectually saved. The prediction ADC scheme is then confirmed by a frame-based CMOS image sensor, and following this an improved TDI CMOS image sensor is conceived with features such as online deblurring function, adaptive TDI stages, low-power signal conversion and output.

This thesis seeks solutions for the vibrations with a complexity-reduced imaging system, and the final design can succeed to compensate for the vibrations, capture details of a given scene, and produce sharper TDI images with low power consumption, and without the assistance of any other additional devices or equipments. The proposed design is capable to be integrated into the remote imaging system of small satellites, e.g., nano-satellites and pico-satellites. The proposed method opens a door that will facilitate the design of remote imaging systems by alleviating most of the design constraints associated with pointing accuracy, active vibration controlling and cancellation. Therefore it can help to develop the small satellites with minimized system complexity, compressed size and reduced cost.

7.2 Recommendations for Further Research

This thesis succeeds in providing solutions for vibration issue in satellite imaging system with TDI CMOS image sensors. In view of the progress made at this juncture, the following points are recommended for future work to improve the pervious designs.

(1) The noise in the TDI signal path is a limitation that seriously restricts the TDI performance and the number of the achievable TDI stages. Thus amplifier with high gain and low noise is recommended to increase the SNR. Moreover, solutions with less operation and hardware proves to be a more effective way to reduce noise.

(2) In this thesis, the online deblurring operation can manage to recover the image blur, and produce sharp images with distortion. So further on-chip processing to recover the distortion is recommended as to achieve higher efficiency and accuracy then the post image processing.

(3) The silicon area and the column-parallel arrange style would also sidetrack the TDI image sensor implementations and performance. Thus the three-dimensional integrated circuit stack is highly recommended to fabricate the TDI CMOS image sensors. With the three-dimensional implementation, more silicon area can be obtained not only for the high performance fundamental circuit blocks that can achieved lower noise, but also for more functional parts of the signal processor that can operate more and more complicated on-chip signal/image processing operation.

Author's Publications

Patents

(1) Shoushun Chen, Kay Soon Low and **Hang Yu**, "Image Sensor and Method of Controlling the Same," filed with PCT international application number PCT/SG2014 /000319.

(2) Shoushun Chen, Kay Soon Low and **Hang Yu**, "A Method to Merge Ambient Light Sensor into a CMOS Image Sensor," filed with PCT international application number PCT/SG2014/000023.

Journal Papers

(1) **Hang Yu**, Wei Tang, Menghan Guo, and Shoushun Chen, "A Two-Step Prediction ADC Architecture for Integrated Low Power Image Sensors," *IEEE Sensors Journal, in process.*

(2) **Hang Yu**, Xinyuan Qian, Menghan Guo, and Shoushun Chen, "An Anti-Vibration Time Delay Integration CMOS Image Sensor with Online Deblurring Algorithm," *IEEE Transactions on Circuits and Systems for Video Technology*, vol. x, no. 99, pp. 1-1, Aug. 2015.

(3) Xinyuan Qian, **Hang Yu**, and Shoushun Chen, "A Global-Shutter Centroiding Measurement CMOS Image Sensor with Star Region SNR Improvement for Star Trackers," *IEEE Transactions on Circuits and Systems for Video Technology*, vol. x, no. 99, pp. 1-1, Aug. 2015.

(4) Xinyuan Qian, **Hang Yu**, Shoushun Chen, and Kay Soon Low, "A High Dynamic Range CMOS Image Sensor with Dual-Exposure Charge Subtraction Scheme," *IEEE Sensors Journal*, vol.15, no.2, pp. 661-662, Feb. 2015.

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(1) **Hang Yu**, Vigil Varghese, Xinyuan Qian, Menghan Guo, Shoushun Chen, and Kay Soon Low, "An 8-Stage Time Delay Integration CMOS Image Sensor with On-Chip Polarization Pixels," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 1098-1101, 24-27 May 2015.

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