Wide Dynamic Range CMOS Image Sensor for Star Tracking Applications

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A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirement for the degree of
Doctor of Philosophy

2015

Acknowledgments

I would like express my deepest gratitude to my thesis supervisor, Professor Chen Shoushun, for his insightful technical guidance, steady encouragement and unwavering support throughout my Ph.D. study at NTU. I would also like to extend my appreciation to my thesis co-supervisor, Professor Low Kay Soon, for providing invaluable suggestions and advice in the thesis.

I thank my colleagues in our research group, Dr. Zhao Bo, Dr. Yuan Chao, Mr. Zhang Xiangyu, Mr. Gibran Limi Jaya, for their continuous assistance. They have help made my Ph.D. journal enjoyable, interesting and fruitful. Special thanks to my colleague, Mr. Yu Hang for providing help and suggestions throughout the four years. It won't be easy to complete my research without all of you.

I also thank the School of Electrical and Electronic Engineering of Nanyang Technological University for awarding me the postgraduate scholarship as the financial support in my PhD candidature period.

Lastly, I owe a big debt of gratitude to my parents for their selfless love, inspiring support and continuous encouragement.

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List of Abbreviations

ADC	Analog-to-Digital Converter
ADCS	Attitude Determination and Control System
APS	Active Pixel Sensor
CCD	Charge Coupled Device
CDS	Correlated Double Sampling
CIS	CMOS Image Sensor
CMOS	Complementary Metal-Oxide-Semiconductor
CTIA	Capacitive Transimpedance Amplifier
DAC	Digital-to-Analog Converter
DFF	D-Flip-Flop
ELT	Enclosed Layout Transistor
FD	Floating Diffusion
FF	Fill Factor
FPN	Fixed Pattern Noise
FOV	Field of View
FOX	Field Oxide
HDR	High Dynamic Range
LEO	Low-Earth Orbit
OTA	Operational Transconductance Amplifier
PFM	Pulse Frequency Modulation
PWM	Pulse Width Modulation
PD	Photodiode
PPD	Pinned Photodiode
QE	Quantum Efficiency
SEE	Single Event Effect
SOC	System on Chip
SNR	Signal to Noise Ratio
STI	Shallow Trench Isolation
TID	Total Ionizing Dose

Abstract

Recent trends in space technologies highlight the importance of star trackers. Star trackers are optical-electronic devices that measure starlight directions. They are the most accurate sensors for 3-axis satellite attitude estimation. Current generation star trackers generally use CMOS image sensors as their star sensor thanks to this type of sensors inherent advantages of low power, low cost and, more importantly, their ability to integrate system-on-a-chip technology. This high degree of integration reduces process complexity and improves efficiency in attitude data processing. It also allows smaller, lighter star tracker designs, a distinct advantage in miniaturized space platforms. Conventional CMOS image sensors, however, do not meet design specifications for use in a star tracker, where several important limitations and design challenges have to be overcome. Most off-the-shelf CMOS image sensors are not space qualified to withstand the space radiation environment. Not only can radiation effects significantly exacerbate a sensors performance degradation, but they can also permanently damage the sensor itself. Radiation tolerance is therefore a critical prerequisite for such charge-sensitive devices destined for use in space applications. A wider dynamic range is also required if a wide range of star brightness is to be detected accurately, while active pixel sensors in deep submicron CMOS technologies fall short of meeting aggressive high dynamic range requirements due to their supply voltage limitations. Moreover, high-sensitivity pixels and low-noise readout circuits capable of achieving a high signal-to-noise ratio are essential for high centroiding accuracy. This thesis focuses primarily on the above-mentioned design aspects of CMOS image sensors. Its main contributions can be separated into three parts.

Firstly, radiation-induced impact on active pixel sensors were investigated. Different radiation hardening techniques were validated using silicon implementations to outline proper design guidelines for CMOS image sensors to be used in space applications. Secondly, two novel wide dynamic range CMOS image sensor architectures were proposed. One of them allows adaptive integration time for each pixel and expedites the readout using multiple readout channels. The other applies a dual-exposure charge subtraction strategy to extend dynamic range, and, accordingly, a new high-sensitivity capacitive transimpedance amplifier pixel was proposed. Finally, with very large scale integration (VLSI) architectures to improve centroiding accuracy in mind, a global-shutter CMOS image sensor with star-region SNR improvement was proposed.

Chapter 1

Introduction

1.1 Thesis Motivation

Attitude knowledge is important for modern space platforms. It must be measured and controlled for a variety of operations, such as pointing solar panels at the sun, aligning high-gain communications links with ground stations or attitude acquisition for scientific payloads. Missions like these, requiring high attitude precision, naturally imply a need for high-accuracy attitude sensors. Attitude sensors are widely used to detect an aircrafts orientation with respect to a reference frame in space. They are classified into different categories for example gyroscopes, sun sensors, magnetometers or star trackers - according to the reference vectors they use. One of these sensor types, the star tracker, measures starlight directions using solid-state imaging devices. Since starlight directions are fixed in the inertial reference frame (ECI frame), they are known to be extremely accurate. Star trackers are therefore considered the most accurate kind of sensor, capable of offering bore sight accuracies in terms of arcseconds. Modern space platforms are usually equipped with a star tracker to satisfy their need for high-accuracy attitude measurement.

CMOS image sensor technologies have evolved so rapidly over the last few decades that these devices have now outpaced Charge-Couple Devices (CCDs) and are widely

used in a wide range of space applications, including robotic and navigation vision systems, astronomical and earth imaging, land and rover cameras, x-ray detectors and star trackers. Recently emerging trends in miniaturized satellite missions, such as micro-satellites and pico-satellites, have favored the deployment of CMOS-based star trackers. A micro-satellite has a wet mass of several tens of kilograms. To reduce the amount of hardware or firmware, and thus to reduce mass and weight, the circuit integration capability of System-on-Chip (SoC) design is vital. Size scaling also limits the number of on-board solar cells, and the sensors used need to consume little power due to the strict power budget. The main advantages of CMOS image sensors are their low power consumption at low voltage operation, their high integration capability for SoC design, their potential for radiation resilience, and the cost effective solutions they provide from a standardized fabrication process. These positive features are particularly beneficial for star trackers in miniaturized satellite missions.

Most commercial off-the-shelf CMOS image sensors are lacking in any specific design consideration of relevance to star trackers. Conventional Active Pixel Sensors (APS) are not qualified for direct usage in space missions. Low-Earth-Orbit (LEO) satellites are exposed to a harsh radiation environment, with grammar rays and high energy particles. Radiation hardness is critical for electronics deployed in space applications, especially the charge-sensitive devices found in CMOS image sensors, which need to be able to survive the radiation environment during long-term space missions. Performance degradation caused by total ionizing dose (TID) can also be a significant source of measurement noise, which increases measurement error. APS do not have sufficient dynamic range to accommodate a wide span of star brightness with a high signal-to-noise ratio (SNR). Wide dynamic range increases the number of detectable stars in the Field of View (FOV). Since the average number of stars in the FOV is also essential for accuracy, wide dynamic range also plays an important role in increasing overall tracking accuracy. Another critical issue

in APS is sensitivity to starlight. It is very difficult for APS to detect a limited number of photons from stars, especially when exposure time is also limited. Since photoelectrons are directly integrated on the large photodiode capacitance, voltage change is small. The SNR obtained is therefore low, making APS unsuitable for high-accuracy star trackers.

The above-described issues set new design specifications for next generation high-accuracy CMOS-based star trackers. Radiation tolerant pixel devices, in particular for CMOS image sensor technologies, are essential in this application. Neither is it easy to achieve high dynamic range and high sensitivity at the same time. This imposes difficult design trade-offs and makes it necessary to seek the specific optimization of each design parameter. My research in this thesis has been motivated precisely by these considerations. To summarize, this thesis investigates various design aspects of a CMOS image sensor for star trackers, exploring VLSI solutions at different levels, from system innovation and circuit techniques to device optimization. It is expected that the findings of this thesis will help improve the measurement performance of the star trackers used in NTUs current attitude determination and control system (ADCS) and prove useful in NTUs future satellite missions.

1.2 Thesis Objectives

The overall objective of this thesis is to develop wide dynamic range CMOS image sensors for star tracking. Three major areas are covered:

(i) To investigate radiation effects on CMOS image sensors used in the space radiation environment and design radiation-tolerant pixels.

(ii) To design new pixel circuit and sensor architecture featuring improved dynamic range suitable for use in star trackers.

(iii) To explore smart sensor architecture capable of aiding star centroiding measurement and improving centroiding accuracy.

1.3 Thesis Contributions

The contributions of this thesis are summarized in the following items:

(i) Radiation-induced impacts on CMOS image sensors were investigated. In particular, total ionizing radiation effects on 4T APS were analyzed. Characterizations from fabricated chips mainly showed dark current increase and temporal noise increase due to the ionizing radiation on the pixel devices. The characterization also showed that the main radiation-induced degradation mechanism in a 4T APS was due to complex photosensitive regions. To mitigate these radiation influences, various radiation hardening techniques using layout enhancement were employed on four proposed pixels. The techniques were then compared to verify their usefulness and effectiveness. The comparison results provided a guideline for radiation-tolerant pixel design as an economic countermeasure to the total ionizing dose effects.

(ii) Two novel wide dynamic range CMOS image sensor architectures were proposed. The first approach was based on the time-domain operation principle of adaptive integration time. Rather than conventional time-domain pixels, which are large and complex, the proposed architecture only utilized pixels with a compact footprint. This was achieved by cyclically checking the integration voltage of a row of pixels in column-parallel circuits, throughout exposure. Brighter pixels could thus be "marked" and read out first. Dark pixels continued to integrate until their voltages fell into a voltage window. Pixel voltage and its sampling time were used together to reconstruct the image. The second approach extended the dynamic range by

means of a dual-exposure charge subtraction strategy. A capacitive transimpedance amplifier (CTIA) was used to achieve high sensitivity at the same time.

(iii) A novel smart CMOS image sensor capable of assisting in star centroiding was proposed. An adaptive SNR improvement algorithm was integrated on the focal plane to improve centroiding accuracy. A corresponding sensor architecture was also proposed. The proposed approach was evaluated using experimental measurement.

1.4 Thesis Organization

The rest of the thesis is organized as follows.

Chapter 2 presents a comprehensive review of existing literature. It starts with an introduction to star trackers. The architecture, operating principle and major design specifications of star trackers are discussed. Next, a brief review of CMOS image sensors is presented and earlier works looking into radiation effects on semiconductor devices and CMOS image sensors are described. The chapter covers the cause of radiation effects and various forms of performance degradation due to those effects. Finally, existing high dynamic range CMOS image sensor solutions are presented, categorized and explained, with some examples from literature.

Chapter 3 is dedicated to radiation-tolerant pixel design. The design details of four radiation-tolerant pixels are described. Different pixel performance parameters such as dark current, dark current non-uniformity and temporal noise are analyzed using radiation characterizations. A radiation-tolerant image sensor based on the characterization results is briefly presented.

Chapter 4 introduces the operating principle, architectural design, circuit details, simulation results and chip measurement of two wide dynamic range CMOS image sensor architectures. The first focuses on the concept of adaptive integration time and the second

is based on a CTIA pixel and a charge subtraction scheme which combines high sensitivity with high dynamic range.

Chapter 5 introduces a smart CMOS measurement sensor for star centroiding. The proposed sensor architecture integrates a focal-plane SNR improvement algorithm to improve centroiding accuracy. The sensor architecture, circuit design considerations, proof-of-concept implementation and measurement results are described.

Chapter 6 draws some conclusions and suggests future work.

Chapter 2

Background Study and Literature Review

This chapter conducts a background study and provides a detailed review of related works in literature. It starts with an introduction to star trackers, focusing on the design specification and accuracy qualification of a star tracker with regard to the sensor employed. It then outlines several design challenges that a CMOS image sensor has to address if it is to be used in star trackers. The analysis shows how, just like other space electronics, star tracker sensors must have radiation tolerance as a common qualification. They must also have high sensitivity and wide dynamic range to achieve high tracking accuracy. After a brief introduction to CMOS image sensors, a detailed description of radiation effects on CMOS devices is presented, followed by a review of general radiation hardening design techniques. With regard to high dynamic range CMOS image sensors, several representative high dynamic range CMOS image sensor solutions described in literature are categorized and discussed.

2.1 Attitude Determination of Satellites

Attitude determination is the process of estimating satellite orientation by observing others celestial objects or reference points remotely. Commonly used reference objects

are the Earth magnetic field, the Sun, the Earth and celestial sphere and stars. Satellite attitude is determined based on the calculation of its relative attitude to these well-known objects in space. It is also controlled to point to some orientation for the purpose of performing specific operation during space mission, for example, pointing solar panels at the sun, pointing a high-gain communications link towards a ground station or attitude acquisition for a scientific payload. Based on different aspects of requirements, such as pointing accuracy, space constraints and power consumptions, the on-board attitude determination and control system (ADCS) is equipped with suitable sensor configuration [10]. Commonly used attitude sensors are sun sensor, magnetometer, gyroscope, earth horizon sensor, star tracker, etc.

2.1.1 Sun Sensor

The sun sensor is the most widely used sensor type on satellite due to simple structure, low cost, and low power consumption [11] [12]. It is a device to measure the sun illumination using a photodiode to estimate incident angle of the sun rays relative to the sensor [13]. Sun being the brightest light source in space around the earth, the sun sensor is a reliable sensor without discriminating among sources [14]. There are numerous types of sun sensor in the market with field of view ranging from 10 degrees to 128 degrees and accuracy from 0.5 degrees to 5 degrees [15] [16] [17].

2.1.2 Magnetometer

Magnetometer is an instrument to measure the strength or direction of magnetic fields. The earth magnetic field is modeled to have moderate accuracy using state-of-the-art earth magnetic field models. There are many types of magnetic sensor: search coil, fluxgate, optically pumped, nuclear precession, SQUID, Hall-effect, anisotropic magneto resistance and micro-electro-mechanical systems (MEMS)-based magnetic sensors [18]. They vary in mass, sensor complexity and power consumption [19].

2.1.3 Gyroscope

Gyroscope is an instrument used to measure the rotational rate [20]. There are various types of gyroscopes, such as mechanical, optical, MEMS and etc. They differ in operation principles. The gyroscope axes are aligned with the satellite body frame [21]. The gyroscope is often used with other sensors. For instance, an inertial measurement unit (IMU) is an integrated electronic device with a 3-axis magnetometer, a 3-axis gyroscope and a 3-axis accelerometer. It can achieve a reasonable accuracy.

2.1.4 Earth Horizon Sensor

Earth horizon sensor is an infrared device that detects the contrast of the cold space and the earth surface and determines orientation relative to the infrared radiation from earth surface. They can also provide moderate accuracy at a low cost [22]. The disadvantage is that this type of sensor is restricted to the circular orbit.

2.1.5 Star Tracker

Star tracker is an optical-electronics device that determines the satellite attitude by measuring starlight directions. Starlight directions are fixed in the inertial reference frame (ECI frame) [23], and starlight directions are known to be extremely accurate. Therefore, the accuracy of star trackers can be in range of arc seconds. It is the most accurate solution among all the state-of-the-art attitude sensors.

Star tracker in old generations are expensive, bulky and power thirsty until the era of solid-state imaging [24]. Current generation star trackers widely use CMOS image sensors as their sensing components. The development in star trackers benefits from the advantages of CMOS technology, such as low power, low cost and capability of system-on-a-chip (SoC) integration. It allows star trackers to become smaller and lighter, making it the best candidate for miniaturized space platform. The SoC integrability also enables the

great advancement in the efficiency of the data processing. Traditionally, data must be transmitted to ground and the attitude determination is performed in the ground station after downloading star image data through telemetry. Modern star trackers integrate a signal processing microprocessor in it so it can perform attitude determination algorithms such as image processing, star identification and attitude calculation directly on board. A fast update rate up to 100 Hz can be achieved.

2.2 Review of Star Trackers

2.2.1 Overview

Fig. 2.1 shows the block diagram for a typical star tracker. The device mainly consists of a set of telescope optics and an image sensor together with signal processing electronics [25].

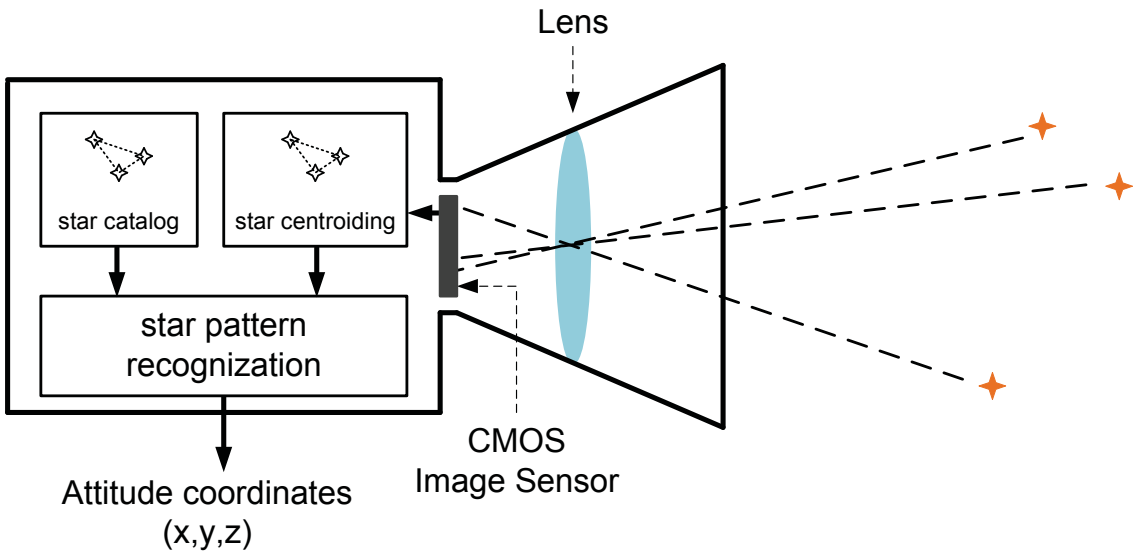


Figure 2.1: System block diagram of a typical star tracker.

The optical system and the CMOS image sensor map the star field onto the focal plane, as shown in Fig. 2.2. The centroids of the detected stars are extracted and computed to build up a star pattern after necessary star image processing. On the focal

plane, the positions of the star centroids are transformed into a Cartesian coordinate system using a pinhole model. Star catalog is a database which lists the stars used for star pattern recognition. Usually, it requires to be processed before it is loaded into the star tracker's on-board memory [26]. A subset of the star catalog is often selected in consideration of database size and searching speed. The star pattern recognition takes the calculated star centroids as input and extracts important star features following the recognition algorithm. It then searches to match the star pattern with the reference patterns in star catalog, identify the pattern and produce the attitude coordinates. There are different autonomous star pattern recognition algorithm and they vary in complexity, recognition speed, database size, recognition accuracy, and recognition robustness.

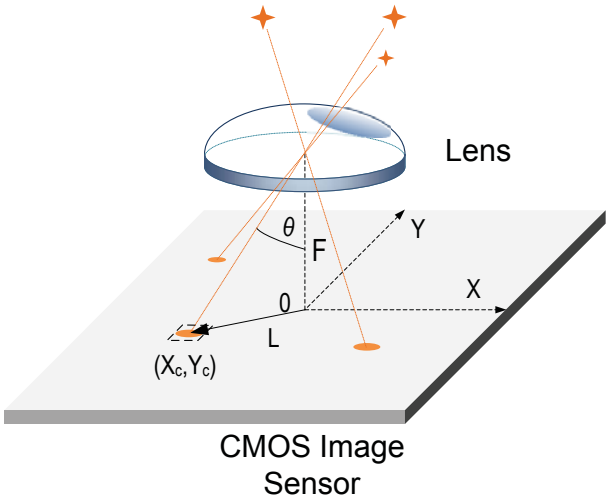


Figure 2.2: Focal plane for star centroid calculation.

In a star tracker, there are two operating scenarios: initial attitude estimation mode (or "lost in space" mode) and attitude tracking mode. In the initial attitude estimation mode, the star tracker has no pre-knowledge of the attitude information. It requires to perform star pattern recognition as discussed. The identification typically takes a few seconds to complete. This mode is used in the launch and early orbit phase (LEOP) of the satellite or employed when the satellite losses its attitude. The attitude tracking

mode is used when the star tracker has already known its three axis attitude with some uncertainties. The task in this mode is much easier since only previously identified stars at known positions needs tracking.

2.2.2 Star Detection and Star Centroiding

Stars are point sources and the most accurate optical references for satellite attitude determination. The stars positions are fixed in the Earth center inertial frame and they are very small size objects as seen from the solar system. The star catalog contains the star positions in arc-seconds accuracy. Hence, the star tracker can perform the attitude determination with accuracies in the arc-seconds range. Due to the imperfection of star tracker hardware such as optical lens, image sensor and electronic circuitry, the practical accuracy is estimated around 90 arc-seconds.

For an aberration-free lens system, the point spread function (PSF) on the focal plane obtained by far-field diffraction analysis is usually a Bessel function. However, the energy distribution of star image will not be a Bessel function as the effects of the aberration and defocusing. Generally, the defocused starlight is assumed to have a two-dimensional Gaussian distribution [27], a common assumption in optical applications with point sources:

$$I(x,y) = \frac{I_0}{\sqrt{2\pi\sigma_{PSF}^2}} \exp\left\{-\frac{(x-x_c)^2 + (y-y_c)^2}{2\sigma_{PSF}^2}\right\} \qquad \text{(Eq. 2.1)}$$

where $(x_c\ ,\ y_c)$ represents the position of the "true" star center, I_0 is the starlight intensity and σ_{PSF} is the spread of the Gaussian. Due to the discrete pixelization on the focal plane, the two-dimensional bell-shaped responses will typically spread over several neighboring pixels with peak in the center and form a star spot. By calculating the centroid of the star spot using hyperacuity technique or centroiding algorithm, the

accuracy of the star position can achieve sub-pixel accuracy, and thus the attitude can achieve arc-seconds accuracy.

The most common centroiding algorithm to determining the star locations is the center of mass (COM) algorithm [28]. There are a few other variants of the algorithm but bear the same principle. In this algorithm, every pixel in the image and compares it to a threshold value. If a pixel is above the threshold, a square region of interest (ROI) is identified with the detected pixel at the center. The pixel values on the ROI border are averaged and subtracted from each pixel within the ROI. This process subtracts out the background noise. A COM calculation is then used to find the centroid location within the ROI.

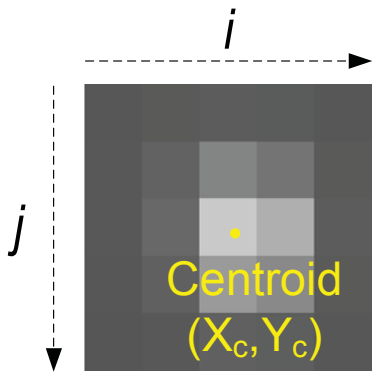


Figure 2.3: An example ROI with 5×5 pixels. The highlighted centroid is calculated using the centre of mass algorithm. It can achieve sub pixel accuracy

Fig. 2.3 shows an example pixel responses in a 5×5 region-of-interest (ROI). The star centroid can be calculated as follows:

$$\begin{cases} x_c = \sum_{i,j} x_{ij} S_{ij} \Big/ \sum_{i,j} S_{ij} \\ y_c = \sum_{i,j} y_{ij} S_{ij} \Big/ \sum_{i,j} S_{ij} \end{cases} \qquad \text{(Eq. 2.2)}$$

where (x_c, y_c) represents the calculated centroid coordinate and S_{ij} is the signal magnitude at pixel(i,j) in the ROI. The error introduced by the centroiding algorithm has a

systematic contribution and a random one [29]. Systematic error is due to the nature of the algorithm, for example the assumptions of point spread function or the effects of pixelization and spot size. On the other side, random contribution comes from the measurement uncertainty. The deviation of S_{ij} due to sensor noise from its ideal value will propagate through a deviation in the calculated centroid [30]. In [31], the effects of various noise sources of CMOS image sensors on the centroiding accuracy were analyzed in detail. It is suggested the centroiding accuracy can be improved with the increase of SNR.

2.2.3 Apparent Magnitude

One of the fundamental observable quantity of a stellar object is its brightness. Because stars can have a very wide range of brightness, it is a common practice to introduce a scaled system to classify the brightness. Historically, the magnitude scale is the logarithmic measure of the brightness of an object, in astronomy, measured in a specific wavelength or passband, usually in optical or near-infrared wavelengths. The apparent brightness of a star observed from the Earth is hence called the apparent magnitude. Fig. 2.4 shows the apparent magnitude of some exemplary celestial objects along the magnitude scale. The most negative value on the ruler represents the brightest celestial objects and the faintest on the other side. Most stars stay in bounds of magnitude 1 to 6. Some very bright celestial objects can have magnitudes of negative numbers and very faint objects that cannot be detected by human eyes have magnitudes greater than +6. Some example apparent magnitudes are: Sun = -26.7, Moon = -12.6, Venus = -4.4, Sirius = -1.4, Vega = 0.0, faintest naked eye star = +6.5, brightest quasar = +12.8 and faintest object = +30 to +31.

On this quantified magnitude scale, a magnitude interval of 1 corresponds to a factor of $100^{1/5}$ or approximately 2.512 times the amount in actual light intensity. And an

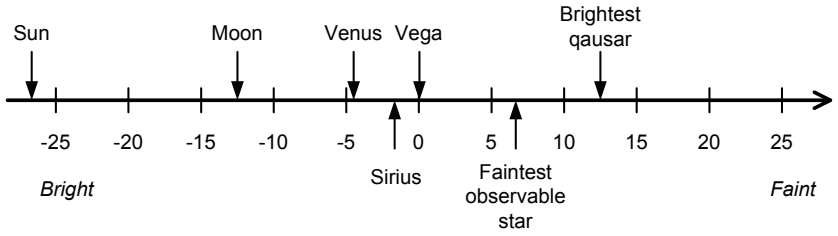


Figure 2.4: Apparent magnitude of some celestial objects in the magnitude systems.

increase of 1 in the magnitude scale corresponds to a decrease in brightness by such factor. Therefore, the calculation between any two magnitudes can be performed by raising or the 2.512 to the power of the number equal to the difference in magnitudes. In general, the intensity-magnitude relation between two stars is mathematically given in Eq. 2.3 and in Eq. 2.4 reversely.

$$m_2 - m_1 = -2.5(\log_{10} I_2 - \log_{10} I_1) = -2.5 \log_{10} \left(\frac{I_2}{I_1} \right) \qquad \text{(Eq. 2.3)}$$

and

$$\frac{I_2}{I_1} = 100^{\frac{m_1 - m_2}{5}} = 2.512^{(m_1 - m_2)} \qquad \text{(Eq. 2.4)}$$

where m_1 and m_2 are apparent magnitudes to both stars belong, respectively, and I_1 and I_2 are the corresponding intensity. This relation indicates, for instance, first magnitude stars are about $2.512^{2-1} = 2.512$ times brighter than second magnitude stars, and $2.512^{3-1} = 2.512^2$ times brighter than third magnitude stars, etc. The knowledge is further used to calculate the star light sensitivity if the intensity of one celestial object is already known, the intensity of other one can therefore be determined by this magnitude mapping. In next section, the star light sensitivity are calculated following this manner with apparent magnitude taking the Sun as a reference magnitude point.

2.2.4 Star Light Sensitivity

Knowing the apparent magnitudes of two celestial bodies, one can identify the illumination intensity of the star given the illumination intensity of a reference celestial body. Since many bright stars in the star field have surface temperatures close to that of the Sun and therefore belongs to the same spectral class G2. The calculation can be easily done from the above relation. The following calculation is adapted from [1]. As a reference, the apparent magnitude (Mv) of the Sun is -26.7 and the solar flux is 1.3 KW/m^2. Therefore the Sun is $2.512^{26.7}$ times brighter than a $M_v = 0$ star. The incident power on an imaging area of 1mm^2 from $M_v = 0$ star regarded as a black body radiator shares the same relative spectral characteristic and the total power is then (1.3 KW/m^2 $\times$ 10^{-6}m^2) / $2.512^{26.7} = 2.96 \cdot 10^{-14}$ W.

This calculated power received from a black body is spread over the total spectral range and is a function of the wavelength and temperature, which is given by

$$I(\lambda, T) = \frac{2 \cdot \pi \cdot h \cdot c^2}{\lambda^5 \cdot (e^{h \cdot c / \lambda \cdot k_B \cdot T} - 1)} \qquad \text{(Eq. 2.5)}$$

where λ is the wavelength and T is the temperature (in Kelvin). Other constants are $h = 6.626 \cdot 10^{-34}$ J $\cdot$ s; c is the speed of light equal to $2.997 \cdot 10^8$ m/s, and k_B is Boltzmann constant equal to $1.38 \cdot 10^{-23}$ J/K. The resulting total power influx from a $M_v = 0$ star with 5800K temperature on an area of 1mm^2 is shown in Fig. 2.5 (a).

Of the total amount power received, the portion of the wavelengths that can reach the focal plane is limited by the optics. As the the optical system transmits visible wavelengths in the range between 400 nm to 800 nm band. This, in fact, is like a pass-band filter and the resulting power influx on the focal plane is shown in Fig. 2.5 (b). Moreover, it is possible to express the power influx in term of photon influx due to the energy of a photon $E = hc/\lambda$. The resulting spectral spread is shown in Fig. 2.5 (c).

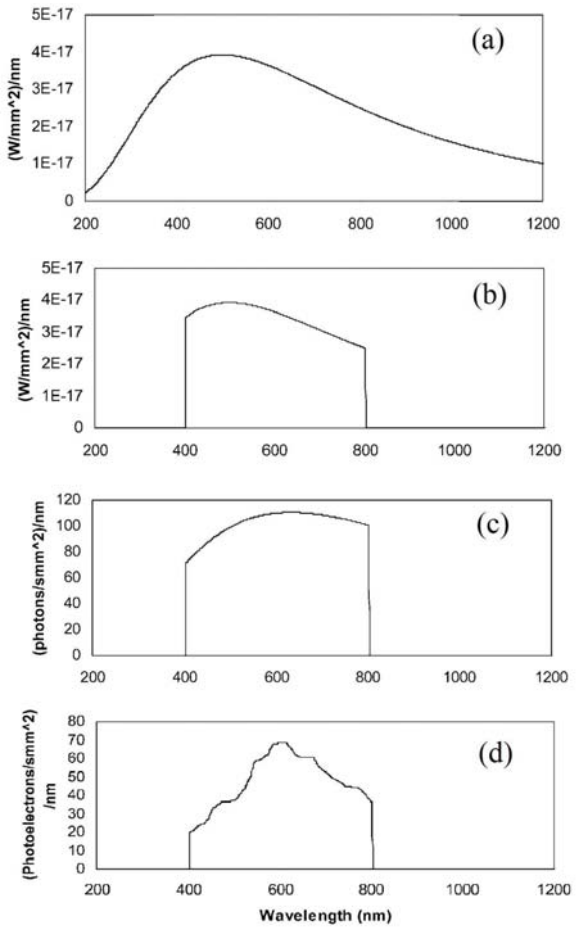


Figure 2.5: (a) Power spectrum from a $M_v = 0$ star on an area of 1mm^2. (b) Power influx onto the focal plane. (c) Photon influx onto the focal plane. (d) Detectable photons on the focal plane. Adapted from [1].

On the focal plane, these photons are converted into photo-generated charges (photoelectrons). Only a fraction of these photons are effectively converted and contribute to the signal due to the quantum efficiency limitation. The limitation is wavelength dependent. The resulting photons received in a typical sensor is as shown in Fig. 2.5 (d). The total amount of photoelectrons that are summed over the wavelength is 19100. This means that under one second exposure and a lens aperture area on 1mm^2 will generate 19100 photoelectrons for a $M_v = 0$ star. Using this number, it is easy to calculate other

stars with other magnitudes. Take $M_V = 4$ star as example, the resulting photoelectrons generated in 1mm^2 under 200ms exposure time will eventually be equal to

$$19100\frac{photoelectrons}{s \cdot mm^2} \cdot \frac{1}{2.512^{4-0}} \cdot 0.2s \cdot \pi \cdot 15^2 mm^2 = 68000\frac{photoelectrons}{mm^2} \quad \text{(Eq. 2.6)}$$

This example of calculation gives a quantitative estimate of the star signals in a star image. Generally, a star can only generate limited number of photoelectrons, which makes star detection a challenging issue. At one hand, a detection threshold is necessary which sets a boundary to differentiate the real stars from the dark background. The background quality of the captured images are typically limited by several sensor noise contributions. To avoid false detection, the signal charges should be sufficiently large to achieve a large signal-to-noise ratio (SNR). When selecting the detection threshold, one should take into consideration of acceptable SNR.

On the other hand, when above the detection threshold, a broad range of apparent magnitudes are required to be detected without losing the capability to differentiate their apparent magnitude. This requires the image sensor to support a high dynamic range capability to capture all illumination details within star pixels. Any loss of illumination information by saturation is not expected. The illumination details within the star pixels are critical to the further star centroiding processing.

2.2.5 Star Catalog and Star Pattern Recognition

Star catalog is a star database that lists stars with identifications. It is used for initial attitude acquisition or for calculating the attitude quaternion. There are a number of available open-source star catalogs, such as SAO J2000. Modern autonomous star trackers have an on-board star catalog stored in the firmware. The star catalog needs a delicate compilation process before installed to the firmware [32]. Typically, it is subsetted

Table 2.1: Star Radiation and Luminance

Light source	Apparent magnitude	Radiation(W/m^2)	Luminance(lux)
Sun	-26.7	1360	130000
Earth		193	3.15193e+4
Sirius	-1.4	5.19e-8	1e-5
Star Magnitude 0	0	1.44e-8	2.7e-6
Star Magnitude 1	1	5.7716e-9	1.0533e-6
Star Magnitude 2	2	2.3105e-9	4.2131e-7
Star Magnitude 3	3	9.2418e-10	1.6852e-7
Star Magnitude 4	4	3.6967e-10	6.74e-8
Star Magnitude 5	5	1.4787e-10	2.6964e-8
Star Magnitude 6	6	5.9148e-11	1.0785e-8

from the complete catalog according to the spectral sensitivity of the star tracker. It is further used to generate star pattern database, which stores the features-in-interest describing each reference star in this catalog.

Star pattern recognition is to extract these important features of captured star and match them with the database according to some rules. There are different recognition algorithms developed, which vary in complexity, recognition speed, database size, recognition accuracy and robustness [33]. One well-established method is Liebe algorithm [28] [34]. The method utilizes triple star pattern, characterized by three features, namely 1) the angular distance to the first neighbour star; 2) the angular distance to the second neighbour star; and 3) the spherical angle between the two neighbour stars. This triple star pattern is compared with the pattern catalog to determine the correct star identity. Other algorithms include grid star pattern recognition algorithm [35] [36], pyramid star pattern recognition algorithm [37], the planar triangle algorithm, geometric voting algorithm [38] and so on.

2.3 Fundamentals of CMOS Image Sensors

There are two major competing technologies for solid-sate imaging in the market: charge coupled devices (CCD) and CMOS image sensors (CIS). The introduction of first CMOS image sensors by Westinghouse, IBM, Plessy and Fairchild dates back to late 1960s [39]. CCDs were invented by Bell Laboratory as an analog memory device in 1970 and quickly became the dominant technology in the field of solid-state imaging. Early CMOS image sensors are severely limited by CMOS technologies available at that moment. They suffer from poor imaging performance and large pixel size, which constrain their applicability to low-end imaging applications. Since 1990s, CMOS image sensors have been the subject of extensive development after the emergence of Active Pixel Sensor (APS) and the advent of deep submicron CMOS technologies. Thanks to the rapid advancement of CMOS imaging technologies in last decades, the imaging performance was drastically improved, making CMOS image sensors a viable alternative to CCDs in a wide range of applications. In addition, many advantages of CMOS image sensors such as low power, low cost due to standardized fabrication process and the inherent capability to integrate signal processing on-chip with image capturing has found its usefulness in many emerging applications [40], including space applications.

2.3.1 Imager Architecture

Generally, a CMOS image sensor is composed of an imaging area and peripheral readout circuitry, as shown in Fig. 2.6. The imaging area consisting of a two-dimensional array of pixels is the core of the imager and the pixel is the key device that is responsible for the imaging performance. Row and column access circuits are used to select a pixel in the array and read the pixel value. These can be either scanners for sequential read-out or decoders that enable random access to the pixel in the array. There is another category of event-driven readout method, called Address Event Representation (AER).

AER is originally a communication protocol of communicating sparse neural events between neuromorphic chips. Therefore, AER is commonly used in bio-inspired imaging systems [41] [42] [43]. Instead of reading out the pixel values passively driven by the sensor controller, the readout process is initiated by the pixel itself by sending a request once an event is "fired". An acknowledgement is sent back by the global AER controller. The handshaking between the pixel and the outside is established and the data transmission is initiated. When there are multiple requests at the same time, row and column arbitrated circuits are then required to ensure multiplexing the 2D array into a single output bus. The readout circuitry is composed of an one-dimensional array of signal processing circuits. They can vary in different forms, such as sample and hold circuit, noise cancelling circuits and column-parallel ADCs and so forth.

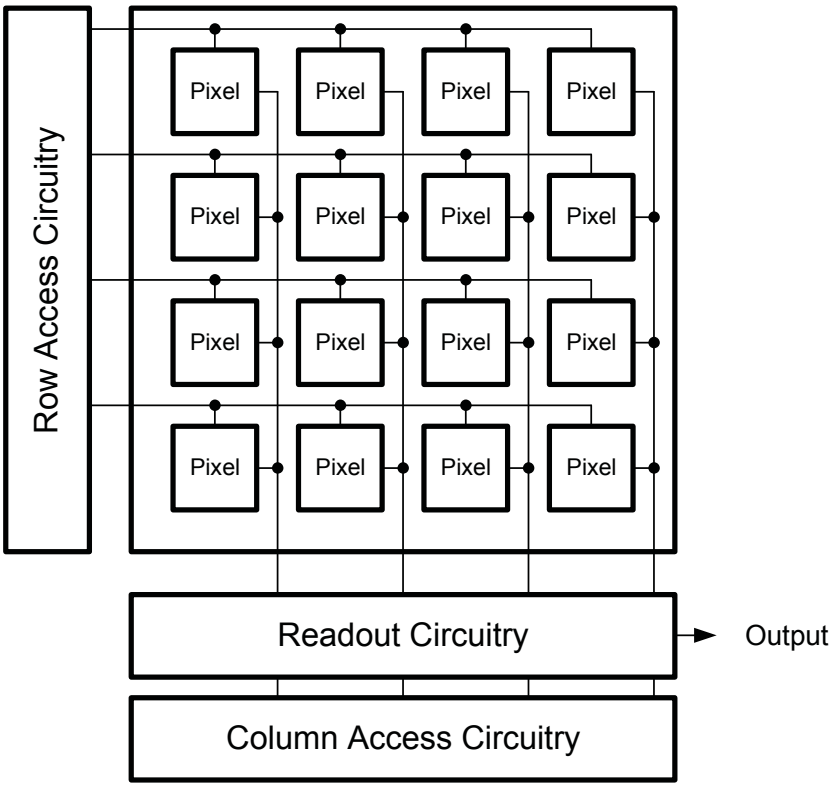


Figure 2.6: General architecture of a CMOS image sensor.

2.3.2 Photodetection and Photodetectors

Most photodetectors in solid-state imaging are essentially reversed-biased PN junctions. The most popular type of photodetector used in CMOS image sensors is photodiode (PD). It is easy to fabricate in bulk CMOS process. There are a variety of photodetectors based on the structure variations and operation principles. Other photodetectors include photogates, phototransistors, avalanche photodiodes (APDs) and single photon avalanche diodes (SPADs). In the following discussion, photodiode is used to explain the photodetection.

Fig. 2.7 shows the cross-section view of a N+ diffusion/P-substrate junction photodiode. Other commonly-used photodiodes are N-well/P-substrate and P+ diffusion/N-well photodiodes [44], etc.

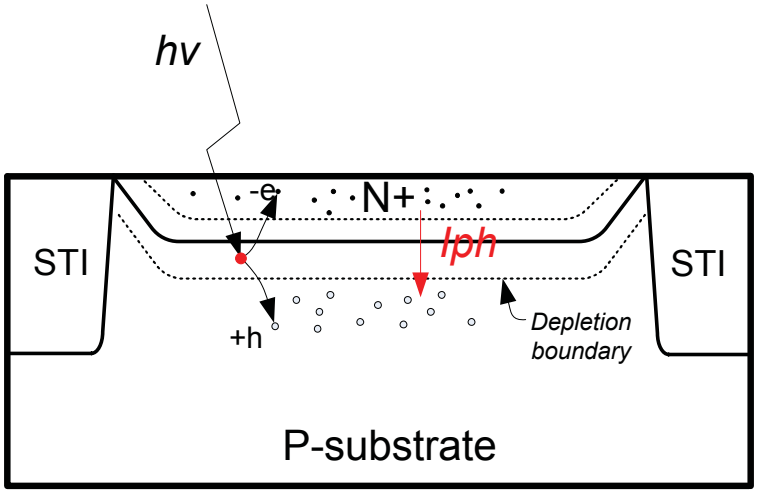


Figure 2.7: Cross-section view of a N+ diffusion/P-substrate photodiode.

When light passes through the dielectric layers and is incident on silicon, a portion of the incident light is reflected but the rest will penetrate into the silicon and is absorbed in the material. The penetration depth depends on the light wavelength. Typically, blue light penetrates about 0.2 μm while red light penetrates as deep as 10 μm. The differ-

ence in penetration depths can be an important figure for determining the photodiode structure for the design of color sensors.

When light is absorbed in silicon, photons carrying energy ($E = h\nu = hc/\lambda$) above bandgap ($E_g = 1.124$) of the silicon material can excite an electron to conduction band, leaving a hole in the valance band. The process is called electron-hole pair (EHP) generation. When EHP generation occurs in the depletion region of the photodiode, the electrical field will sweep electrons to N+ diffusion and holes to P substrate, respectively. The photogenerated carriers are effectively separated by the electric field. The movement of a large amount of photogenerated carriers forms the flow of drift current. If EHP is generated outside the depletion region where the electric field is weak, the carriers are likely to recombine. But there is still chance that they can diffuse to the depletion region and get separated. This small diffusion current also contributes part of the photocurrent (I_{PH}). The photogenerated electrons will be collected in the N+ diffusion. Considering all the above conditions, the carrier collection is a complex mechanism related to a number of factors including the location and width of the depletion region, minority carrier diffusion length. These, in turn, are primarily determined by the doping profile of the photodiode and strongly influenced by the process parameters.

It can be estimated that for typical ambient illumination level of approximately several hundred lux, the photocurrent is as small as on the order of a few picoamperes. It is difficult to measure and read photocurrent directly. Therefore, a practical image sensor must accumulate the charges over some time so that a reasonable signal can be measured. The time required to accumulate the charges is often referred to integration time or exposure time. The sensor is often referred to voltage mode or integration mode sensor. In such mode, N+ diffusion of the photodiode is electrically floated when the photocurrent discharges the parasitic capacitance of the photodiode. One can measure the voltage drop so at to determine the photocurrent from simple electric relationship. One thing to note

is that the discharge of the photodiode is not perfectly linear. The nonideality is caused by the change of the deletion width and thus photodiode capacitance due to the drop of the reversed-bias voltage.

2.3.3 Basic Pixel Architecture

The photodetector, together with accessing and readout circuits, comprises a pixel. There are different types of pixel architectures in CMOS image sensors.

2.3.4 Passive Pixel Sensor

The first commercially available CMOS pixel sensor in history is Passive Pixel Sensor (PPS). PPS has a simple structure. It is composed of a photodiode and a switch transistor, as shown in Fig. 2.8. It is similar to dynamic random access memory (DRAM).

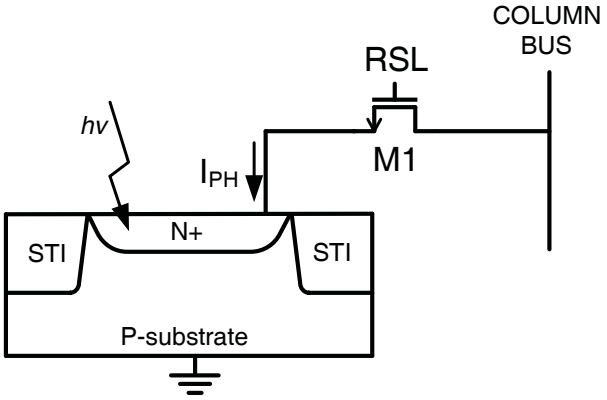


Figure 2.8: Schematic and cross-section view of a PPS.

Its simple structure of PPS has the advantage that the pixel area consumed by the circuits is minimized. This allows it to achieve high fill factor, which is preferable in CMOS image sensors. But the simplicity is also the source of several disadvantages. Switching noise and SNR is the crucial issue. Specifically, the noise power in charges is kTC, where C is the parasitic capacitance on the column bus. One should note that the

parasitic capacitance on the column bus scales up when the array size grows. This results in a large sampling capacitance for a PPS and hence results in large noise. In addition, as the parasitic capacitance on the column bus is large, the small amount of charges in PPS cannot change the voltage much. The output signal degrades easily, making SNR a significant issue during readout.

2.3.4.1 3T Active Pixel Sensor

Active Pixel Sensors (APS) is named after its active device amplifiers the signal in each pixel to distinguish from the name of PPS. There are a number of advantages compared with PPS, which makes it the most popular pixel architectures. Fig. 2.9 shows the schematic of an APS. The pixel configuration is referred as 3T APS. Another advanced 4T-APS has four transistors is discussed in the next section.

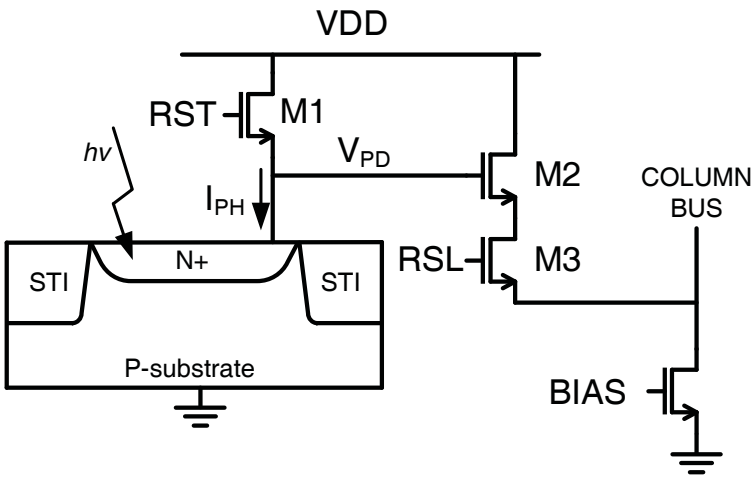


Figure 2.9: Schematic and cross-section view of a 3T APS

The pixel has a photodiode and three NMOS transistors. $M1$ is used to reset the photodiode to a reset voltage level, which is typically, $VDD - V_{TH}$, where V_{TH} is the threshold voltage of $M1$. After $M1$ turns off, the cathode of the photodiode, which is the sensing node is then electrically floating. The photocurrent, normally ranging

from femtoampere to picoamperes, starts to discharge the photodiode. The accumulated charges change the potential on the sensing node and the voltage of the photodiode V_{PD} decreases according to the input light intensity throughout the integration period. $M2$ acts as a source follower when row select signal RSL is asserted to turn on $M3$. The current source of the source follower resides in the column and is shared by all pixels in a column. The signal is buffered to the column bus. When the pixel readout is complete, RSL is turned off and RST is turned on to repeat the above procedures. Noteworthy is that 3T APS readout is nondestructive so multiple sampling on the sensing node is allowed.

While the accumulated charges are transferred directly to the column bus in a PPS, an APS converts the accumulated charges to a voltage signal. By incorporating amplification inside the pixel, the APS effectively reduces readout noise at a cost of lowering the fill factor. Also, fixed pattern noise (FPN) is introduced due to the amplifiers but can be significantly reduced in column signal processing [45].

Despite the SNR advantage of APS over PPS, there are several issues with the APS. It is difficult to suppress the reset noise, i.e. kTC noise due to the reset transistor. Besides, the photodetection and the photoconversion (from accumulated charges to voltage) on the same node constraints the photodiode design. The full well capacity increases as the photodiode parasitic capacitance increases. On the other hand, the conversion gain is inversely proportional to this capacitance. These two parameter, in turn, affects other important APS performance figures, that is, dynamic range and sensitivity. This implies the trade-off relationship existing in a 3T APS. The 4T APS resolves the trade-off as well as cancel easily suppress the kTC noise.

2.3.4.2 4T Active Pixel Sensor

The 4T APS has been introduced and developed based on 3T APS and to alleviate the aforementioned problems with the 3T APS.

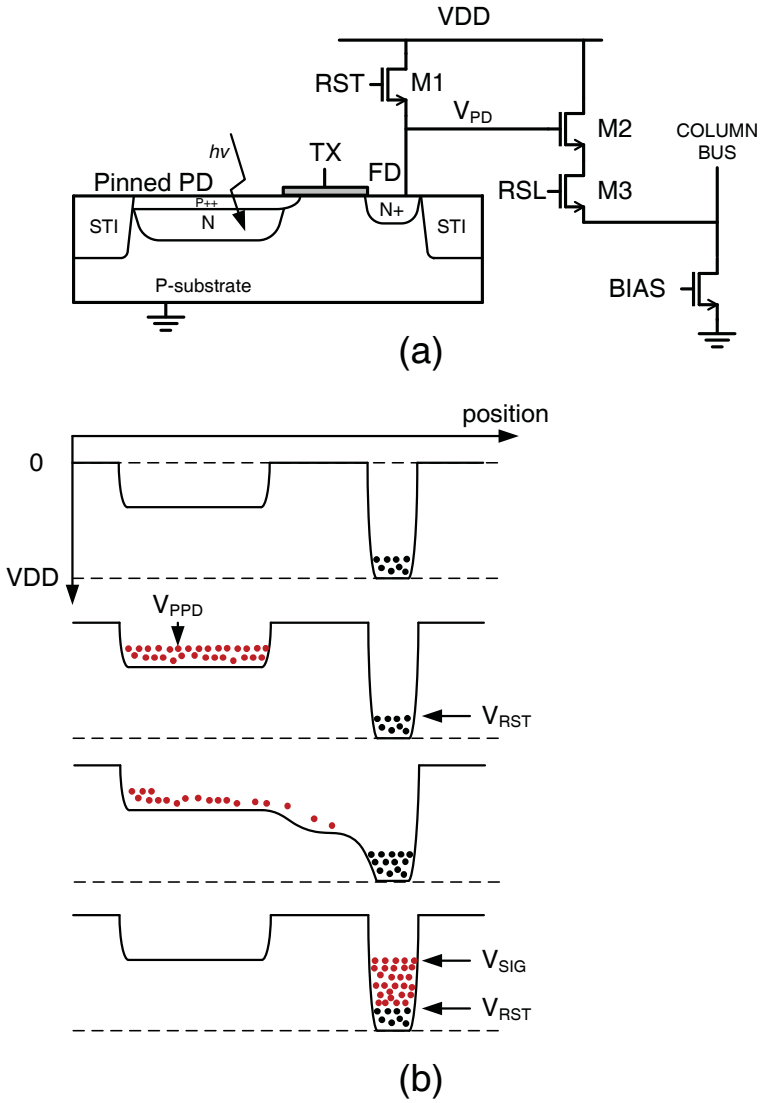


Figure 2.10: Schematic and cross-section view of a 4T APS.

The schematic of a 4T APS is shown in Fig.2.10 (a). In a 4T APS, the site of photodetection and photoconversion are separated by an additional transistor, TX. Photodetection is conducted within the pinned-photodiode (PPD) and the accumulated charges are transferred to a floating diffusion (FD) and converted to a voltage. The cross-sectional view of this region is illustrated in the figure. PPD is a specialized photodiode structure based on conventional photodiode. In contrast to the conventional PD, there is a very

thin pinning P++ layer on top of the PN junction, hence forms another PN junction close to the silicon surface. There are advantages with this structure. Firstly, PPD demonstrates a better light sensitivity than conventional photodiode since another PN junction on top of the the N region extends the depletion region to the surface, which enables the effective carrier collection generated by short wavelength photons. Moreover, the pinned layer isolates N region from the defective Si/SiO2 interface so as to reduce the dark current generated from the interface states. However, the fabrication of PPD requires the support of specialized CMOS image sensor process, which is more expensive than standardized CMOS process. Many CMOS image sensor process are developed from mixed-signal CMOS process and offered as an additional process option in many foundries.

The 4T APS can achieve low noise readout and provides the imaging performance comparable to CCDs. A proper timing can be devised together with the use of charge transfer characteristics to supress kTC noise. The pixel operation procedure is illustrated with the help of potential diagram [46], as shown in Fig. 2.10. It is assumed that in the reset phase, there are no accumulated charges in the PPD, thus the PPD is completely depleted. The photogenerated charges are accumulated in PPD when the FD is reset by turning on the the reset transistor $M1$. The reset level, V_{RST} is read out firstly by turn on the row select switch $M3$. After the reset readout is complete, the charges in PPD is then transferred to the FD by turning on the transfer gate TX, followed by the signal readout (V_{SIG}). It can be noted the voltage difference between the reset level and the signal level is strictly proportional to the amount of accumulated charges in PPD. The readout of both reset level and are short enough in time, which is essential for correlated double sampling (CDS) to cancel the kTC noise in column signal processing.

A carefully designed potential profile in PPD, FD and the transfer gate is required to assure a complete depletion in PD as well as a complete charge transfer through TX.

2.3.5 Performance Analysis

There are a number of important features and characteristics used to describe the performance of CMOS image sensors. This sections gives a detailed description.

2.3.5.1 Quantum Efficiency

Quantum efficiency (QE) is one of the main characteristics to describe the photodetector performance. It is defined as the fraction of incident photon flux on the photodetector that contributes to the photogenerated charges. It is a function of wavelength (400-700 nm range of visible light for silicon) and is always less than one for the discussed photodetectors. QE is largely determined by the doping concentration of the photodetector, geometric arrangement of the photodetector, reflection of the dielectric property above the photodetector, etc.

2.3.5.2 Dark Current

Dark current, also termed as dark signal, is another characteristic of the photodetector. It is the signal response when there is absence of light to the photodetector. The generation of dark current is due to thermal generation of charge carrier. They are related to many design and technology factors including the silicon defect density, the bias condition of the photodetector and operation temperature. Dark current is generated by several sources, including diffusion current, tunnel current, generation-recombination current in the depletion region, impact, ionizing current, surface leakage current due to surface states [46]. Dark current consumes the well capacity unexpectedly. It also varies with time and the pixel location, producing the temporal and spatial variation. The temporal variation contributes to the random noise while the spatial one adds to the fixed pattern noise.

2.3.5.3 Fill Factor

Fill factor (FF) is a parameter related to pixel geometry. It is defined as the percentage of the photosensitive area to the entire pixel area. CCD achieves around 100% fill factor. Incorporating transistors in the pixel will inevitably reduce the fill factor. A high fill factor is generally desired to achieve . The use of microlens and back-side illumination (BSI) helps to increase the effective fill factor of modern CMOS image sensors.

2.3.5.4 Temporal Noise

Temporal noise, also termed as random noise, is the variation in pixel values under same illumination from frame to frame [47]. It is independent of the pixel location in the array. There are several temporal noise sources in CMOS image sensor including photon shot noise, pixel reset noise, thermal and flicker noise in readout circuits and quantization noise in ADCs.

More specifically, photon shot noise is the noise associated with the random arrival of photons. It is an expression of a natural process rather than pixel design or fabrication technology. Thus, photon shot noise is the most fundamental noise among all the noise sources.

Reset noise is mainly associated with thermal noise in reset operation. When the accumulated charges are reset through reset transistor, the thermal noise $4k_BTR_{ON}\Delta f$ is sampled in accumulation mode, where the Δf is the bandwidth and R_{on} is the ON-resistance of the reset transistor. The thermal noise is calculated to be k_BT/C_{PD}, where C_{PD} is the photodiode capacitance. The k_BTC_{PD} noise can be eliminated by the CDS operation.

Thermal and flicker noise is added by the readout circuits. They are due to the transistors along the readout path. The summed noise sets the noise floor of the sensor, which restricts the imaging performance, especially under low illumination conditions.

2.3.5.5 Fixed Pattern Noise

In addition to temporal noise, CMOS image sensors also suffer fixed pattern noise (FPN). FPN refers to the inter-pixel output variation under uniform illumination due to device mismatches. It is time-invariant noise component. There are mainly two types of FPN: offset FPN and gain FPN. Offset FPN is independent of pixel signal but gain FPN due to the gain error of the readout circuits, varies with the signal magnitude. In addition, another serious FPN source is the column FPN introduced by the column signal processing circuits. Such FPN can cause visibly stripes in the image. There are various noise cancelling circuit techniques [45] to suppress the FPN.

2.3.5.6 Signal-to-Noise Ratio and Dynamic Range

Both temporal noise and FPN influence the image quality the sensor produces. It is often characterized by the signal-to-noise ratio (SNR) and determine the illumination range the sensor can detect, known as dynamic range (DR).

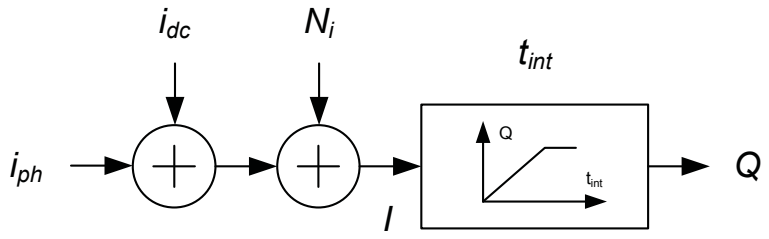


Figure 2.11: A simplified CMOS image sensor model, adapted from [2]

Using a simplified CMOS image sensor model [2], a quantitative analysis of SNR and DR is presented. Fig. 2.11 shows the simplified integration mode sensor model, where i_{ph} is the photocurrent and i_{dc} is the dark current and the Q is the output signal in the form of charge. N_i represents the zero-mean input referred noise of the CMOS image sensor. The simplified model assumes CDS is performed to cancel the FPN effectively and various noise components in the sensor are uncorrelated. Average noise power due to

photon shot noise is $q\left(i_{ph}+i_{dc}\right)t_{\text{int}}$, where q is the electron charge. Average noise power due to readout circuit and ADC quantization is σ_{read}^2.

With this model and these assumption, the SNR, which is the ratio of the signal power to the total average noise power, can be presented as:

$$SNR = 10\log_{10}\frac{\left(i_{ph}t_{\text{int}}\right)^2}{q\left(i_{ph}+i_{dc}\right)t_{\text{int}}+\sigma_{read}^2} \qquad \text{(Eq. 2.7)}$$

The dynamic range (DR) quantifies the capability to image intra-scene wide variation in illumination. It is defined as the ratio of the maximal non-saturating signal(i_{max}) and minimal detectable signal(i_{min}) under dark conditions. The largest saturating signal is determined by the well capacity and integration time, while the minimal detectable signal is limited by the noise floor under dark conditions.

Using the same sensor model, DR can be expressed as:

$$DR = 20\log_{10}\frac{i_{\text{max}}}{i_{\text{min}}} = \frac{Q_{well}-i_{dc}t_{\text{int}}}{\sqrt{qi_{dc}t_{\text{int}}+\sigma_{read}^2}} \qquad \text{(Eq. 2.8)}$$

where Q_{well} is the well capacity. Note that DR increases with increasing well capacity and decreasing readout noise. Also, DR decreases as integration time increases due to adverse contribution of the dark current.

2.4 Radiation Tolerant CMOS Image Sensor

Space environment is associated with complex radiation exposures characterized with various sorts of energetic particles. The main sources of energetic particles are: 1) protons and electrons trapped in the Van Allen belts, 2) heavy ions trapped in the magnetosphere, 3) cosmic ray protons and heavy ions, and 4) protons and heavy ions from solar flares [48]. The exposures pose a hazard to microelectronic devices on satellite if their orbiting spends significant time in the radiation belt. Usually these devices are protected with adequate shielding during the operation. Nonetheless, for radiation sensitive devices as CMOS

image sensors, their capability to withstand the radiation effects is of a major concern. This section provides an overview of radiation effects to CMOS circuits. The impact of radiation has historically been categorized into two groups: one reflects the effects over a long period of time, termed as total ionizing dose and the other is the immediate result of a single radiant charged particle, known as single event effects .

2.4.1 Total Ionizing Dose Effects

The Total Ionizing Dose (TID) effects are cumulative effects from ionizing radiation and the impact on device performance is determined by the exposure history. Energetic particles present in the radiation environment such as high-energetic electrons and protons can ionize atoms and generate electron hole pair (EHP) in the oxide. The generated electrons or holes can further impact other atoms and generate EHP as long as the energies of them are higher than the minimum ionizing energy required to excite the electron. In this manner, a single, high-energetic incident particle can create thousands of EHPs in the oxide. The mechanism is depicted in Fig. 2.12, which illustrates a band diagram of a biased NMOS capacitor in P substrate under ionizing radiation. Immediately after EHPs are generated, the electrons are mobile and easy to be swept out of the oxide quickly. The holes, despite the electron-hole recombination, will be hop toward to the silicon/silicon dioxide interface through localized states in the oxide. As the holes approach the interface, some portion will be trapped and form a positive trapped charge buildup and interface states. During the hole's movement, hydrogen ions (protons) are likely to be released and also drift towards the silicon/silicon dioxide interface, where they may react to form interface traps. This oxide degradation leads to almost all consequent TID effects [49]. Based on the different location the oxide degradation occurs, three major and consequential effects are shift of threshold voltages, edge leakage in NMOS transistors, and NMOS inter-transistor (isolation field) leakage current [50] .

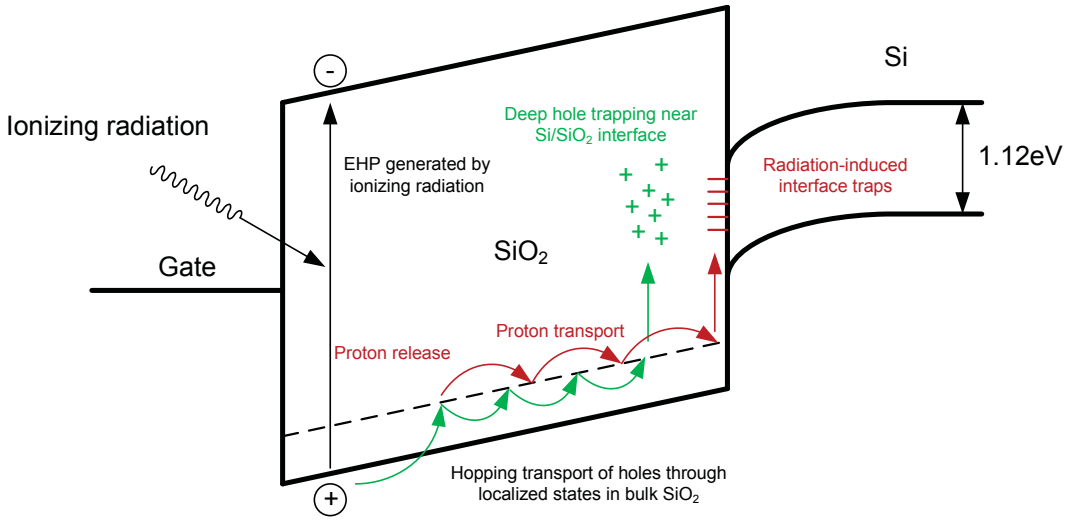


Figure 2.12: Band diagram of a MOS capacitor with positive gate bias. The process of radiation-induced device degradation is illustrated, adapted from [3]

2.4.1.1 Threshold Voltage Shift

When hole trapping occurs in gate oxide, it causes a negative shift in threshold voltage of a transistor, which inclines to turn NMOS transistor and turn off PMOS transistor. On the other side, interface states are negatively charged in NMOS transistor and positively charged in PMOS transistor, leading to positive threshold shift in NMOS and negative threshold shift in PMOS transistor, respectively. The magnitude of the threshold voltage shift is proportional to the degree of the hole trapping and also to the thickness of the oxide. Thus, the magnitude of radiation induced threshold voltage shift was experimentally found to get considerably smaller when the thickness of the gate oxide is less than 12 nm (found in deep submicron CMOS technologies), the radiation induced holes in the gate oxide have a much better chance to tunnel out of the oxide (requiring only 6 nm effective tunneling distance) before they are trapped [48].

2.4.1.2 Leakage Current

The dominant source for TID effects is then the presence of thick field oxide (FOX) or shallow trench isolation(STI) that isolate MOS devices. As the positive radiation-induced charges build up in the transition region at the sides of the MOS device, as shown in Fig. 2.13, it can cause inversion channels beneath it and generate two parasitic edge leakage path which will greatly increase the device leakage current. These parasitic side channels can corrupt the characteristics of the whole device, especially for narrow (small W/L) transistors. Edge leakage are typically reflected as a rapid increase in static supply current, while they may also cause functional failure as the parasitic channel cause the device permanently turned on. Another possible leakage path due to TID effects is the one between adjacent transistors. For example, a leakage path between a N-well (which is typically connected to VDD) and a N+ source (typically connected to VSS) can directly draw current from VDD to VSS, resulting in a sharp change in supply current with increasing radiation.

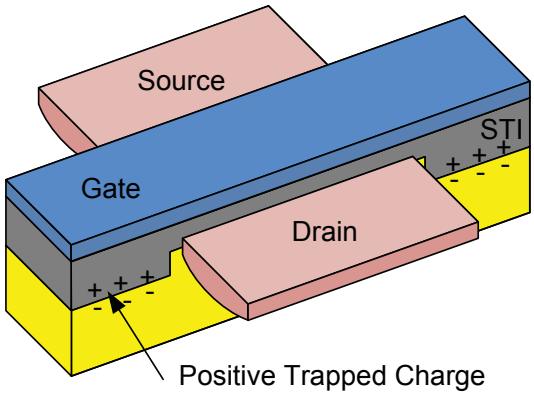


Figure 2.13: Cross-section of a transistor where positive charges due to ionizing radiation are accumulated at the edges of the transistor

The most effective way against this edge leakage current is by layout enhancement [50]. As a comparison, Fig .2.14 shows the layout details between the normal transistor

layout and the enclosed layout transistor (ELT). In ELT, one diffusion region is enclosed completely by the gate so that there is no such isolation field connecting the source and the drain. Therefore the edge leakage path is eliminated. A variety of ELT have been proposed and discussed [51] [52] [53]. One thing to note is that ELT has asymmetric structures, meaning the diffusion size and its parasitic capacitance must be different. Besides, ELT has a much larger minimum W/L ratio due to the annular structure. Moreover, in order to curtail the leakage between transistors, P+ guardring is usually used as a channel stop implanted at the interface between the field oxide and the silicon. The high doping of this P+ guardring is much difficult to invert and thus effectively breaks the leakage path.

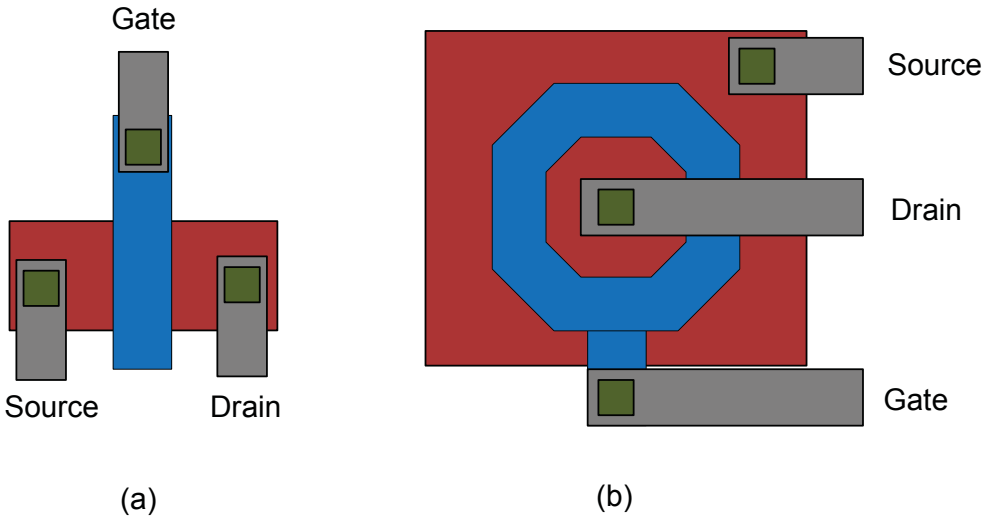


Figure 2.14: (a) Normal transistor layout, (b) Enclosed layout transistor.

2.4.1.3 TID Effects in Active Pixel Sensors

Like other semiconductor devices, APS shares the various radiation-induced undesirable characteristics due to the in-pixel transistors. CMOS image sensors are inherently susceptible to TID-induced leakage current. In fact, one of the most significant observed

radiation-induced degradation is the dark current increase [54] [55] [56]. Therefore, earlier radiation tolerant pixel designs attempts at applying these layout enhancement to pixel transistors [57] [58] [59] as the countermeasure to this dark current increase. Nonetheless, the leakage current can also rise from the TID-induced defects in the photodetectors. It has been discovered that the dark current depends on the physical interaction between oxide isolation and the PD [60]. This is primarily due to the formation of the interface states in the region. Once these interface states are in a depletion region, they result in the source of dark current. The direct interaction of the N+ diffusion of the conventional PD with peripheral shallow trench isolation (STI) walls, where most interface states are located, and can be disastrous according to the the TID-induced leakage mechanism. There have been research efforts in analyzing the TID effects on various photodetector designs [61] [62], especially in deep submicron technology [63].

Recently, advanced pinned photodiode structure and 4T APS have become the choice of radiation-tolerant pixel candidate [64]. Overall TID effects on 4T APS have been investigated [65] [60]. Degradation in spectral response has been analyzed [66]. Degradation in the pixel performance has been outlined in [67]. According to the results, one of the motivations is to reduce the surface generated dark current [68] thanks to the pinning layer, which can help prevent the interaction between the PD and the radiation-induced surface states. In addition, P-well protection around the PD can help mitigate the influence of the STI around the PPD. Fig. 2.15 shows the recessed-STI photodiode [68]. The N+ diffusion is placed away from the STI sidewalls deliberately with a distance. In order to further push away the depletion region away from the STI wall, a P-well pinning layer is used to enclosed the STI wall. The principle of P-well pinning layer is similar to the pinning layer on top. P-well protection has relatively higher doping density than P-substrate, which further makes the depletion region away from the STI. The use of recessed-STI PPD with P-well protection has proved to be effective in

improving dark current performance [62] so that it can be a potential radiation tolerance solution in terms of isolating those radiation induced interface states from the critical charge collection [66] [69].

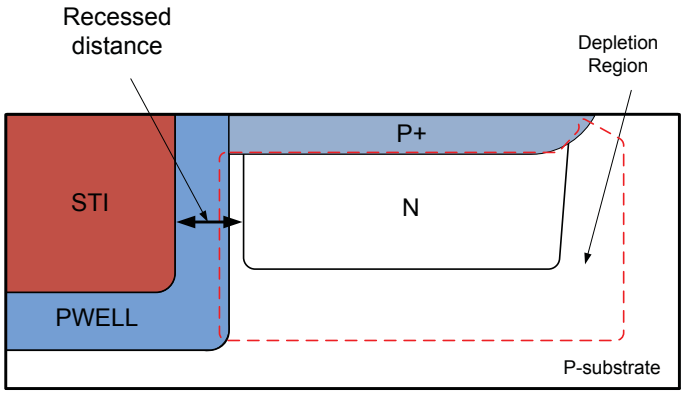


Figure 2.15: Cross section of a recessed-STI photodiode.

Moreover, 4T APS has a complex photodetection and photoconversion structure (PPD, TX and FD), so the causes of the TID-induced degradation is more complex. There have also been extensive research efforts on this region. [70] provides the radiation characterization of this region. The influence of TX, in particular, is discussed in [71]. An ELT TX, which encloses the FD, has been proposed in [72].

2.4.2 Single Event Effect

Besides TID effects, Single Event Effects (SEE) have become even more problematic for CMOS VLSI circuits in the deep submicron regime [73]. This is primarily due to shrinking feature sizes, lower voltages which cause reduced noise margins. Single Event Transients (SET) occurring in combinational logic are a more critical detractor for system reliability. These transients are able to propagate and latched improperly in a memory element, causing Single Event Upsets (SEU). Another SEE risk of CMOS technology in radiation environment comes from latch-up problem. Single Event Latchup (SEL) occurs

in bulk CMOS devices because of the parasitic NPN and PNP bipolar transistors. These parasitic transistors are in a positive feedback configuration. The impinging high energy particle is able to spur the positive feedback and eventually render large currents flowing in the CMOS devices, usually shorting the power supply. Latch-up generally does not clear itself and can cause permanent damage to the circuit.

2.5 Overview of Wide Dynamic Range CMOS Image Sensors

To expand the dynamic range, various solutions to extending the dynamic range in CMOS image sensors at the pixel, circuit, and system level have been proposed and demonstrated recently. They can be coarsely divided into four main categories [74]: logarithmic response, well capacity adjustment, dual/multiple sampling and saturation detection.

2.5.1 Logarithmic Pixel

The logarithmic pixel is inherently capable of capturing wide dynamic range intra-scene images. In contrast to APS operating in integration mode (voltage mode), the logarithmic pixel operates continuously in time (current mode). The schematic of a conventional three-transistor (3T) logarithmic pixel is shown in Fig. 2.16. The logarithmic pixel is very similar to a conventional 3T APS. $M2$ and $M3$ function as a source follower and row select, respectively. The difference is the way $M2$ is connected. The gate of $M2$ is connected to VDD and form a diode-connected NMOS transistor, instead of to an external reset signal in a 3T APS. The small photocurrent, I_{PH}, is supplied by $M2$, so $M2$ is in the subthreshold region. Its gate-source voltage ($VDD - V_{PD}$) changes as the logarithm of I_{PH}, providing non-linear compression on the photocurrent. The compression allows a wider range of illumination can be detected.

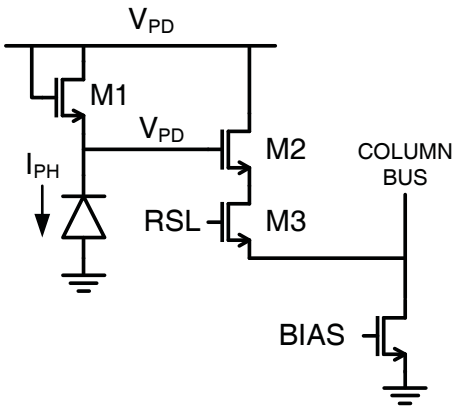


Figure 2.16: Conventional 3T logarithmic APS

This inherent compression of photocurrent holds the advantage that high dynamic range can be achieved within a small output signal range and hence it is ideally suitable for the reduced voltage swing in deep sub-micron technologies. However, logarithmic pixel suffers a number of considerable disadvantages including lower SNR, increased FPN and image lag. In particular, the performance of logarithmic pixels are drastically limited at low illumination level. At low illumination level, photocurrent falls commensurate with or even much smaller than the dark current and the dark current becomes the dominant contribution of the logarithmic response. As a result, SNR is lowered. In addition, logarithmic pixel exhibits higher FPN due to the subthreshold characteristics of a NMOS transistor. Therefore, logarithmic pixel requires a complex calibration process to calibrate the offset and gain error due to the process variation. Moreover, it is also hard to conduct FPN calibration as is done in APS due to the lack of reference level.

In order to address the aforementioned issues, there have been some approaches to incorporate both logarithmic and linear responses in one sensor. The idea is to use the linear response preferably in the low illuminated condition, while the logarithmic response is suitable in the high illuminated condition. In this manner, the sensor remains a relatively high SNR for the dark light region while the extension of the DR is achieved

by the logarithmic. Different logarithmic-linear pixel architectures have been proposed [4] [75]. [76] proposed a threshold voltage cancellation scheme to achieve low FPN in a logarithmic-linear pixel. The authors in [77] have combined the logarithmic and linear responses in one 4T APS.

As a representative design, a combined linear-logarithmic CMOS image sensor in [4] is explained as follows. The sensor is capable of imaging in both linear and logarithmic modes of operation within one pixel. Both sets of data are acquired and combined to generate a high dynamic range image. The schematic of the proposed pixel is shown in Fig. 2.17. The pixel consists of seven transistors, which can be configured to allow the pixel to operate in both modes. For linear operation, $M4$ functions as a reset transistor which reset the pixel voltage to the Vrt assigned on $col4$. To turn on $M6$ and precharge the gate of $M2$ to 0V on $col3$, $M2$ is turned off to prevent the conducting current from Vrt to pix. $M5$ remains on while $M1$ and $M3$ function as source follower and row select, respectively. In this configuration, the pixel behaves like a conventional 3T APS and output the integration result on pix after a exposure period. $M7$ is an anti-blooming transistor which allows the excessive photo-generated charges to flow to Vrt.

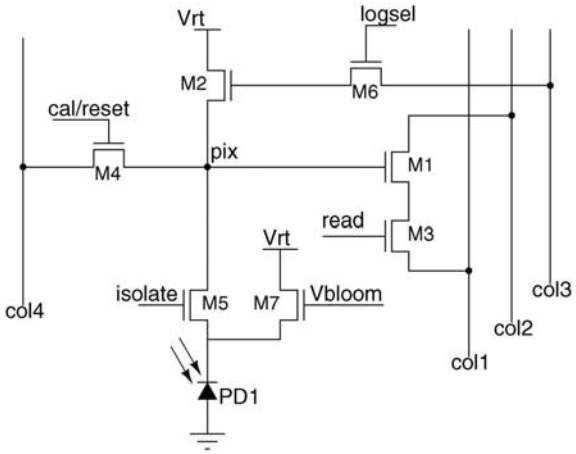
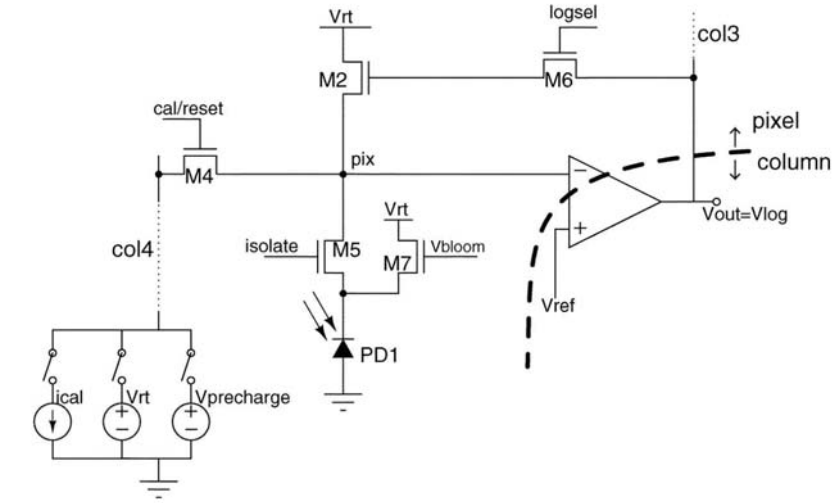
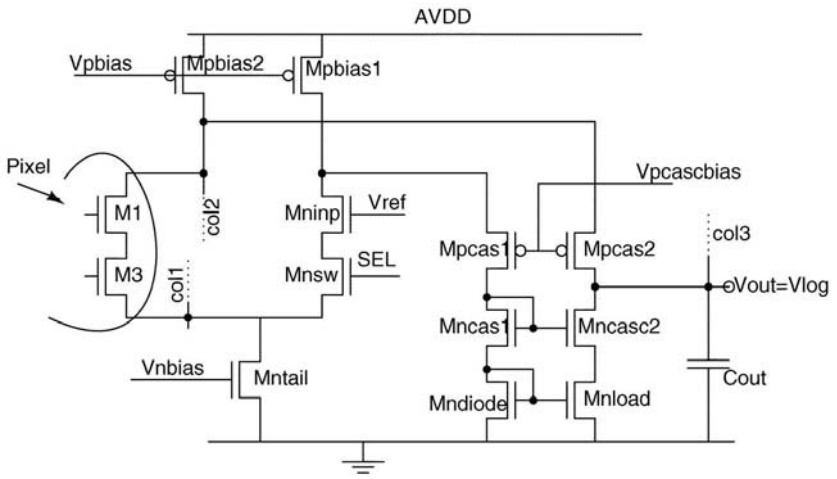


Figure 2.17: Schematic of the linear-logarithmic pixel, adapted from [4].

To derive a logarithmic response, the pixel is configured as the shown in Fig. 2.18 (a). M1 and M3 become the input transistors of an column amplifier and the rest of the amplifier resides in the column, as shown in Fig. 2.18 (b). The pixel-column connection forms a negative feedback loop, which settles the *pix* node to the reference voltage. The output voltage on *col*3 follows a logarithmic response to the photocurrent.



(a)



(b)

Figure 2.18: (a) Logarithmic pixel configuration and (b) Column amplifier for logarithmic operation, adapted from [4].

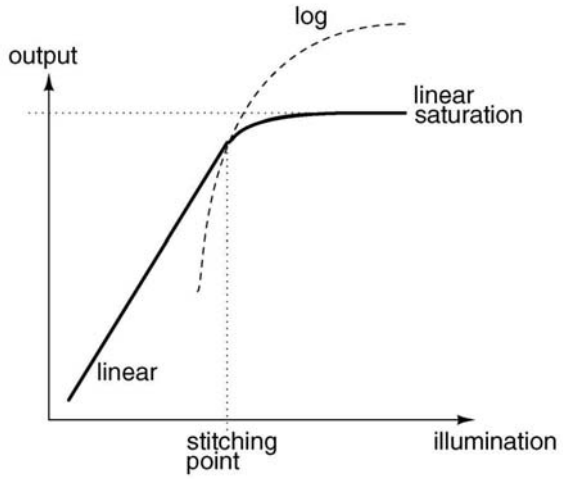


Figure 2.19: Combined linear-logarithmic response curve, adapted from [4].

Both linear and logarithmic data are acquired for each pixel, they are combined to render a WDR image in post processing. Fig. 2.19 shows the synthesis curve from linear and logarithmic response curve. The logarithmic curve has been properly aligned to the linear response around the stitching point. When the illumination is below the stitching point, linear response will be used and logarithmic response is selected above the stitching point. This scheme takes both advantages of the high SNR of the linear data in the dark light region and logarithmic compression in bright light region. It effectively addresses the lower SNR issues in conventional logarithmic pixels.

2.5.2 Well Capacity Adjustment

The well capacity adjustment is a technique to adjust the well capacity in the charge integration site during exposure. A drain for the overflow charges is used in this technique to hold the excess charges. As high illumination impinges on the pixel, the photo-generated charges are saturated in the PD and flow over into the drain. The saturated charges on PD together with the overflow charges on the drain are then the total collected charges. In [5], an in-pixel lateral overflow integration capacitance (LOFIC) is used to

hold the overflow charges. Following this thread, [78] and [79] proposed an additional column capacitor as LOFIC to further extend the dynamic range. The pixel architecture is simple and devised operation timing allows for CDS operation. Noise reduction benefits from the CDS so that a high SNR and a low FPN can be obtained.

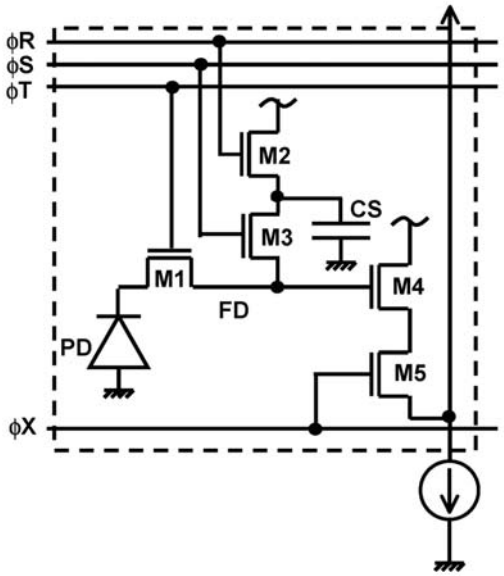


Figure 2.20: Pixel schematic, adapted from [5]

The pixel schematic in [5] is illustrated in Fig. 2.20. The pixel is composed of a pinned photodiode (PPD), a floating diffusion (FD), an overflow capacitor (CS), a charge transfer gate ($M1$), a reset switch ($M2$), a switch between the FD and CS ($M3$), source follower ($M4$) and row select switch ($M5$).

The corresponding pixel timing and potential diagram at the respective timing phases of the operation are shown in Fig. 2.21 and Fig. 2.22, respectively. In advance to the exposure, FD and CS are connected by turning on switch $M3$ and turning off $M1$ and $M2$. At this time point, PD is completely depleted and ready for integration. At t_1, FD and CS are reset by turning on $M2$. The reset noise and threshold voltage variation of $M4$ are immediately sampled as $N2$ after turning $M2$ off. During the exposure (t_3),

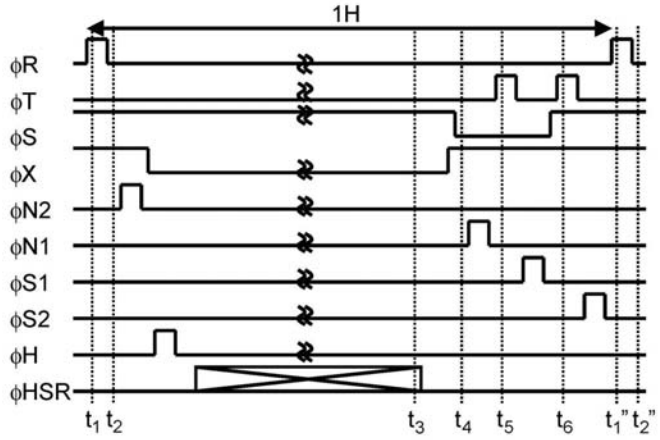


Figure 2.21: Timing diagram of the pixel operation, adapted from [5]

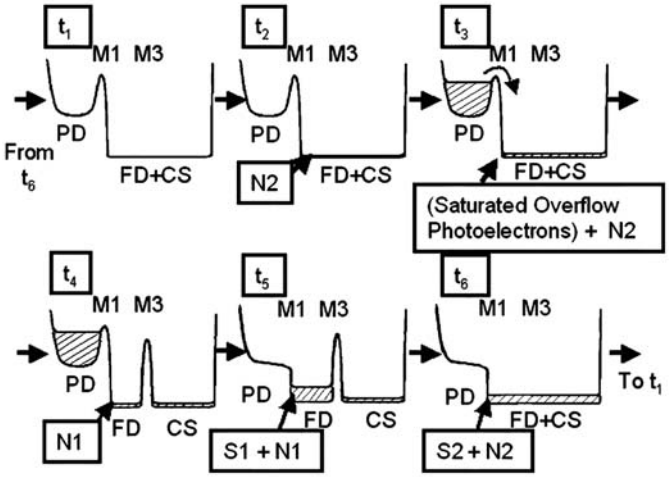


Figure 2.22: Potential diagram of the pixel operation, adapted from [5]

photo-generated charges are integrated on the PD and flow into both FD and CS when it is saturated. At this operation phase, $M1$ operates as the overflow path. The collection of the overflow charges enables the utilization of the overflow photoelectrons for the signal charges. At t_4, signal charges on FD and CS are separated in accordance with their capacitance by turning off $M3$. The residue charges in FD are read out, noted as $N1$. right after that at t_5, the charges in PD are completely transferred to FD by turning on and off $M1$. Charges on FD is read out as $S1 + N1$. Note that the charge transfer is

complete, $S1+N1$ is not affected by the device variation, especially the threshold voltage variation of $M1$. At t_6, all the charges in FD and CS are mixed together and sampled as $S2+N2$. At this moment, $M1$ is turned off so that PD is reset. Finally $M2$ is turned on to reset both the FD and the CS for next capture. This complete operation allows the integrated charges to be read out without any loss and the extension of dynamic range with linear signals.

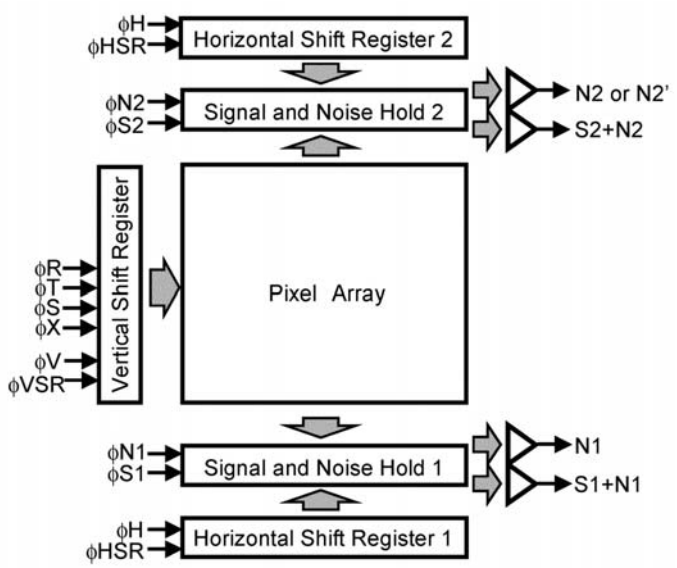


Figure 2.23: Block diagram of the sensor architecture, adapted from [5].

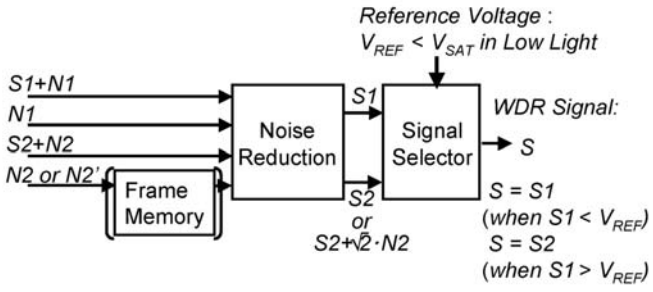


Figure 2.24: Signal processing flowchart of the dynamic range extension, adapted from [5].

The obtained signals are used to synthesize the HDR image by the post processing

of the signals. Fig. 2.23 shows the sensor block diagram. Two sets of sample and hold circuits are incorporated for the signal readout circuits. The signal $N2$, $N1$, $S1 + N1$, $S2 + N2$ are read out sequentially. The real non-saturated signal $S1$ is calculated by subtracting the readout signal $S1 + N1$ with the noise readout $N1$. Similar operation is done to obtain $S2$, which is total signal charges collected on PD, FD and CS. With both $S1$ and $S2$ at hand, the composition of WDR signal(S) is performed by thresholding with a reference voltage, as shown in Fig. 2.24. The reference voltage is supposed to be set lower than saturation level of the $S1$ to avoid the influence of the saturation voltage variation. On the other hand, the reference voltage is also supposed to be as high as possible to maintain the high SNR in $S2$.

2.5.3 Dual or Multiple Sampling

Techniques from this group are based on sampling of the identical scene two or several times with different length of exposure time and synthesize those samples in one image. Generally, the techniques require sample and hold circuits (frame memory) to store the previous samples and no changes of pixel structure [80]. Therefore it can be applied to a 4T APS for high resolution integration. To avoid the usage of large frame memory, a column level illumination detection scheme is proposed in [81]. In [6], the floating diffusion in the 4T APS is used as the memory. In other architectures proposed in [82] and [83], no external memory is required since the dual sampling uses PD for storage. The output image can be obtained from these samples according to different synthesis algorithm. Some algorithms use the last sample before saturation. Others may include introducing a weighing factors between these samples. The weighing factors are less than one, and can be determined by the ratio of the long exposure time to short exposure time.

Using dual sampling as an example, the principle of the dynamic range extension is explained in details as follows. Generally DR is given by

$$DR = 20 \log \frac{I_{\max}}{I_{\min}}(dB) \quad \text{(Eq. 2.9)}$$

where $I_{\max}$ and $I_{\min}$ are the maximum and the minimum photocurrent that can be handled in the pixel. $I_{\max}$ and $I_{\min}$ are given by

$$I_{\max} = Q_{\max}/T_S \quad \text{(Eq. 2.10)}$$

and

$$I_{\min} = Q_{\min}/T_L \quad \text{(Eq. 2.11)}$$

where $Q_{\max}$ is the maximum signal charge that can be collected in the pixel, $Q_{\min}$ is the minimum signal charge determined by the noise level and T_S and T_L are the short and long exposure time, respectively. Thus DR can be reorganized as

$$DR = 20 \log \frac{Q_{\max}}{Q_{\min}} \frac{T_L}{T_S}(dB) \quad \text{(Eq. 2.12)}$$

Compared to the single capture, the dynamic range can be expanded by a factor of T_L/T_S.

The combination of two exposure times, on the other hand, causes a SNR dip at the edge of switching the use of the samples. The SNR dip is general in dual sampling and is largely related to the ratio of long exposure time and short exposure time. Fig. 2.25 shows the concept of the SNR dip when two exposure times are merged. Compared to the SNR curve of the long exposure time, the SNR curve of the short exposure time shifts toward the higher light intensity. If the photocurrent exceeds $Q_{\max}/T_L$, the output is switched to the short exposure time signal. At this transition point, the signal charge is reduced from $Q_{\max}$ to $Q_{\max}(T_S/T_L)$. If the SNR is determined in terms of signal of each exposure level and the noise charges mainly due to shot noise, the SNR dip, is represented as

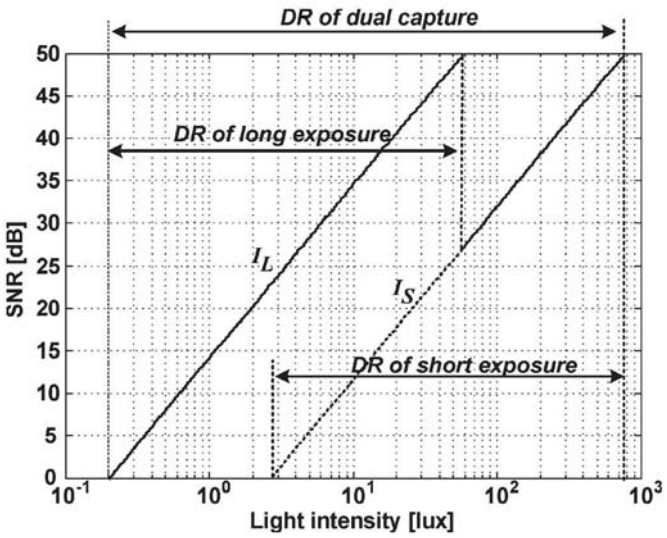


Figure 2.25: SNR versus light intensity, adapted from [6].

$$\Delta SNR = 10 \log_{10}(T_S/T_L) \qquad \text{(Eq. 2.13)}$$

Therefore, the ratio of T_L and T_S should be carefully designed. It cannot be too large to result in a large SNR dip while a small ratio only comes with a small expansion of DR. As a common practice as mentioned previously, a lowest SNR of 40dB should be provided at this switching point. To handle the SNR dip in dual capture, more complex readout manner of multiple exposure with varying short exposure time are proposed. The authors in [7] employed several different exposure times in one frame readout. During the readout time of one short exposure period, a even shorter exposure period is inserted, while a further shorter exposure period is inserted and so on. This is shown in Fig. 2.26. In this manner, the expansion of the DR is still determined by the the ratio of longest and shortest exposure time. But the SNR dip can be improved by making a proper ratio between two varying exposure time.

2.5.4 Saturation Detection

The saturation detection is based on monitoring and controlling the saturation signal. The method lets the pixel achieve its saturation level and record the time it takes to achieve the saturation state. By retrieving the time information before saturation on the specific pixel, the post processor is able to rebuild the image by extrapolating the incident light. Since saturation detection measures the time it takes the photocurrent to produce a given voltage change at the sense node, it switches from the voltage domain to time domain and the dynamic range is no longer restricted by the low supply voltage and small well capacity and thus extended. The scheme is very similar to the time-domain imaging proposed on a number of imaging applications, such as the time-to-first-spike(TFS) scheme [41] in bio-inspired CMOS imaging system to simulate retina encoding. Time-domain imaging uses pulse modulation (PM) to encode the time quantity. In general, PM can be classified into two categories, pulse width modulation (PWM)

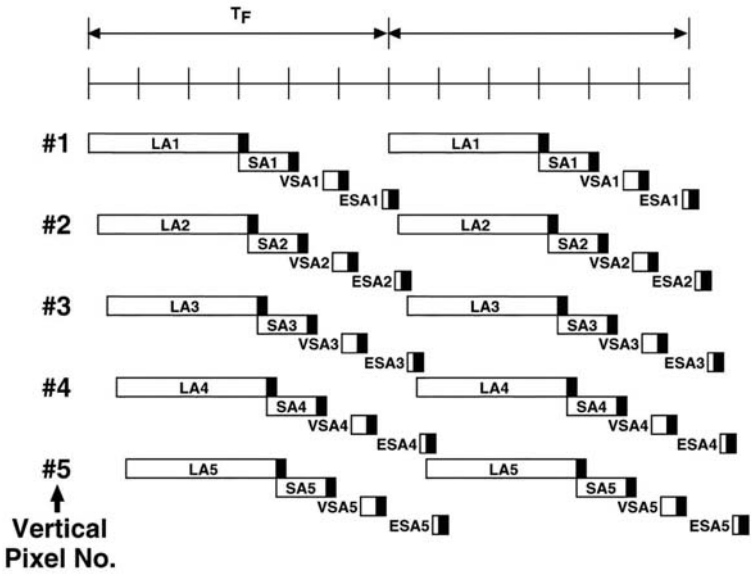


Figure 2.26: Timing diagram of the multiple sampling with different exposure lengths, adapted from [7]. Four exposure lengths are used, namely LA: long accumulation, SA: short accumulation, VSA: very short accumulation, ESA: extremely short accumulation.

and pulse frequency modulation (PFM). Fig. 2.27 shows both encoding mechanism of the exposure information. In contrast to the APS, the pixel connects the sense node to a comparator which toggles states when the voltage on the sense node crosses some reference value. The states are simply reflected in the binary signal. When the signal is used to latch a timer and reset of the pixel is done by external controller as the case of PWM in Fig. 2.27 (a). If the signal is connected to the reset transistor to form a closed loop, the pixel becomes an oscillator which outputs pulses at a frequency related to the instantaneous photocurrent (integration rate) as shown in the Fig. 2.27 (b).

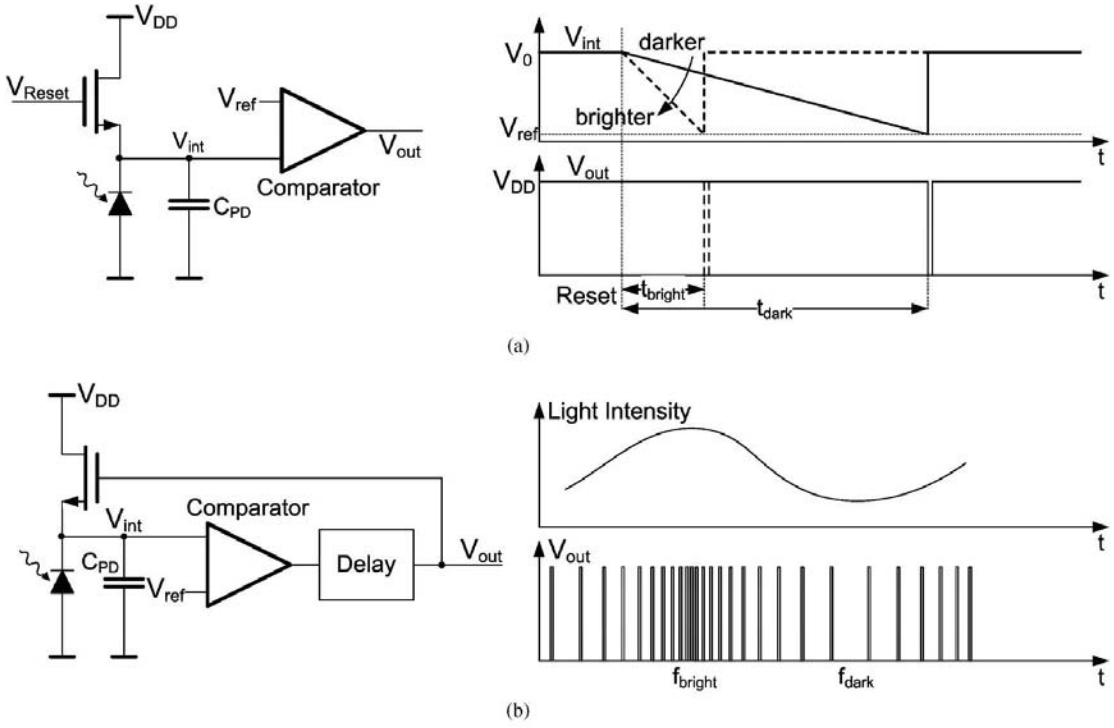


Figure 2.27: (a)PWM and (b) PFM encoding scheme of exposure information, adapted from [8].

The SNR usually benefits from the PWM encoding. This is because in each integration cycle, the pixel is not read out until it approaches a threshold voltage, sometimes maximum integration voltage. Accordingly the achievable SNR is essentially irrelevant

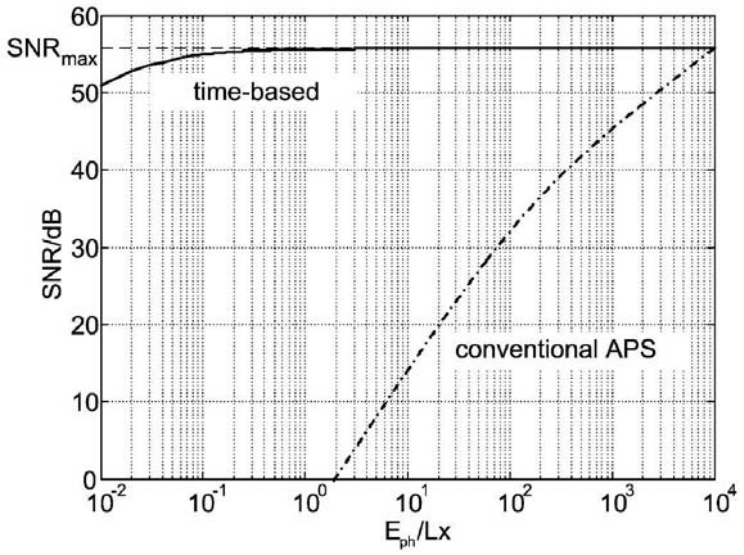


Figure 2.28: SNR comparison between a conventional APS and a time-domain pixel as a function of illumination levels, adapted from [8].

to the size of illumination and photocurrent. Fig. 2.28 plots SNR comparison between a conventional APS and a time-domain pixel as a function of light intensity (photocurrent). The SNR is highly dependent on the light intensity while even for low light conditions, SNR for time-domain pixels remains almost unchanged. However, in order for such kind of pixel to sense and store the time information, it needs a detection circuit, normally composed of a comparator, analog/digital memories and some switches, to be incorporated into each pixel, it unexpectedly result in increasing the pixel size and lowering the FF, which inevitably restricts the high density integration.

There have been a number of designs featuring the saturation detection [84] [85]. As an representative example, Fig. 2.29 illustrates the general WDR concept proposed in [9]. The basic idea is PWM and the time it takes the voltage on $Cint$ to reach the threshold Vth is encoded in the form of voltages stored on two analog memories (capacitors). The light intensity is hence derived by the information on the toggling time.

For the purpose to record the saturation time in each pixel without helps of external

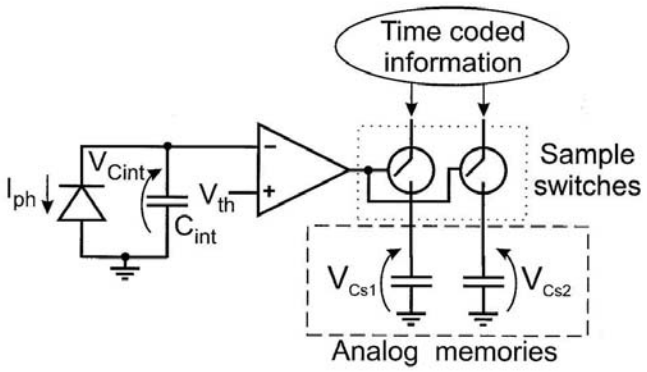


Figure 2.29: HDR pixel concept, adapted from [9].

circuit elements, and to allow a linear mapping of high timing range, two voltage ramps have been used to suitably encode the time information Fig. 2.30 plots the operation timing of the HDR pixel, in particular, the details of two time-coding voltage ramps. Two scenarios indicating both high and low illumination conditions have been illustrated. On one hand, in case of low illumination condition, where there is no toggling of the comparator occurring throughout the integration time, the voltage on the photodiode is directly readout similar to normal APS operation. On the other hand, the voltage signals, $Vramp1$ and $Vramp2$, on two analog memories are stored and provide the time-coded information in high illumination condition. $Vramp1$ sweeps back and forth in a 1V range N times. $Vramp2$ monotonically decreases in steps of $T, 2T, ...2^{N-1}T$ and divides the 1V range in N equal parts. Consequently, $Vramp2$ allows to discriminate between different time slot before complete integration time and Vramp1 provides a more discreet resolution of time with each time slot. As in the case shown in Fig. 2.30, two voltages $Vcs1$ and $Vcs2$ are sampled, respectively. Accordingly, the values can uniquely produce back the the value t_c with a high resolution provided both ramping voltage.

The beneficial DR extension results from the high detectable photocurrent by the pixel architecture, where the maximum detectable photocurrent is determined by the resolution

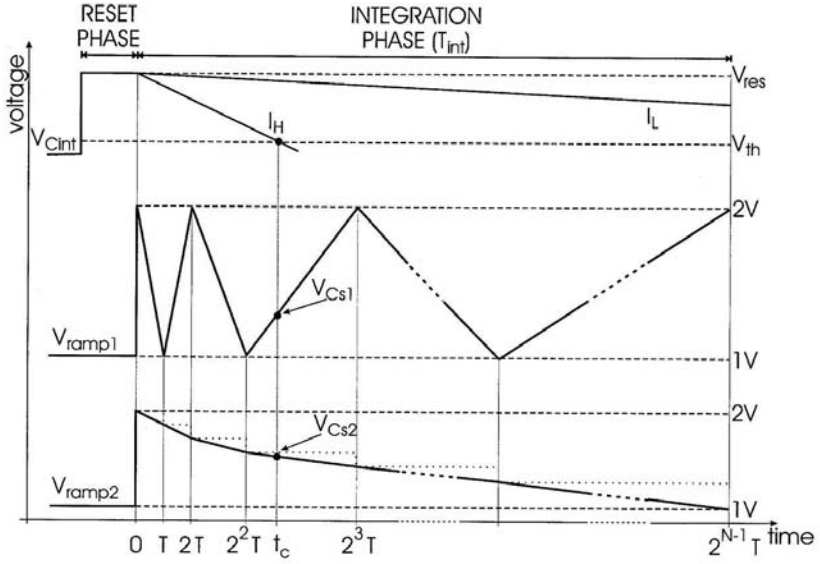


Figure 2.30: HDR pixel operation timing, adapted from [9].

with which the voltage Vramp1 is generated. The extended DR is characterized by an overall dynamic range enhancement factor (DRF), which is expressed by

$$DRF = \frac{T_{\text{int}}}{T_{LSB1}} \qquad \text{(Eq. 2.14)}$$

where T_{LSB1} is the minimum detectable time, corresponding to the temporal LSB in the first time slot divided by $Vramp2$. Therefore, assuming a k-bit resolution for $Vramp1$, the DRF is:

$$DRF(dB) = 20 \cdot (N - 1 + k) \cdot Log2 \qquad \text{(Eq. 2.15)}$$

To take the following sensor parameters, 8-bit $Vramp1$ resolution with N=8, as an example, the resulting DRF achieves 90 dB. This means the total DR can reach as high as 140 dB considering a 50 dB DR in conventional APS readout manner.

The pixel schematic of the WDR concept is illustrated in Fig. 2.31. To increase the well capacity, there is an integration capacitor aside from the photodiode functioning

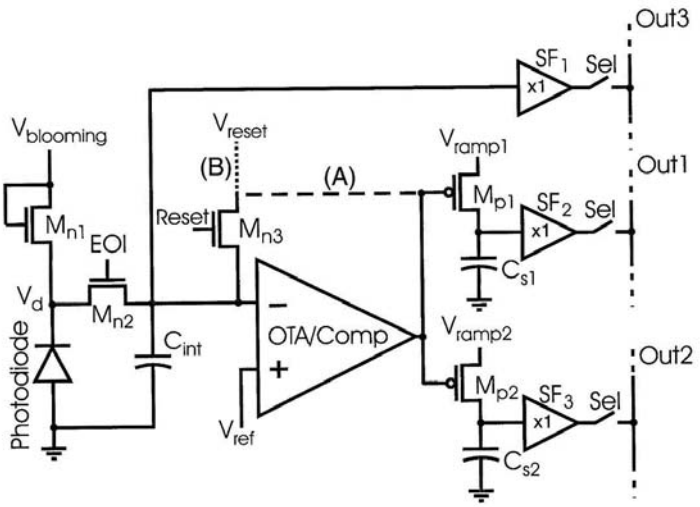


Figure 2.31: Schematic diagram of the HDR pixel circuit, adapted from [9].

as both a sensor node and S/H input of the comparator. The pixel-level comparator is a standard OTA. There are three column buses dedicated to the signal readout. Anti-blooming is provided by the an additional transistor.

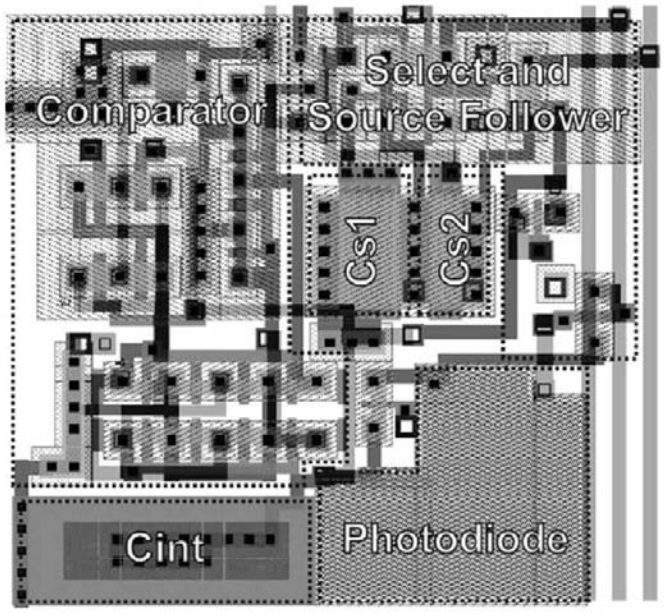


Figure 2.32: Layout of the pixel, adapted from [9].

Fig.2.32 shows layout of the pixel. The pixel pitch amounts to 24.65 μm while the FF is only about 10% due to the large physical occupation of the detection circuits. A large portion of the pixel area is consumed by the capacitors. Together with the area consuming circuits in the pixel, this results in unfavorable large pixel and low FF. This limits its usage in high resolution applications.

2.5.5 Comparison of the WDR Techniques

Four categories of WDR techniques and a variety of WDR solutions in literature have been introduced in the previous section. They differ in pixel and system complexity as well as SNR performance. Simple pixel complexity allows for high resolution imaging but at the cost of lowered SNR. For example, conventional logarithmic pixel has only three transistors, but it suffers large FPN noise, especially at low illumination level. On the other hand, high SNR performance can be achieved at the cost of high pixel complexity and large pixel footprint, for example, saturation detection. Table 2.2 shows the comparison of the WDR techniques in terms of pixel complexity, system complexity and SNR.

Table 2.2: Comparison of the WDR Techniques

	Pixel Complexity	System Complexity	SNR
Logarithmic Pixel	Low; simple three-transistor pixel	Low; inherent nonlinear response	Large noise in low light intensity due to large FPN
Well Capacity Adjustment	Medium; additional in-pixel capacitor	High; to synthesize the image from overflow signals and require frame memory	SNR dip at the switching point
Dual or Multiple Sampling	Low; simple active pixel sensor	High; to synthesize the image from multiple samples and require frame memory and synthesis algorithm	SNR dip when switching the use of the samples
Saturation Detection	High; complex in-pixel saturation detection circuits	Medium; to extract photocurrent from PWM or PFM	High SNR since the signals are captured at saturation level

Chapter 3

Design and Characterization of Radiation-Tolerant Active Pixel Sensors

3.1 Introduction

In order for integrated circuits to operate properly during a long-term space mission, it demands radiation hardness to withstand the harsh radiation environment on the space orbit. This is particularly important for CMOS image sensors since they are one of the most vulnerable devices to radiation effects. They have to be directly exposed to the radiation dose in operation.

This chapter discusses the design and characterization of radiation-tolerant pinned-photodiode 4T active pixel sensors. Based on the various radiation hardening techniques introduced in Chapter 2. Four different pixel variants employing these techniques are proposed. Having the same pixel size, these proposed pixel candidates vary mainly in layout parameters of the photodetector and in-pixel transistors. In a prototype implementation, they are formed in separate pixel arrays to generate characterization data for performance analysis. Experimental and comparison results are reported to evaluate these radiation hardening techniques and sort out a possible guideline to achieve radiation hardness 4T APS. In addition, according to the characterization results, an

improved version of the sensor which utilizes the best of the four candidate designs will be briefly reported. It integrates a larger pixel array for higher resolution and adopts improvement on the readout circuits. The sensor has been integrated into the camera payload in NTU's VELOX-1 satellite mission.

3.2 Radiation-tolerant Pixel Design

4T pinned photodiode APS, composed of four NMOS transistors, suffers the same TID effects as it occurs on other transistors. Our primary design consideration against ionizing radiation concentrates on radiation tolerance of the in-pixel photosensing frontier, which consists of two NMOS transistors, RST and TX, and two charge-sensitive regions, PPD and FD. We have implemented four different pixel designs to evaluate the radiation hardness against TID. As of both RST and TX, we have alternatively implemented ELT on RST and TX in pixels. The radiation hardening on the rest of the pixel, SF and RSL, are not considered, since radiation-induced leakage current present in both transistors is normally several magnitude less than the bias current, and thus negligible. In addition, the geometry parameters of the PPD and FD are also used as design parameter in terms of radiation tolerance. Fig. 3.1 illustrates the layout of the four pixels (Pixel0, Pixel1, Pixel2, Pixel3). Each pixel occupies $6.5 \times 6.5 \mu m^2$. Additionally, Table 3.1 summarizes the device characteristics of all the pixel configurations. Pixel3 is a reference design with no physical enhancement to ionizing radiation. Both RST and TX in Pixel3 are selected to the minimum size allowed by the process design rule. The RST in Pixel0, Pixel1 and Pixel2 are all ELTs. Pixel0 and Pixel1 have the same layout except the size of the FD node. Taking advantage of unequal structure of ELT, Pixel0 connects its pinned photodiode to the inner diffusion of the RST transistor, which results in a relatively small FD parasitic capacitance. On the other hand, Pixel1 uses outer diffusion of the RST transistor for large FD capacitance. The extraction results shows that the

FD capacitance in Pixel1 is over twice of that in Pixel0. In Pixel2, TX is additionally designed to be ELT. Both inner diffusion are used as FD node, which results in the small FD capacitance of 4.23 fF. It is noteworthy to mention that the use of ELT has a limitation of the minimal aspect ratio of the transistor. For example, TX transistor in Pixel2 is approximately 3 times larger than other pixels.

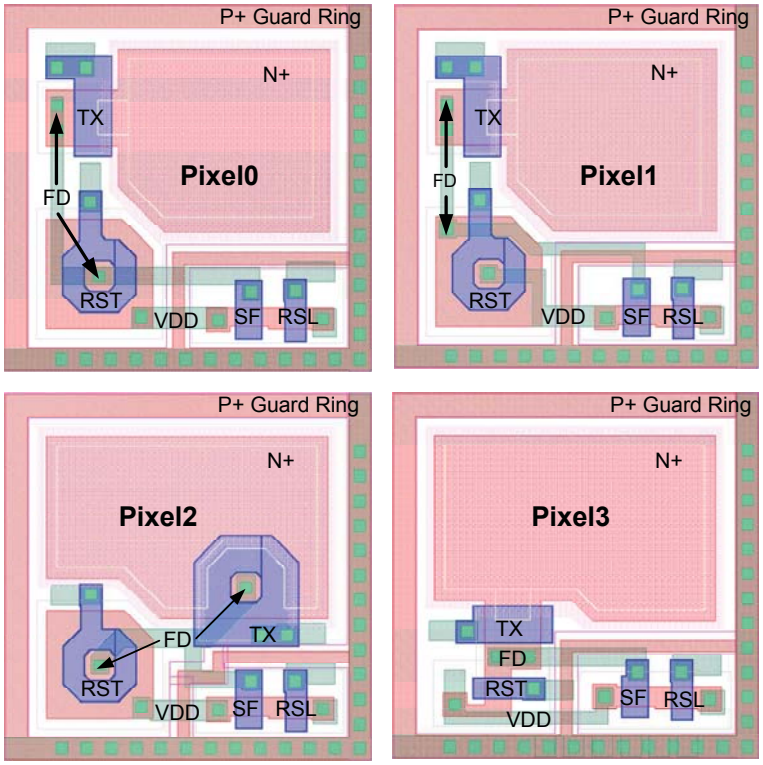


Figure 3.1: Layout of the four different pixel types.

A prototype chip that incorporates four pixel designs has been fabricated using TSMC 0.18 μm CIS process (2-poly 6-metal layers). Fig. 3.2 shows the microphotograph of the fabricated chip. Each pixel design is formed in an array of 256×256 pixels and each pixel array has its own readout circuit. The total chip size costs 5 mm × 5 mm. The chip is characterized before the radiation characterization. The parameter summary of each pixel type is summarized in Tab.3.2. The chip was irradiated by gamma-rays from one to four days at the dose rate of 1.8 krad/hour. The image sensor is not biased during

Table 3.1: Summary of the Pixel Constitutions for Four Pixel Types (Sized in μm)

Type	RST		TX		PD			FD
	Layout	W/L	Layout	W/L	C(fF)	Peri	Area	C(fF)
Pixel0	ELT	3.58 / 0.43	normal	1.06 / 0.70	8.17	13.2	10.45	4.53
Pixel1	ELT	3.58 / 0.43	normal	1.06 / 0.70	8.17	13.2	10.45	9.94
Pixel2	ELT	3.58 / 0.43	ELT	3.31 / 0.77	8.81	17.7	11.34	4.23
Pixel3	normal	0.50 / 0.40	normal	1.06 / 0.70	10.78	16.5	14.54	2.41

Table 3.2: Characterization Summary of Each Pixel Type

Item	Pixel0	Pixel1	Pixel2	Pixel3
Saturation Voltage(V)	1.52	1.42	1.32	1.52
RMS Random Noise($e-$)	60	44	66	84
FPN(%)	0.10	0.10	0.09	0.09
Dark Current(nA/cm^2)	2.37	1.01	5.20	1.56

radiation and it was functional after the irradiation at all the total dose levels up to maximally 170 krad(Si).

3.2.1 FD Leakage

In order to determine the total ionizing radiation effect of edge leakage in both RST and TX transistor, we can evaluate the FD reset voltage. In 4T APS pixel, FD is reset by the RST transistor to VDD and read out immediately after the RST transistor is turned off. However, the voltage on FD can still be changed by both transistors through the radiation-induced edge leakage. Therefore, by evaluating the reset voltage of the FD, one can identify the radiation-induced degradation of both RST transistor and TX transistor.

Fig. 3.3 shows the average reset voltage variation of FD at various ionizing doses. The voltage data are collected in normal pixel readout operation and then averaged within

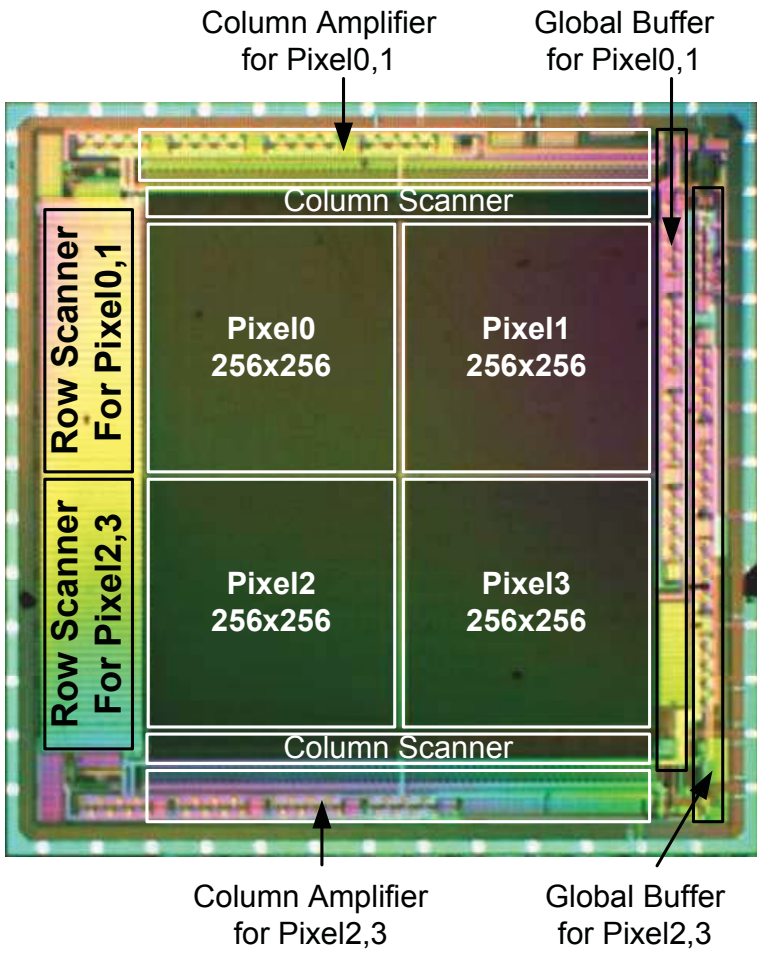


Figure 3.2: The microphotograph of the prototype chip. There are four pixel sub-array on the chip. Main building blocks are highlighted.

the entire pixel array. The variation for all the four pixel types are shown for comparison. All pixel types have shown a slight increase in FD reset voltage with the total ionizing dose at the given dose range. More specifically, Pixel3, the reference design, where no ELT is used on either RST or TX, has shown the positive variation compared with non-radiation condition. It seems to indicate that the FD reset voltage is dominantly changed through the edge leakage current of the RST transistor. On the other hand, pixels with ELT RST transistor (Pixel0, Pixel1 and Pixel2) has demonstrated a negative variation. It can be inferred that the edge leakage in RST transistor is effectively curtailed and the edge leakage in TX has mainly contributed to the voltage variation. ELT TX has further

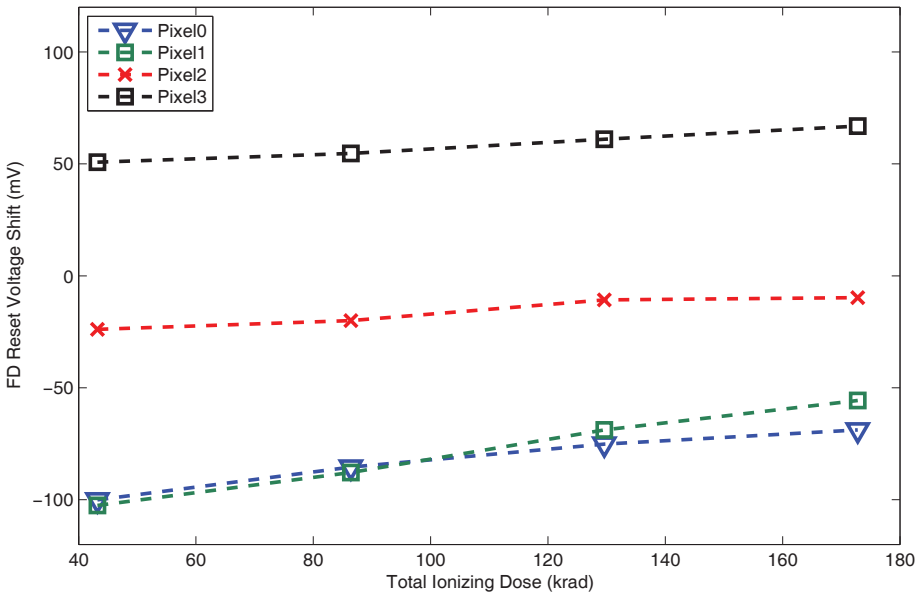


Figure 3.3: FD reset voltage increase as a function of total ionizing radiation dose for four implemented pixel types.

demonstrates its effectiveness on minimizing the voltage variation. Pixel2 with ELT TX has much smaller negative voltage variation (around -25mV) than pixels without ELT TX (Pixel0 and Pixel1).

3.2.2 Dark Current

Ionizing radiation is known to induce large dark current rises in CMOS image sensors. The dark current measurement was done through normal 4T APS readout operation as mentioned earlier by sampling the pixel output voltage at different integration time. The dark current was then obtained by calculating the discharging rate. The average dark current was further calculated by averaging the dark current in the entire pixel array (edge pixels have been excluded). In such APS readout manner, there are several major dark current sources. Firstly, the dark current is generated in the PPD during the the integration. The peripheral of the PPD, i.e. the defective sidewall STI surrounding

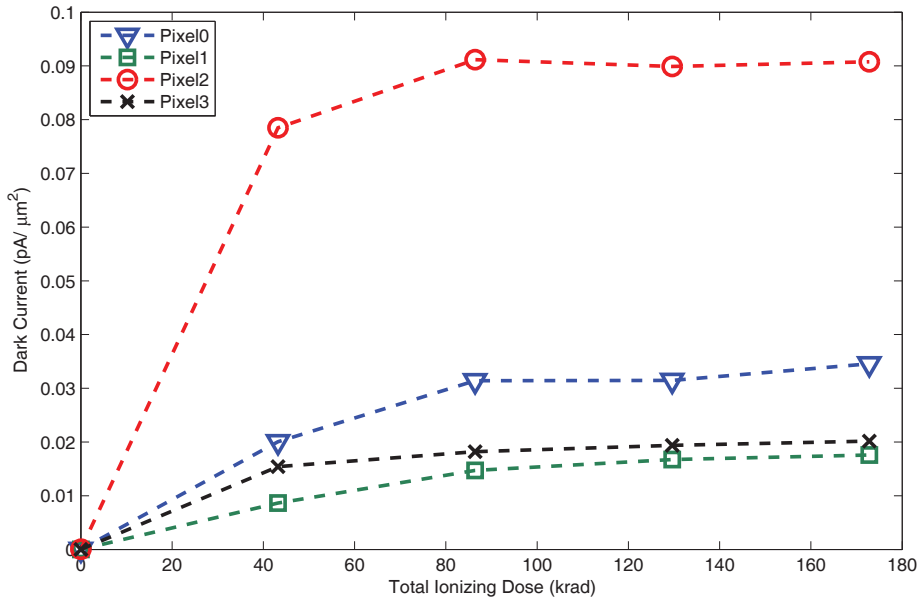


Figure 3.4: Average dark current with regard to total ionizing radiation dose for four implemented pixel configurations.

the photodiode, is the most dominant dark current source in PPD. Secondly, the leakage current through the TX transistor during integration. Thirdly, the dark current generated at the FD node after the transfer of the integrated charges from PPD to FD node during the readout phase.

Fig. 3.4 shows average the dark current increase as a function of total ionizing dose for all the pixel types. For all the pixels, the dark current is fairly low before irradiation thanks to the the optimized CMOS image sensor technology. The thin P+ pinning layer over the PPD utilized in this CIS technology shields it from the surface defects and suppress the noise charges. In addition, P-Well protection and the spacing between the N implant of the PPD and STI are employed to restrict the photodiode junction from interaction with the defective sidewalls and edge. All pixel types exhibit dark current increase. At the tested radiation dose levels, the dark current has shown non-linear increase. To evaluate the FD's contribution of the dark current during the the readout,

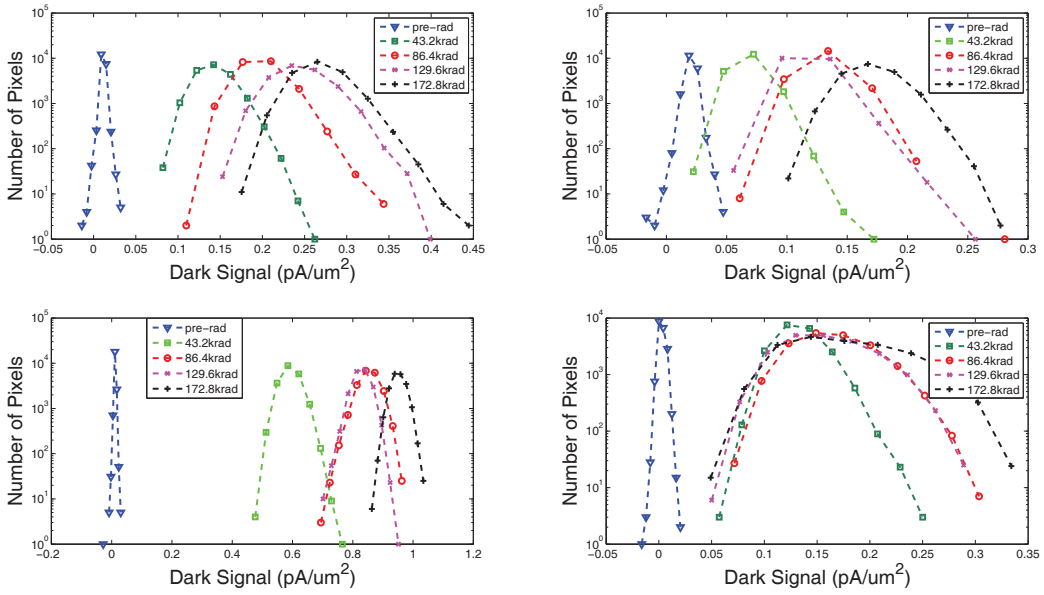


Figure 3.5: Histogram of dark current.

one can compare the dark current of Pixel0 and Pixel1 since they differ only in the FD capacitance. Pixel1 with large FD capacitance demonstrates lower dark current than Pixel0 at all dose levels. Moreover, Pixel0 has the slowest increase rate with the radiation dose. It can be inferred that the pixel with larger FD capacitance is more tolerant to leakage current caused by radiation degradation. Large FD capacitance is supposed to be favorable to radiation tolerant design. Pixel2 with additional ELT TX transistor shows unexpected large dark current increase compared with other counterparts. We expected the ELT TX transistor to curtail the leakage path under STI so as to minimize the radiation-induced edge leakage. However, the TX transistor used in this CMOS technology has a large intrinsic leakage current, which has contributed most of the dark current instead of well-know radiation-induced edge leakage path. To compare it with Pixel0, which is similar to Pixel2 in other device characteristics, the ELT TX transistor has an aspect ratio almost 3 times of the normal TX transistor. It can be inferred that the TX transistor is the region where the most severe degradation happens and the leakage

current increases tremendously under TX transistor during the integration.

3.2.3 Dark Random Noise

Fig .3.6 shows the dark random noise with regard to the radiation dose. The measurement is performed by sampling one pixel in a number of consecutive frames under dark condition and calculate the standard deviation of the these samples. Dark random noise increases after radiation for all pixels is observed. This is because the increased generation of radiation-induced interface states in the transistor [60] [65]. Basically, the phenomenon can happen in all transistors in the pixel. Since SF and RSL are identical design, it is expected that the difference of the dark random noise comes from the TX and RST transistors with associated FD region. TX can generate random noise charges during the charge transfer. As is observed among all pixels, pixel1 has shown the lowest dark random noise and smallest dark random noise increase, this is probably because the

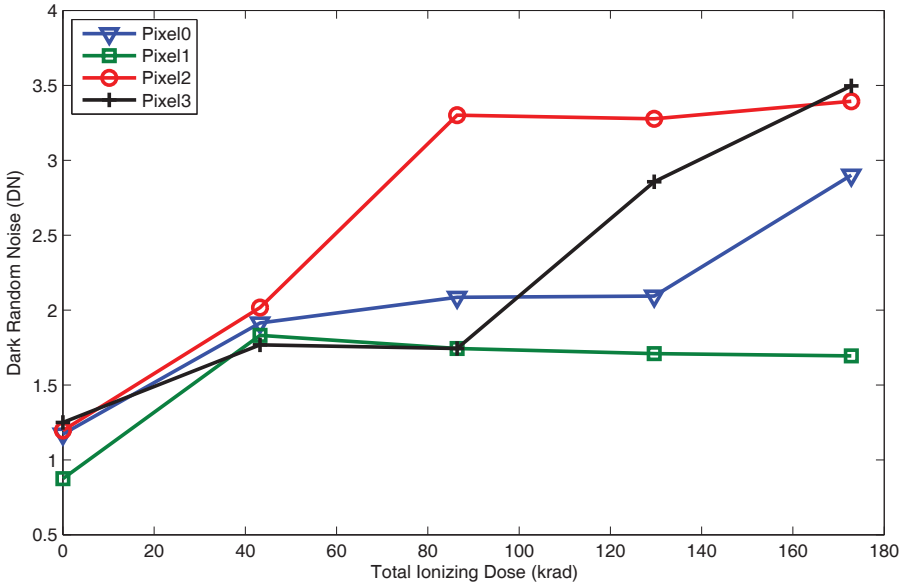


Figure 3.6: Dark random noise (standard deviation value) before and after ionizing radiation for all the pixel types.

largest capacitance at the FD has suppressed the contribution of the randomly-generated charges of these interface traps to the readout signal.

3.2.4 Recessed-STI Photodiode

For DSM technology, The STI is considered to be the prominent mechanism of leakage current, which contributes most of the dark signals in the photodiode region. Recessed-STI pinned photodiode is provided in this CIS technology for the optimization in terms of dark signals. The cross-section detail of the recessed-STI pinned photodiode is illustrated in Fig. 3.7. In recessed-STI photodiode, the pinned photodiode is deliberately spaced from the defective STI-sidewalls. In addition, the pinned photodiode is further protected by the P-well structure. The P-well structure encloses the STI-sidewalls of the photodiode and passivates the STI sidewalls of the photodiode. Since the doping density of the P-Well region is relatively higher than that of N+ doping region of the photodiode, STI is isolated from the depletion region during integration.

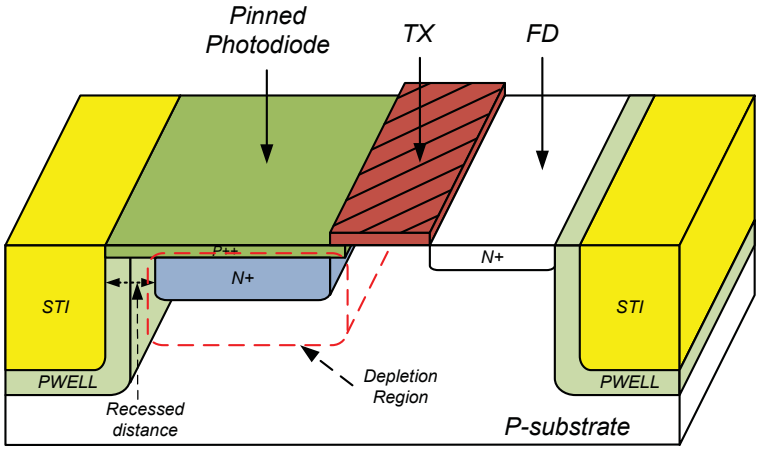


Figure 3.7: Pinned photodiode cross-section details.

In terms of radiation tolerance, we have compared two different recessed distance for Pixel3 so as to investigate the efficiency of the structure against ionizing radiation. The distance of 0.2 μm and 0.3 μm are chosen. Both structures use the P-Well structures and

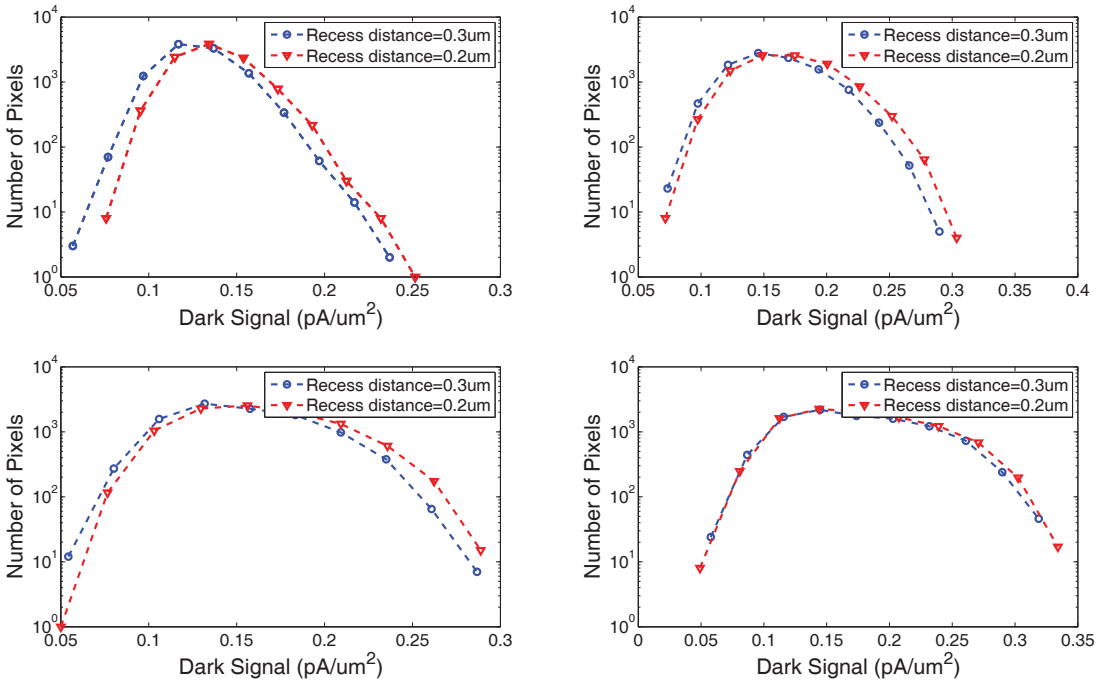


Figure 3.8: Histogram of dark signal regarding recessed distance .

the distance between the P-Well and STI is 0.1 μm. The histogram of the dark signal of both structures are illustrated in Fig. 3.8. Under all the tested radiation level, it is observed that the structure with larger recessed distance (0.3 μm) has lower dark signal than that with closer spacing (0.2 μm). But the difference becomes smaller with increase of the radiation dose. When the radiation dose is high and up to 170krad, The histogram of both structures shows no different distribution. At intense dose, the radiation-induced positive trapped charges seem able to extend the depletion region to the STI interface for both structures, where the interface states and trapped charge densities are high enough to generate dark current.

3.2.5 Summary on Pixel Design

According to our measurement results, TID induces degradation in the FD reset voltage shift and dark current increases. The increase in dark random noise has also been found.

The comparison between our four pixel configurations has suggested that the radiation hardness can be improved by using the ELT RST to curtail the edge leakage current. FD is supposed to hold large capacitance so as to be tolerant to the junction leakage current, which would otherwise give rise to the variation of the signal voltage. Although the ELT TX has suppressed the edge leakage from FD to PPD, the pixel with ELT TX has demonstrated a tremendous dark signal rise compared with other counterparts. Up to 170 krad radiation dose, TX becomes the main degradation mechanism in generating dark signal. The degradation is probably due to the interface traps beneath the TX and the overlapping region between the PPD and TX is a major dark signal source. The large aspect ratio of the ELT TX seems to be responsible for intensive damage. It also seems that the increase is proportional with the aspect ratio. The interface trap generation also plays a role in the increase the dark random noise, which leads to worse spatial non-uniformity in photo response.

The recessed-STI photodiode provides a complex photodiode structure in terms of noise consideration, which will lead to potential radiation tolerance within the photodiode region. The structure tends to recess the N implant of the photodiode against the surrounding STI to avoid the direct interaction between each other. It is further suggested that P-Well protection is inevitable for radiation-tolerant pixel designs as it proves to be useful against STI induced leakage mechanisms. It appears that larger value of the recessed distance results in higher immunity to radiation degradation within the tested dose range. The measurement also gives the hint on the photodiode design at even high dose, that is, to implement even larger recessed distance. However, this is at the cost of sacrifice the size of the photodiode. The effective shrinking photodiode will result in the sacrifice in sensitivity and charge capacity. Therefore, optimization of the spacing is supposed to be made between them.

3.2.6 Other Design Concerns

For digital CMOS circuits used against ionizing radiation, it is safe to use PMOS transistors because of radiation-induced increased threshold voltage. It adds to the noise margin of single event. Though, the negative threshold voltage shift for NMOS transistors is unexpected due to lower noise margin. It has been proved that there is almost no radiation-induced threshold voltage shift with the oxides less than 10 nm in thickness. For current deep submicron technology, the thickness of the gate oxide is usually under 10 nm, and for this technology, the gate thickness is around 6 nm. Therefore, it can be inferred that there is voltage shift tends not to shift much. However, it is still important to pay attention to the noise margin of the CMOS digital circuit when the radiation-induced single event upset becomes the issue. SEE is able to trigger and change the value of the interconnects of the digital circuit and toggle the logic value of the circuit instantly. Especially critical in register, the register may toggle the status due to the SEE, resulting in the timing error and finally the malfunction of the digital controller.

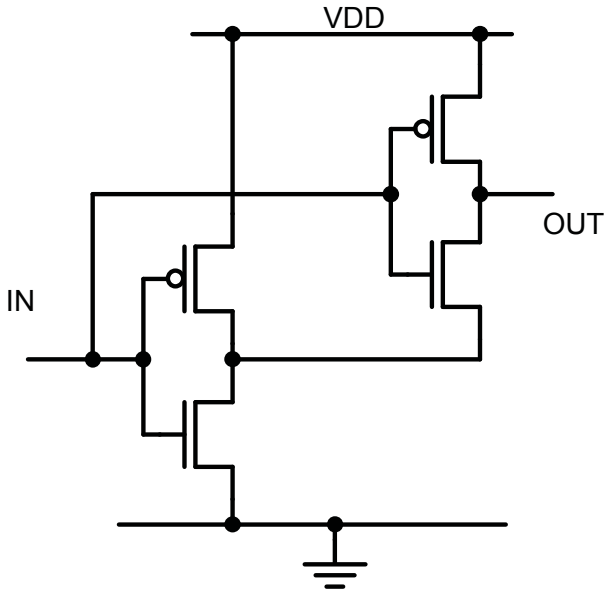


Figure 3.9: Radiation tolerant inverter structure used in D flip-flop.

It is still necessary to deliberately increase the noise margin to make the CMOS digital circuits robust against SEE effect.

As illustrated in Fig. 3.9, the inverter of the modified structure [86] is utilized for all the D flip-flops in the digital controllers. The voltage transfer curve of both the modified inverter and standard inverter is illustrated in Fig. 3.10. The standard inverter toggles at around 1.6V while the modified inverter toggles at around 1.9V. The switching threshold of the modified inverter is lifted as well as the noise margin of the inverter. In addition, Fig. 3.11 and Fig. 3.12 shows the VTC of both inverters under different ionizing radiation dose, respectively. No significant change has been observed, which corresponds well to the conclusion of threshold voltage shift of MOS transistors for deep submicron technology.

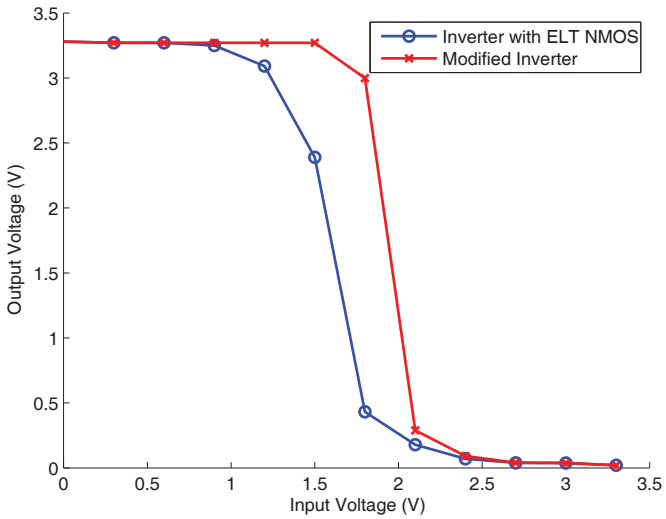


Figure 3.10: Comparison of inverter voltage transfer curve between standard structure with ELT NMOS and the radiation-tolerant modified structure.

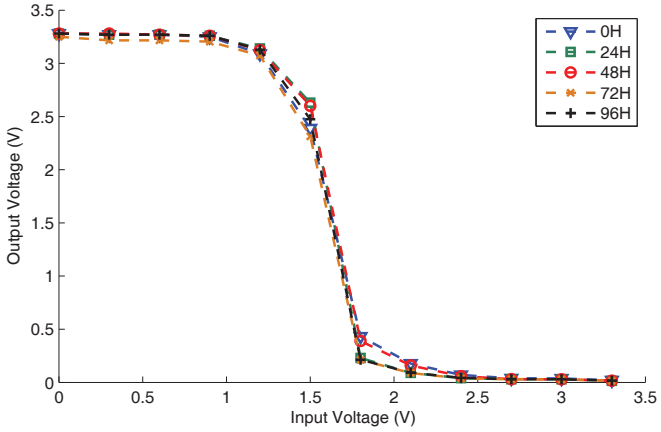


Figure 3.11: Voltage transfer curve of the standard inverter with ELT NMOS under different ionizing radiation dose.

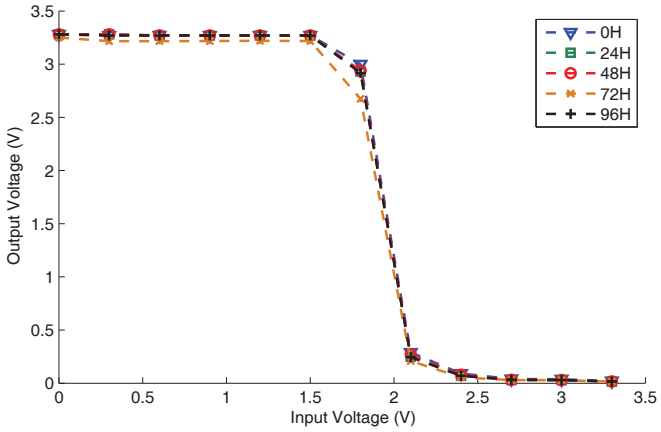


Figure 3.12: Voltage transfer curve of the radiation-tolerant modified inverter under different ionizing radiation dose.

3.3 A Radiation-Tolerant CMOS Image Sensor for VELOX-1 Satellite Mission

Based on the aforementioned characterization results, a radiation-tolerant CMOS image sensor has been developed for the camera payload for NTU's VELOX-1 low earth orbit (LEO) satellite mission. The type of Pixel1 is selected from the four candidates in the prototype chip considering the imaging performance. The pixel pitch remains 6.5 μm

and the resolution of the array is increased to 768×512. The developed sensor has an enhanced readout architecture in terms of noise and readout speed. The camera system is developed for the purpose of earth imaging. The optical system has a focal length of 25 cm to ensure a achievable ground resolution of about 20 m.

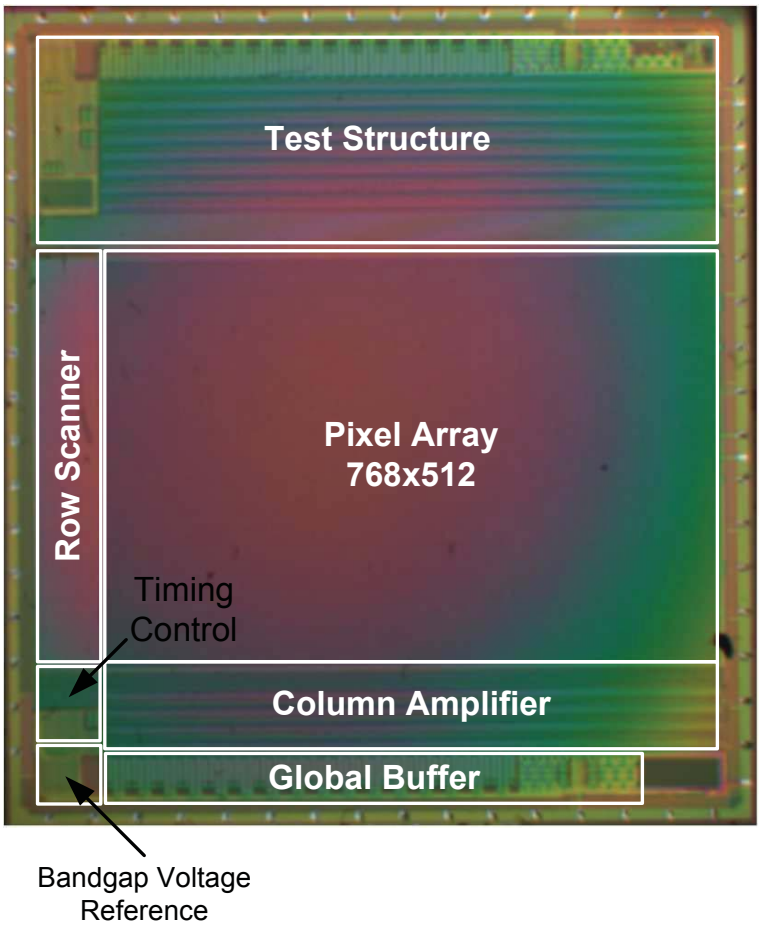


Figure 3.13: Chip microphotograph of the radiation-tolerant CMOS image sensor.

The sensor was implemented using the same TSMC 0.18 μm CIS process as the prototype chip. Fig.3.13 shows the microphotograph of the sensor. The chip size costs 6 mm × 6.8 mm, in which the core of sensor occupies 6 mm × 5 mm in area. The sensor runs at 40 MHz, and correspondingly can achieve 100 fps. Some sample raw images taken by the sensor, as shown in Fig. 3.14, prove the successful operation. The pixel remains

the same size as in the prototype. The comparison of the prototype chip and this sensor is summarized in Tab. 3.3.

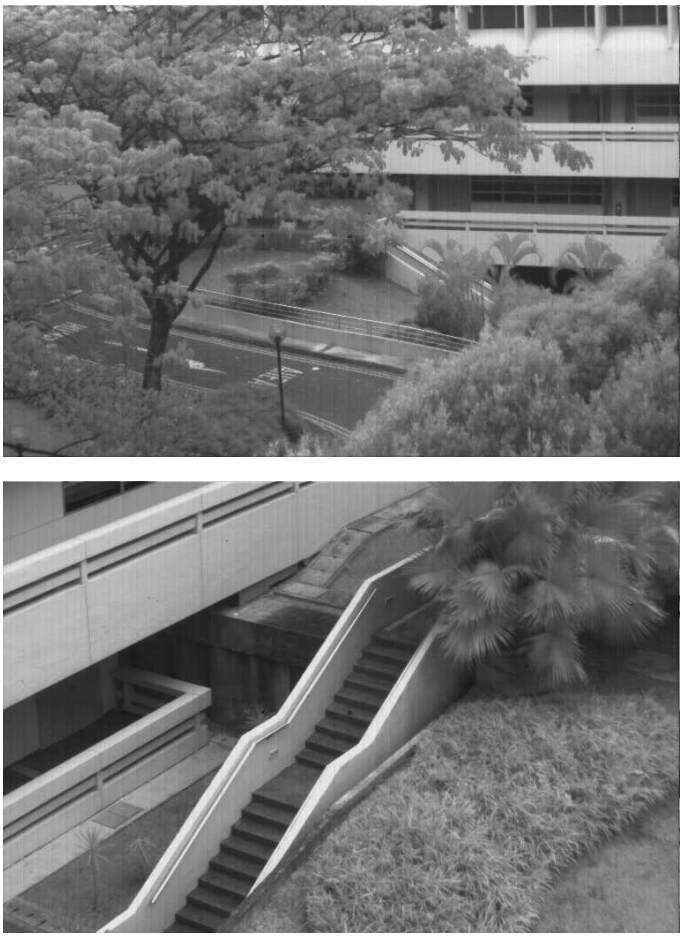


Figure 3.14: Sample raw images taken by the sensor.

3.4 Conclusion

In this chapter, design and characterization of a radiation-tolerant CMOS image sensor were described. Four types of pixel layout based on 4T APS were proposed and analyzed. They vary in a number of pixel parameters of and employ various radiation hardening techniques selectively. A test chip carrying these four pixels, each formed in a small array,

Table 3.3: Main Feature Comparison of Both Image Sensors

Senor	VELOS-1 Camera Payload	Prototype
Technology	TSMC 018CIS	TSMC 018CIS
Pixel Type	4T Pinned Photodiode APS	4T Pinned Photodiode APS
Pixel Size	$6.5\mu m \times 6.5\mu m$	$6.5\mu m \times 6.5\mu m$
Pixel Array Size	768×512	$256 \times 256 \times 4$(array)
Imaging Area	5 mm × 3.4 mm	3.4 mm × 3.4 mm
Power Supply	3.3 V	3.3 V
Clock Frequency	40 MHz	60 MHz
Output	Analog	Analog
Die Size	6 mm × 6.8 mm	5 mm × 5 mm
Number of I/O Pads	64	42

was implemented, radiated and characterized. According to the test results, TID induces degradation in the reset voltage shift and dark current increases. The increase in dark random noise has also been found. It has been found that the radiation hardness can be improved by using the ELT RST to curtail the edge leakage current. FD node is supposed to hold large capacitance so as to be tolerant to the junction leakage current. Although the ELT TX aims at reducing the edge leakage, the pixel with ELT TX has shown a tremendous dark current increase compared with other counterparts. TX becomes the dominant degradation mechanism in terms of dark current.

According to the characterization results, the best pixel candidate of the four is selected for the CMOS image sensor developed for the NTU's VELOX-1 LEO satellite. The sensor was briefly introduced.

Chapter 4

Novel Wide Dynamic Range Architectures for Star Sensors

4.1 Introduction

Dynamic range is a critical measure of performance for a star sensor to produce useful images of planets, asteroids to stars which are then used for star centroiding. Stars have a very wide span of brightness. They range over six apparent magnitudes. There are even worst scenarios in space, where there are extremely bright celestial objects. This demands a sensor to provide very high dynamic range to detect stars correctly. Conventional active pixel sensor only provides limited dynamic range and does not directly suit the need of a star sensor. They can cover only a portion of them, which affects the overall accuracy.

In this chapter, two new high dynamic range architectures of CMOS image sensors are proposed. The first architecture rooted from the time-domain concept of "saturation detection" is presented. Its operation principle, simulation results as well as experimental results will be presented. In the second proposed architecture, the pixel incorporating a dual exposure charge subtraction scheme for high dynamic range is presented . The pixel also takes advantage of a capacitive transimpedance amplifier, which combines the high sensitivity and high dynamic range together. The design consideration will be described and the concept is proved by the chip fabrication and measurement results.

4.2 An Adaptive Integration Time CMOS Image Sensor with Multiple Readout Channels

4.2.1 Overview

Among various techniques for WDR CMOS image sensors, the scheme of "saturation detection" encodes the incident light intensity in the form of temporal information. Incorporating the dimension of time as a system variable, this type of sensor is thus called time-domain sensors or pulse modulation (PM) sensors. Time-domain sensors shift the DR constraints in voltage domain due to limited power supply rails, so that they can achieve very wide range of illumination. There have been reported time-domain image sensors with DR on the order of 100-140 dB [85] [8]. In addition, SNR also benefits since each pixel reaches the saturation level in every integration cycle. Hence, the achievable SNR is essentially independent of the photocurrent.

However, time-domain pixel demands complicated silicon implementation and requires large silicon areas for pixel-level circuits including comparison circuits and memory functionalities to detect and store the temporal information. For instance, two large capacitors are used in [9] as analog memories to encode the time information. In general, this type of pixel has large pixel footprint and low fill factor, which limits the use in high resolution imaging applications.

In this section, a new wide dynamic range architecture for CMOS image sensor architecture is proposed. It allows for adaptive integration time by saturation detection but avoid the use of complex pixel circuitry. This is achieved by cyclically checking the integration voltage of pixels in a row-wise manner throughout the integration time. In this case, bright pixels can be "marked" and read out first. Those dimmer pixels will continue integration until their voltages fall into a window defined by two threshold references. Each pixel consists of only five transistor. The pixel size and its fill factor is comparable to that of an APS. In order to improve the readout throughput, a scheme of multiple

readout channel is proposed accordingly. A MATLAB program is developed in order to simulate the validity and effectiveness of the proposed architecture. Experimental results also show the successful operation of the proof-of-concept implementation.

4.2.2 Operation Principle

The proposed architecture features column-parallel comparison circuits to decide whether a pixel should stop its integration or not. Fig. 4.1 illustrates the operation principle with an example of a 3×3 pixel array.

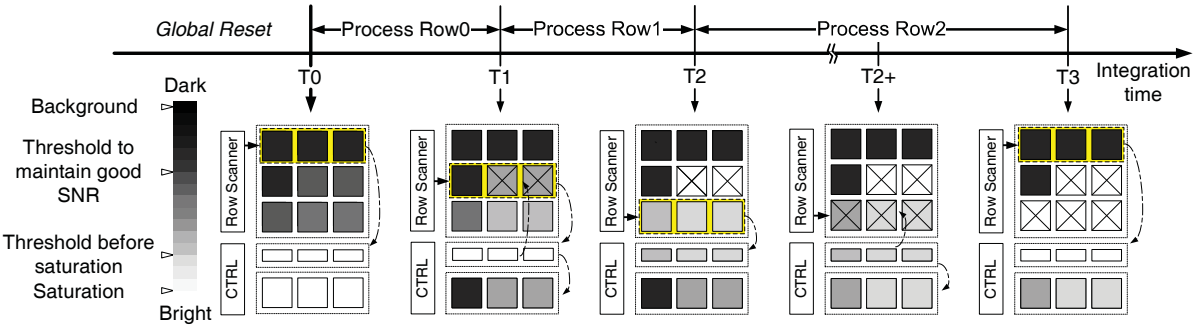


Figure 4.1: Operation principle of the adaptive-integration-time readout scheme.

Initially, the sensor is globally reset and all the pixels start integration. Immediately followed by the reset operation, a row-wise scanner starts rolling. At $T0$, $Row0$ is selected and all the pixels in $Row0$ are simultaneously sampled onto the column-parallel comparison circuits. In this example and at this moment, no pixel has gathered enough photons and therefore none of the pixel's voltage falls into the threshold window. Next at time $T1$, $Row1$ is sampled and checked in the same manner. There are two bright pixels ($Col1$, $Col2$) and their voltage is within the threshold. This will enable the readout process and the whole $Row1$ is assigned to a readout channel. In the meanwhile, the column circuits will raise a flag signal to "mark-off" the two bright pixels. In this way, these two pixels will be ignored in the future checking process. The readout channel takes two clock cycles to readout the active pixels in $Row1$. Instead of waiting for the

completion of readout, the sensor continues to check $Row2$ immediately after channel assignment. A pipeline mechanism has been proposed so that the voltage checking and readout can work in parallel. In the case that all readout channels are occupied, at time $T3$ for example, the row-wise scanner will pause until at least one channel is free. For a particular row, the readout time is proportional to the number of "active" pixels. This is implemented by a scanner with bypass control. When the row scanner hits the last row, it will loop back to the first row to scan another round.

4.2.3 Sensor Architecture

The architecture of the proposed image sensor is shown in Fig. 4.2. It includes a 320×128 pixel array, column-parallel comparison circuits, multiple (three) readout channels, a row scanner, a channel assignment controller and a global timer.

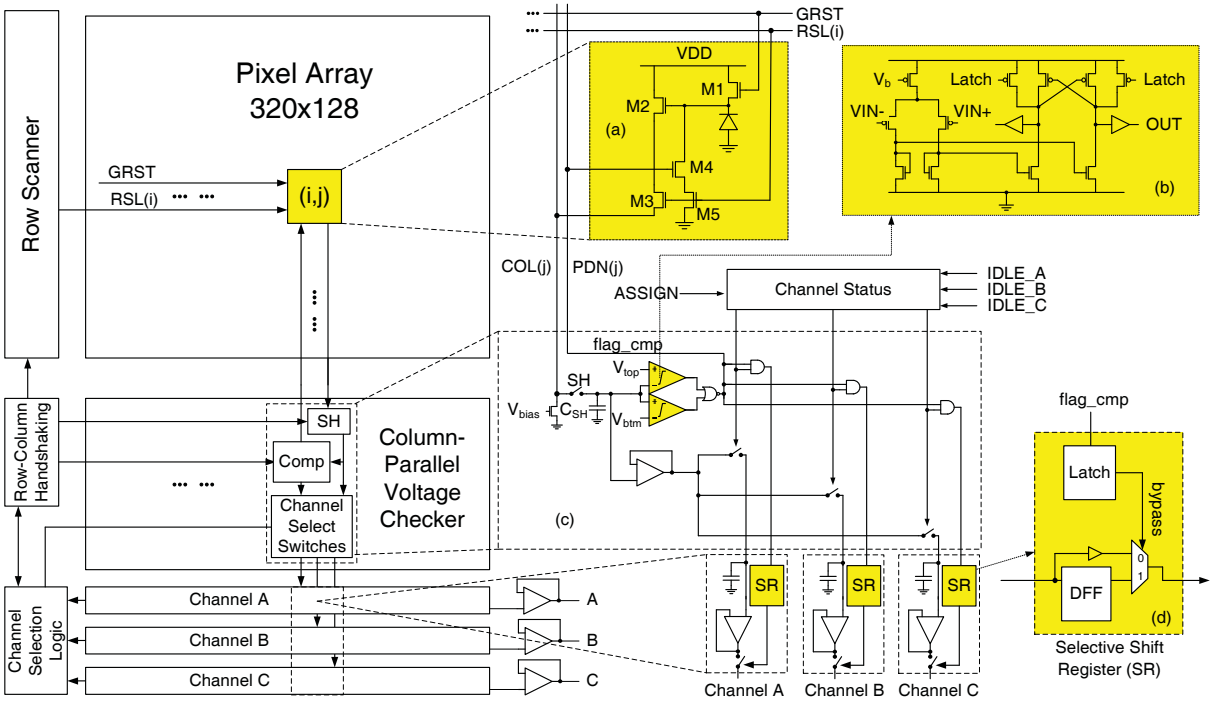


Figure 4.2: Sensor architecture. Main building blocks include a pixel array, column-parallel comparison circuits, three readout channels, row scanner and channel assignment controller.

The pixel array is globally reset by $GRST$. As can be seen from Fig. 4.2 (a), each pixel consists of five NMOS transistors. $M1 - M3$ forms a typical APS. Two extra transistors $M4 - M5$ form a pull-down path for the photodiode. As such, the photodiode can be pulled down to its saturation level by external control signal. The column-parallel comparison circuits reside at the bottom of the pixel array and communicate with the pixel through two vertical buses, COL(j) and PDN(j). The column-parallel comparison circuits is composed of a SH circuit block, comparison circuits and a group of channel select switches. The comparator, as shown in Fig. 4.2 (b), is a static-latched type with pre-amplifier stage [87] [88]. The regeneration node is decoupled by two current mirrors for low kickback noise. In each readout channel, the scan register can be configured to bypass a certain column depending on the comparison result. The channel selection logic allows to decide which channel can be used to read out a selected row.

4.2.3.1 Analog Path

Fig. 4.3 highlights the analog path from the pixel to the readout channel and Fig.4.4 shows the corresponding timing diagram of the sensor operation, respectively.

Two stages of sample-and-hold circuits are required for the pixel voltage to transfer to the analog global buffer. During the cycles when row select signal RSL(i) is ON, the pixel voltage is first sampled-and-held onto C_{SH} within one and half cycles. In order to minimize the sampling error caused by the critical channel charge injection, the single SH transistor switch is replaced by four identical NMOS transistors to suppress the charge injection onto C_{SH}. Followed by the SH operation, ASSIGN switch will be turned on to transfer the pixel voltage on C_{SH} to the corresponding local sample-and-hold capacitor C_{CH} in the channel once a channel becomes "IDLE". The design of ASSIGN switch is the same of the SH switch to minimize the effect of channel charge injection. The analog buffer to drive the next stage is a seven-transistor two-stage operational amplifier. Since

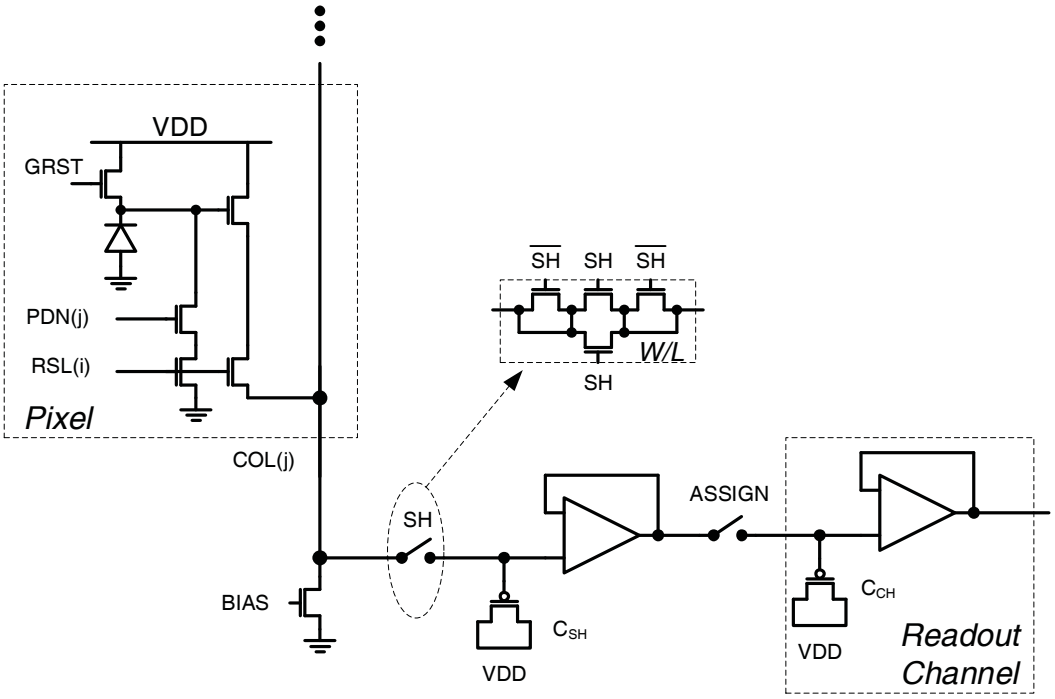


Figure 4.3: Analog signal path from the pixel to a readout channel.

the pixel voltage after the source follower stays at the lower range of the power supply, both C_{SH} and C_{CH} are designed to be PMOS capacitors. Consideration has also been taken to design the size of both capacitors. As in the scenarios when RSL(i+1) is ON, all channels are busy after SH, the sampled pixel voltage on C_{SH} must hold until it is allowed to transfer to C_{CH}. Due to the leakage current across the capacitor, this long delay can cause the voltage on C_{SH} to drop from its expected value. The worst-case delay is approximately 320 clock cycles when all channels are just occupied by other rows. For C_{CH} in the readout channel, on the other hand, the worst case to withstand the leakage current is the one in the last column, which must hold the voltage until all previous columns are readout. This also amounts approximately to 320 clock cycles. Both C_{SH} and C_{CH} are designed to be 6μm $\times$ 2.8μm large and approximately 135fF according to the simulation results. This limits the voltage drop due to leakage current on the capacitor as low as within 0.5LSB after 32us at 10MHz clock frequency.

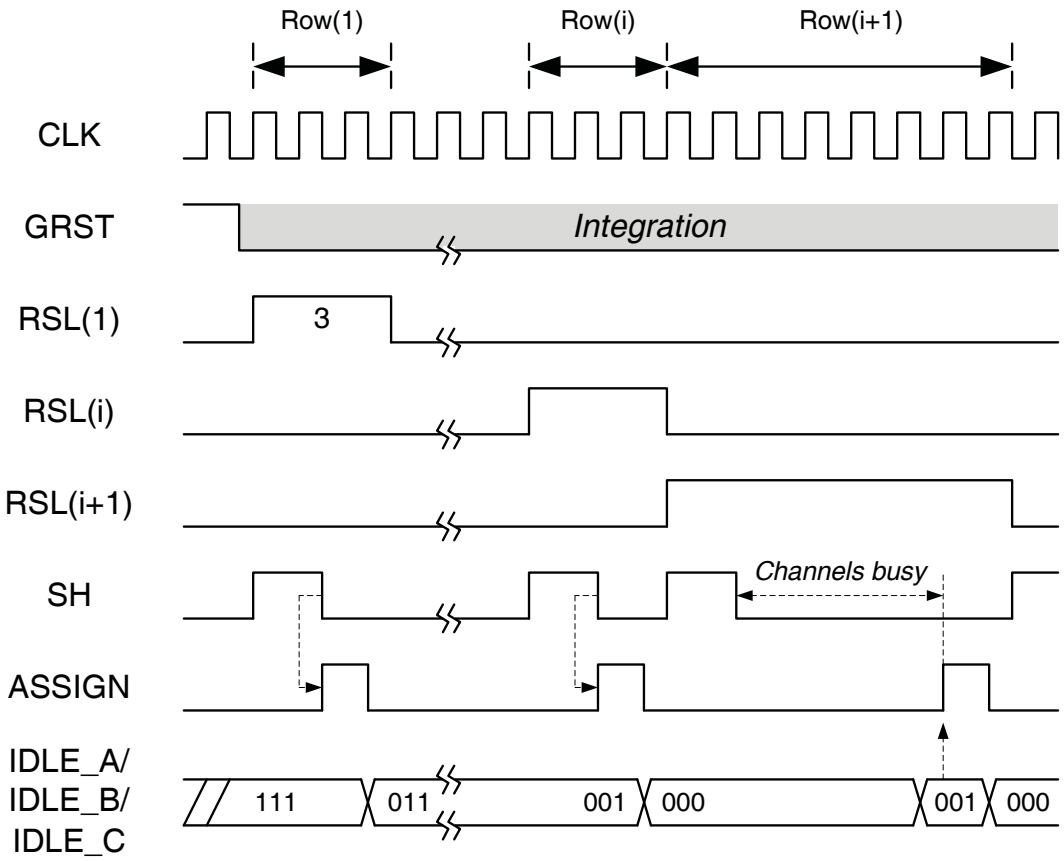


Figure 4.4: Timing diagram of the sensor operation.

4.2.3.2 Readout Channel and Channel Assignment Logic

The sampled pixel voltage on capacitor C_{SH} is compared to two threshold voltages namely V_{top} and V_{bottom}, respectively. The comparison result, $flag_{cmp}$, is fed back to the array and the pixel is "marked-off" by pulling down the diode voltage using transistor $M4$. At the same time, $flag_{cmp}$ is also stored into a latch and further used as a bypass control in the readout channel. Fig .4.5(a), (b) and (c) show the architecture of one readout channel, architecture of a shift register in the configurable column scanner and timing diagram of the column scanning, respectively.

Each channel has a flag register, $IDLE_{CH}$, indicating whether is busy in column scanning. The channel select pulse, SEL_{CH} is generated from channel assignment logic

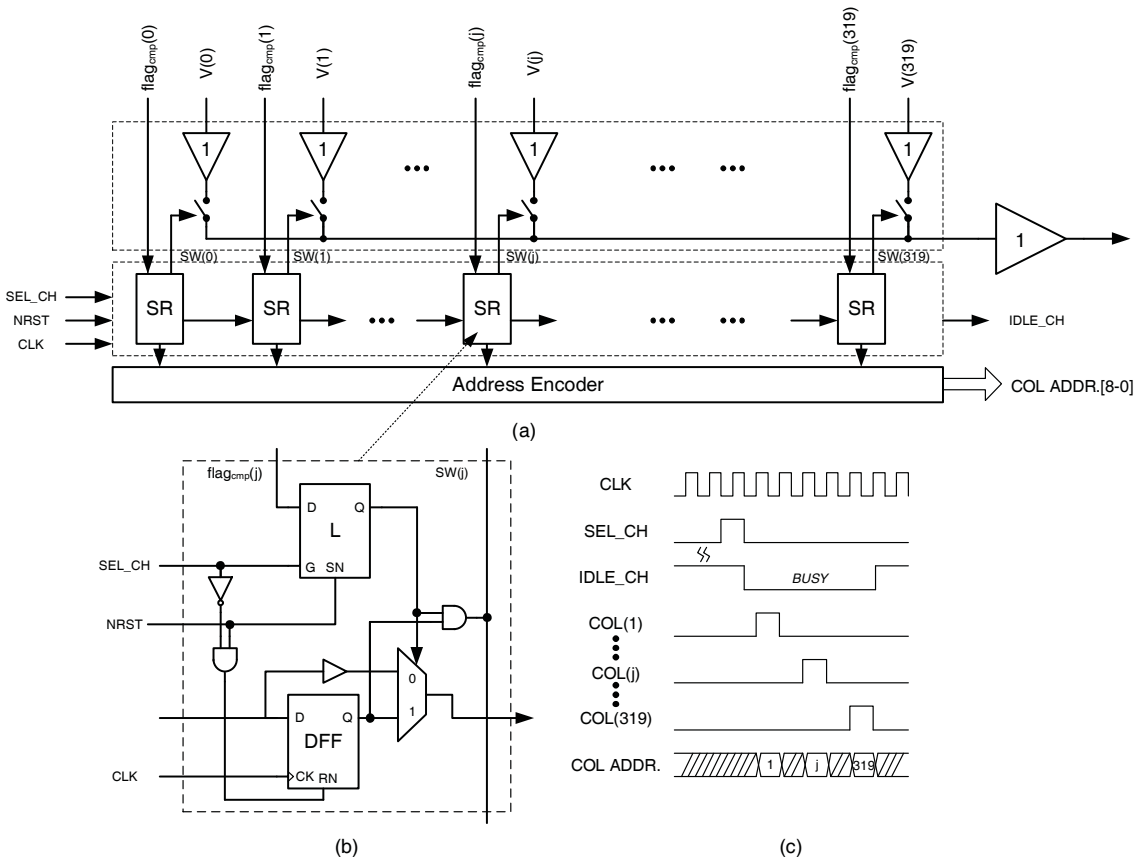


Figure 4.5: The architecture of the readout channel.

when $IDLE_{CH} = 1$. Once SEL_{CH} is ON, it latches $flag_{cmp}$ and configures the data path in the shift register. The column scanning starts right after the configuration and $IDLE_{CH}$ is pulled down accordingly. It skips those columns with $flag_{cmp} = 0$ and the scanning length depends on the number of "active" pixels in the row. Therefore, a row with less "active" pixels will take much shorter readout time.

Our architecture builds three readout channels, which are managed by a channel assignment logic as shown in Fig. 4.6. Each channel has a flag register indicating the status of "BUSY" or "IDLE". The assignment logic uses a simple priority rule to manage the three channels. Channel A has the highest priority and Channel C will only be used when both Channel A and B are unavailable. Once a channel is identified as "IDLE", the assignment switches will be turned on and the analog voltage will be transferred from

capacitor C_{SH} to the corresponding local sample-and-hold capacitor in the channel. The simple logic operation is easy to expand to any number of readout channels.

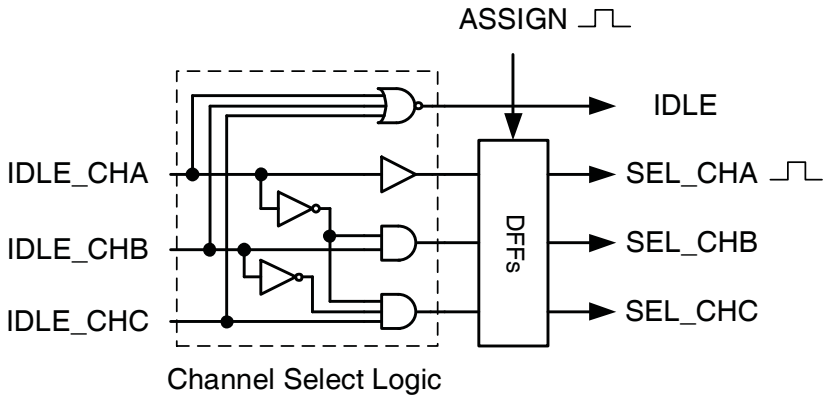


Figure 4.6: Channel select and assignment logic.

4.2.3.3 Image Reconstruction

With this scheme, pixels with different illumination level will have their own integration time. The principle is further illustrated in Fig.4.7. $PixelA$ experiences a sharper discharge slope due to a larger photocurrent. $PixelB$ shows a moderate photocurrent while $PixelC$ is apparently under dark condition. We can set a maximum allowable integration time and those pixels ($PixelC$, for example) that fail to reach the readout window will be considered as dark pixels. The sensor outputs both analog voltage and the time stamp when the voltage is sampled. Both the time (t_s) and voltage (V_s) information are used to reconstruct the picture:

$$I_{ph} = \frac{C_{int} \cdot (V_{rst} - V_s)}{t_s} \qquad \text{(Eq. 4.1)}$$

where I_{ph} is the pixel's photocurrent and C_{int} is the photodiode capacitance.

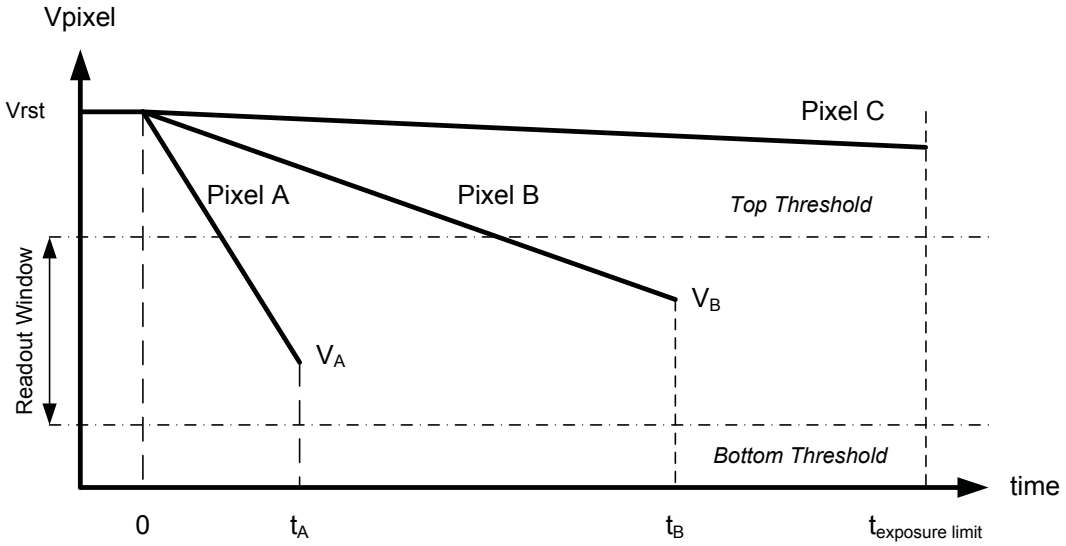


Figure 4.7: Illustration of different pixels' responses. Pixels with different illumination level will have its own integration time.

4.2.3.4 Dynamic Range

Dynamic range of the sensor architecture is given by the following expression:

$$DR = 20\log\frac{I_{\max}}{I_{\min}} = 20\log\frac{C_{\text{int}}\,(V_{rst} - V_{btm})/t_{\min}}{C_{\text{int}}\,(V_{rst} - V_{top})/t_{\max}} \qquad \text{(Eq. 4.2)}$$

where I_{max} and I_{min} are the maximum and minimum photocurrents that can be detected in the pixel, respectively. C_{int} is the photodiode capacitance, V_{rst} is the pixel reset voltage, V_{btm} is the bottom threshold and V_{top} is the top threshold, respectively. $t_{\max}$ is the longest integration time, which is the exposure time limit. $t_{\min}$ is the shortest integration time, which is integration time for a certain pixel in the first-round voltage checking. $t_{\min}$ can be regarded as the waiting time for a pixel to be processed due to row-wise scanning. The minimum of this waiting time is one and half cycles for the first row of pixels since their voltages are checked immediately after reset.

If the sensor operates at 10MHz, that is, 100ns per clock cycle, $t_{\min}$ is then 150ns. $t_{\max}$ is assumed to be 300ms. Also given that V_{rst}, V_{top} and V_{btm} are set to 1V, 0.8V and 0.2V, respectively, DR of 138dB is expected.

4.2.4 Simulation Results

In order to simulate the sensor architecture proposed in this paper, we developed a MATLAB-based simulator. The MATLAB program simulates the operation principle including photo-detection, row-wise scanning, column-wise comparison readout channel assignment with corresponding timing. A 12-bit (ranging 0-4095) grayscale image with 320×128 pixels is first translated into a photocurrent array in terms of digital numbers(DN). The photocurrent array is used as the input of the simulator. For column-parallel voltage comparison, both top threshold and bottom threshold that form the readout window are user variables so that one can evaluate this design parameter as will be explained later. According to the proposed sensor operation, there are three readout channels used in simulation. The pixel values across the array are updated in each cycle. The timing of comparison operation is set to two cycles and the assignment lasts for one cycle before the row scanner switches to the next row. Throughout the integration, those pixels that have been readout are marked as one while zero for those that miss the readout. The reconstructed image is obtained by multiplying the marked results with the original image. Therefore, those pixels that miss the readout become "black" pixels in the final output.

Fig. 4.8 shows the simulation results of a Lena image. In the first group, as shown in (a)-(d), top threshold is set to 3500 and bottom threshold are 1500, 2500, 3000 and 3300, respectively. Second group, (e)-(h), configures the top threshold to 3000 and bottom thresholds are 1000, 2000, 2500, 2800, respectively. Last group, (i)-(l), configures top threshold to 2500 and bottom thresholds are 500, 1000, 2000 and 2300, respectively. Each group thus forms a readout window of 2000, 1000, 500 and 200, respectively. As can be seen from the comparison, one can clearly observes the "black" pixels exist increasingly across the pixel array with the shrinkage of the readout window. These "black" pixels not only exist in the dark region of the original image, but also occupy a large portion

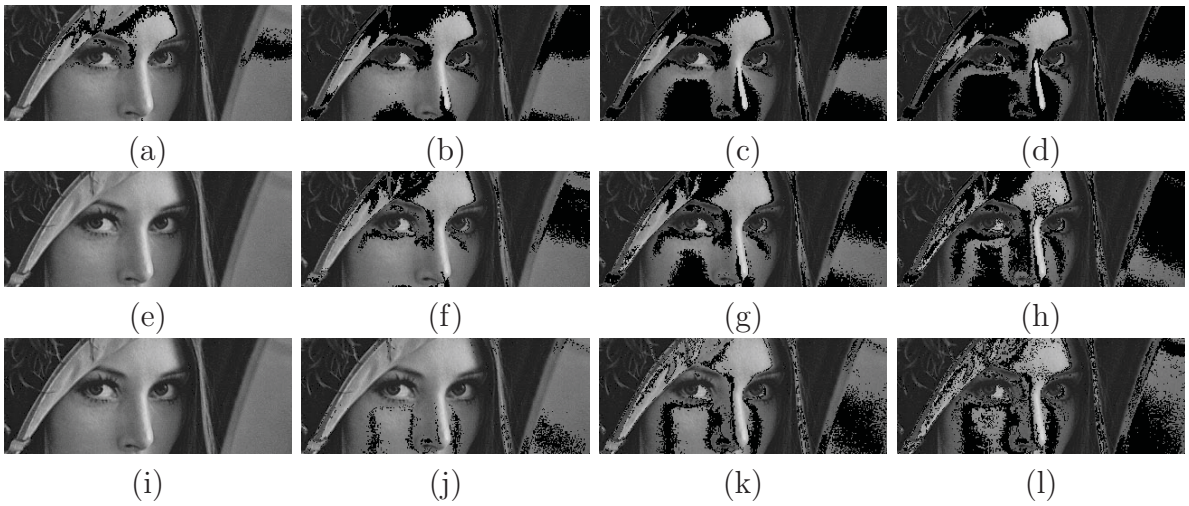


Figure 4.8: Simulation results for a 320×128 Lena image under sensor operation. In(a)-(d), top threshold is set to 3500 and bottom threshold are 1500, 2500, 3000 and 3300, respectively. In(e)-(h), top threshold is set to 3000 and bottom threshold are 1000, 2000, 2500, 2800, respectively. In(i)-(l), top threshold is set to 2500 and bottom threshold are 500, 1000, 2000 and 2300, respectively.

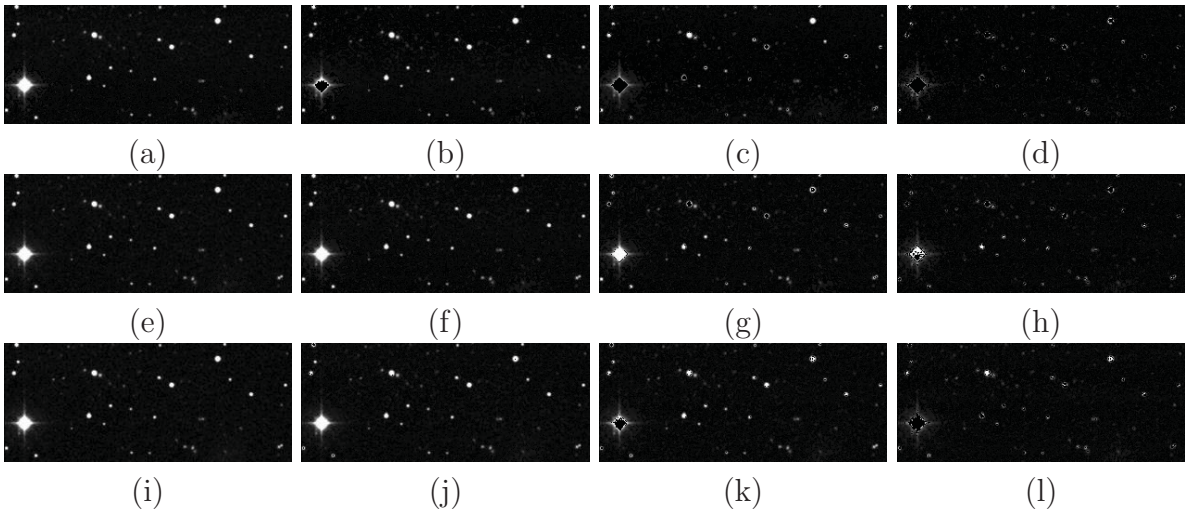


Figure 4.9: Simulation results for a 320×128 star field image under sensor operation. In(a)-(d), top threshold is set to 3500 and bottom threshold are 1500, 2500, 3000 and 3300, respectively. In(e)-(h), top threshold is set to 3000 and bottom threshold are 1000, 2000, 2500, 2800, respectively. In(i)-(l), top threshold is set to 2500 and bottom threshold are 500, 1000, 2000 and 2300, respectively.

of the bright regions. These bright regions across the pixel array are likely to have similar photocurrent magnitude. Therefore if a large portion of these pixels require to be processed, it requires a large amount of time to finish before it proceeds to another region. During this time, other bright regions are still integrating and their pixel values are likely to fall below the readout window and therefore regarded as "black" pixels. Generally, the bottom threshold is set slightly above the saturation level to maximize the readout window. When comparing between groups with the same readout window size and different top threshold, one can find that these "black" regions generally shift. Top threshold determines the time for a pixel to fall into the readout window. The higher the top threshold, the earlier the pixel will trigger the readout process. The actual readout sequence is accordingly changed as well. In general, the readout window should be set as wide as possible to increase the number of readouts. But the readout of a scene is still limited by a number of other parameters, for example, actual photocurrent size, pixel array size and readout bandwidth. As discussed earlier, if there are large regions with similar illumination level in the array, it can cause pixels in other regions to saturate before they can be handled. One can imagine of the worst-case of a uniform photocurrent array, where a complete row will be processed before it switches to the next. It will occupy the readout channel for long so as to cause other rows to saturate. On the other hand, if the imaging scene has a sparse distribution of similar illumination levels, for example, a star field, one can take advantages of this dynamic readout scheme. Fig. 4.9 shows the simulation results of a star field image with the same parameter settings as the previous example. Stars are the regions of interest and has a sparse distribution of similar illumination levels. Although, some very bright stars saturate when the readout window is small, but they are all captured when the readout window becomes wide. And also due to wide distribution of the dark background in such a star field scene, most of the missing readouts are composed of these pixels, which is not of primary concern. Fig. 4.10

(a) and (b) show the readout percentage of the Lena image and star image, respectively. Due to the wide distribution of dark background, the overall statistic readout percentage of a star image (below 92%) happens to be smaller than that of Lena's for the same parameter settings. Nonetheless, from the image reconstruction, the stars are completely captured in all simulated scenarios.

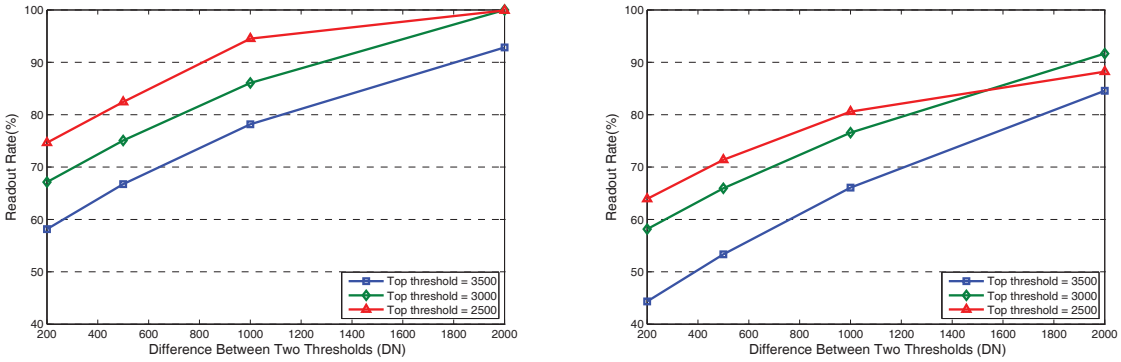


Figure 4.10: Readout percentage of the (a) Lena and (b) star image.

4.2.5 Implementation and Measurement Results

The proposed image sensor has been fabricated in Global Foundries 0.18 μm 1P6M CMOS technology. Fig. 4.11 shows the chip microphotograph where the main building blocks are highlighted. The overall chip dimension is 2.5 $\times$ 2.5 mm^2. The array contains 320 $\times$ 128 pixels. Each pixel features a footprint of 5 $\times 5 \mu m^2$ with a fill-factor of 38%. The column-wise comparators with programmable threshold voltages are placed at the bottom of the pixel array. The chip has three readout channels. Each channel outputs signal pairs consisting analog signal, time and column address. The row address is generated off-chip due to the sequential nature of the row scanner.

The sensor was interfaced with an Opal-Kelly XEM 3010 FPGA board. The FPGA acquires the output signals for each channel and temporarily store them on the on-board

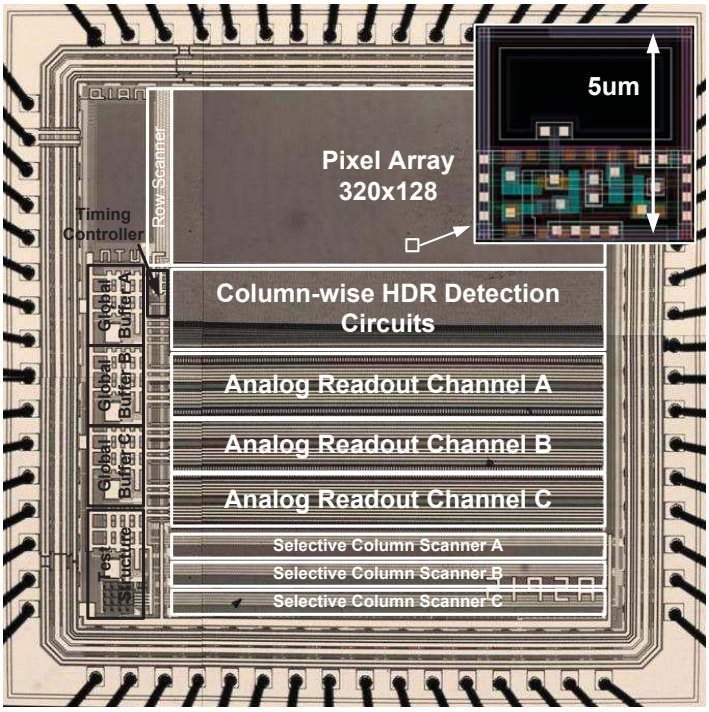


Figure 4.11: Chip microphotograph.

RAM. In addition, the FPGA also provide input control signals and communicate with a host PC through a USB link. The post-processing of the captured data and image reconstruction is conducted on PC. During sensor characterization, we have observed that the chosen process shows poor light response within the tested range up to 18klux. The average dark current is measured at 1537fA for a N+/P-sub photodiode with an area of 4.26μm $\times$ 2.28μm. The sensor has a readout speed of 10 MHz and consumes 247 mW power. The sensor parameters and characterization details are listed in Table 4.1.

Fig. 4.12 shows the relation between the incident light intensity and reconstructed photocurrent. The incident illumination varies from 0.1 lux to approximately 200 klux, which is uniformly exposed to the pixel array. The voltage of the pixel is firstly measured and photocurrent is then extrapolated using Eq. 4.1. The plotted results have offset the dark current. When the illumination approaches about 200 klux, the pixel in the first

Table 4.1: Performance Summary of the Sensor

Technology	Global Foundry 0.18μm mixed-signal CMOS
Die Dimensions	2.5mm × 2.5mm
Supply Voltage	1.8V
Clock Frequency	10MHz
Power Consumption	247mW
Pixel Array Size	320(H) × 128(V)
Photodetector Type	N+/P-sub photodiode
Pixel size	5μm × 5μm
Fill Factor	38%
Signal Swing	180mV - 950mV
Temporal Noise	148e-
Sensitivity	0.25V/lux·s
FPN	1.6%

row starts to saturate after 150 ns integration. The total DR is therefore about 126 dB.

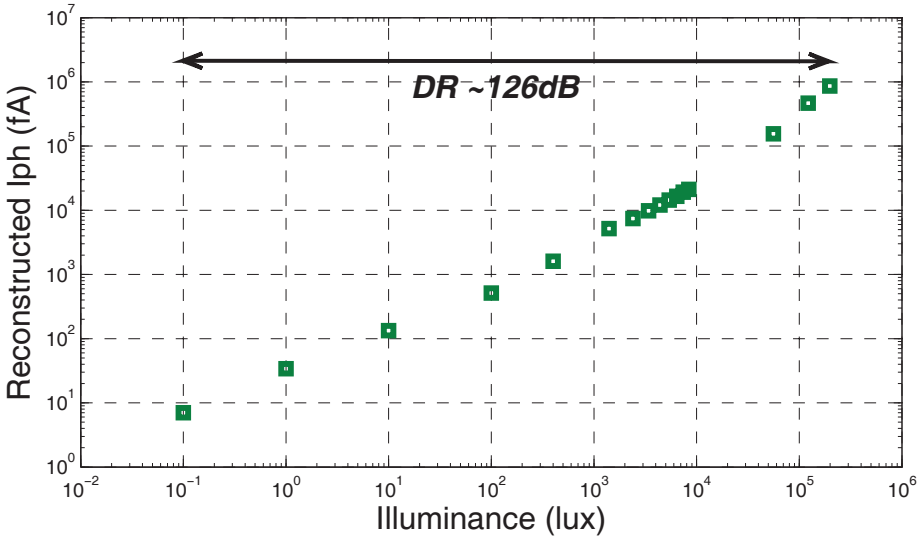


Figure 4.12: Measured photocurrent with regard to incident illuminance.

4.2.5.1 Simulated Star-Pattern Measurement

The sensor is used to image the scene of star field where the star objects ("bright pixels") in the scene are of primary concern. In order to simulate the star field imaging, we have built a test platform as shown in Fig. 4.13. The star field is simulated by letting uniform light source back-illuminate through a star pattern mask. The star pattern is made of a PCB stencil with precise position control of the "stars". The light source generates approximately 10 klux photons to pass through the star pattern and camera aperture. The measurement was done in a dark room. The sample images for simulated star-pattern measurement is shown in Fig. 4.14 under various parameter settings. We have swept the bottom threshold from 250 mV to 450 mV for three different top thresholds, respectively. The analog outputs of the sensor are converted to digital values by external Analog-to-Digital Converter (ADC). The photocurrent of each pixel is extrapolated using Eq. 4.1. Those unread pixels are regarded as dark pixels. To represent the image on the monitor, the obtained photocurrent data are further normalized to 8-bit gray-scale pixel values. The sample images are raw star image without any post processing and compensation.

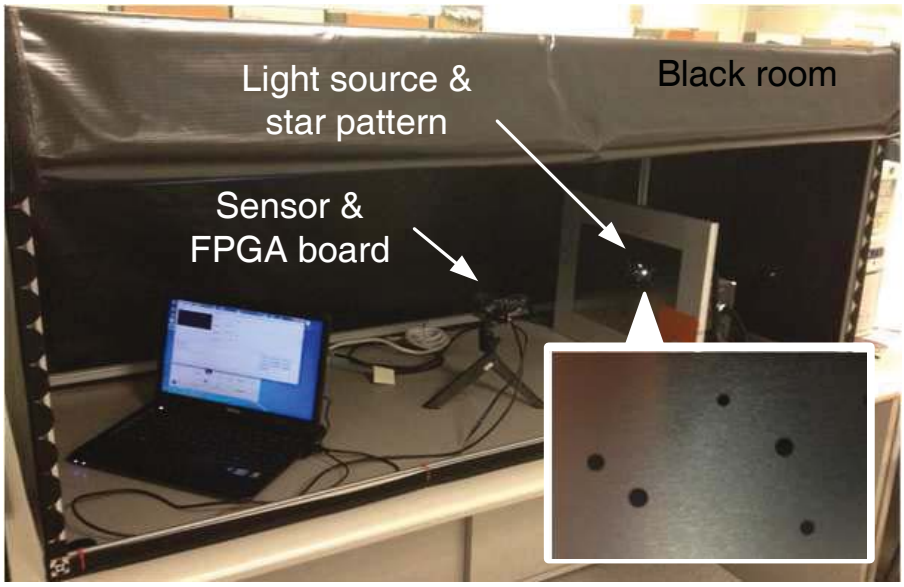


Figure 4.13: Measurement setup for capturing "star" images.

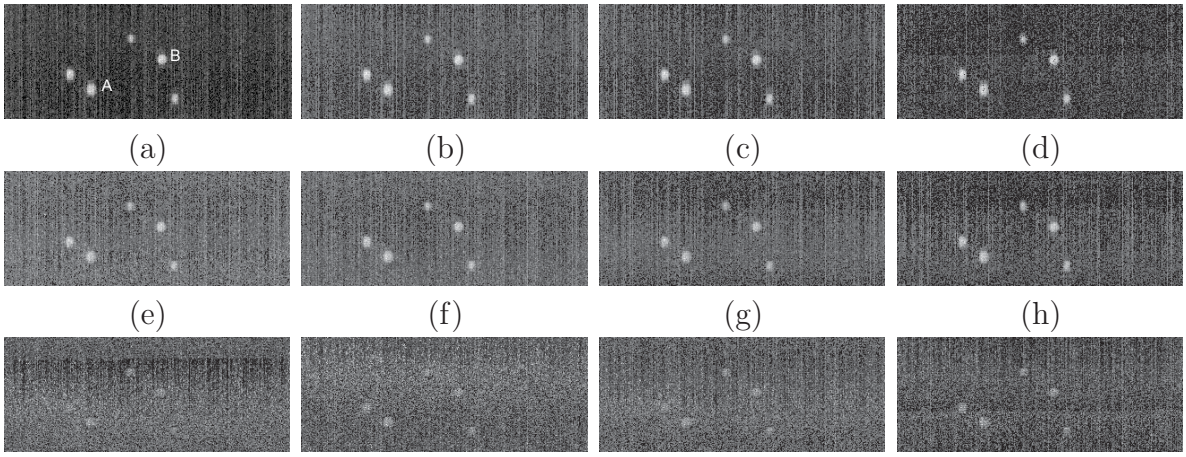


Figure 4.14: Raw sample images for simulated star-pattern measurement under different parameter settings. Images in the first row (a)-(d), top threshold is set to 500 mV and bottom threshold are 250 mV, 300 mV, 350 mV and 450 mV, respectively. In (e)-(h), top threshold is changed to 600 mV and In (i)-(l), top threshold is set to 700 mV. Two "stars", marked as A and B, are selected for centroiding evaluation.

As discussed earlier in our simulation results, both top threshold and bottom threshold play an important role in readout pixel numbers. Fig. 4.15 shows the corresponding readout percentage with different size of the readout window. It is clear that the readout percentage drops with the shrinking of the readout window. Most of the missing readouts are located in the dark background. The diversely-distributed "stars", objects in interest, are completely captured except when the readout window decreases down to 50 mV, as shown in Fig. 4.14 (c). Missing readouts start to appear inside "stars", which leads to measurement errors in star intensity.

The star illumination in a star sensor is used to calculate the star location. Utilizing its intensity values on a mass of pixels, the location of the "star" can be represented by its centroid position. We implement star centroiding [1] to assess the measurement accuracy. Fig. 4.16 shows the gray-scale illumination mapping of the sample star image after image reconstruction. All of the stars are captured without pixel saturation. The relative distances between the "stars" are used as the benchmark to evaluate the precision.

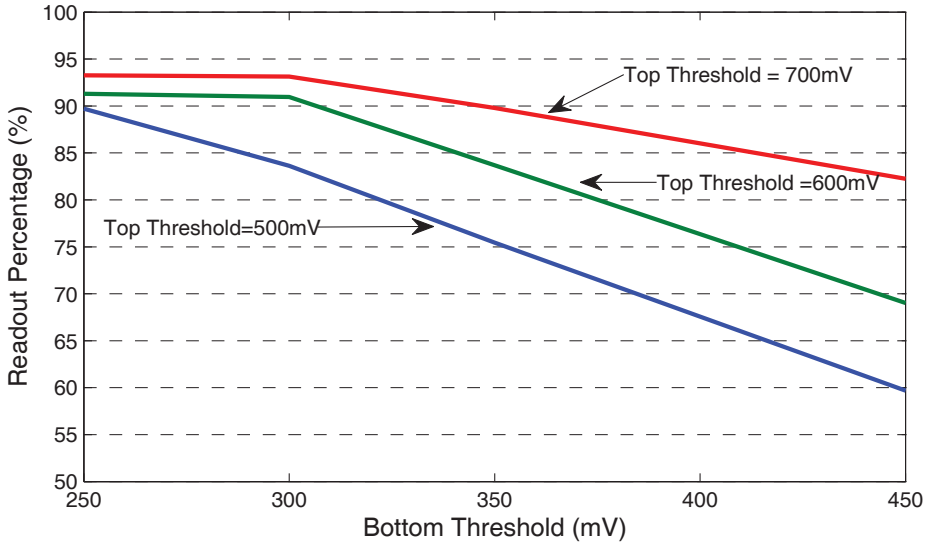


Figure 4.15: Readout percentage of the simulated star-pattern images.

Two "stars" and their distance are selected for evaluation as shown in Fig. 4.14(a). The ideal coordinates of "star" A(63, 97) and "star" B(96, 176) are used. The relative distance between the "stars" is 85.62 pixels (33 pixels horizontally and 49 pixels vertically) in the star pattern stencil. The calculated distance errors for all tested scenarios are illustrated in Fig. 4.17. We have observed sub-pixel errors for most of the tested scenarios. Top threshold has shown significant effect on the calculation error compared with bottom threshold. The absolute calculated error is above 0.89 pixels when the top threshold is 700 mV. The increase in the top threshold will cause the readout of "star" pixels to be triggered earlier with small signal magnitude. It implies that for these "star" pixels, a decreased number of the photons are received during readout. The centroiding accuracy has strong dependance on the number of the received photons [1]. In addition, the position error is also contributed by several factors including non-ideality of optics, sensor and readout circuit noise and ADC noise. The reduced magnitude of the pixel response, that is the reduced voltage difference between the reset voltage and readout voltage, causes a degraded SNR. Moreover, the missing readouts inside the "star" object

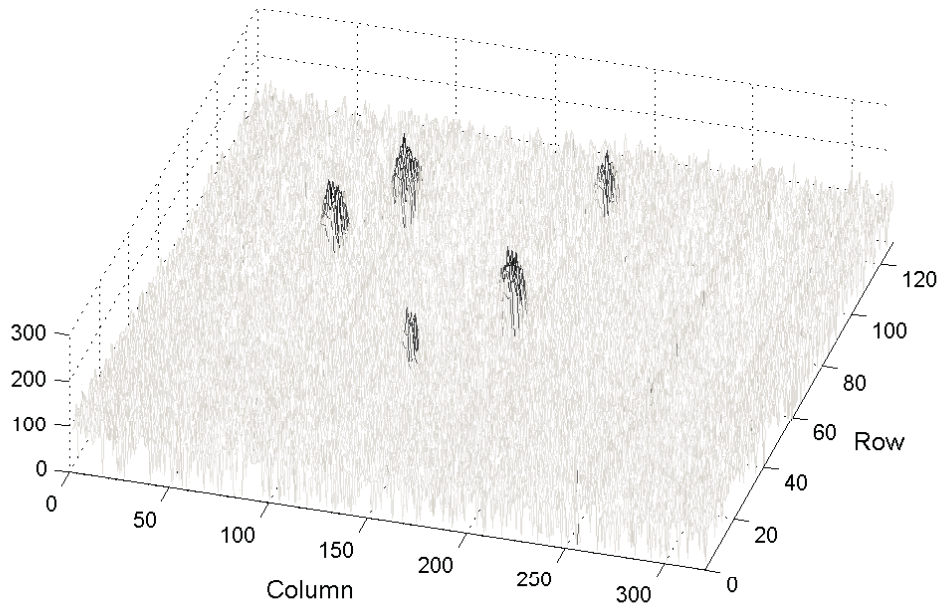


Figure 4.16: Gray-scale mapping of the star image in Fig. 4.14(a)

can also affect the centroiding error to increase. As is in the case in Fig. 4.14(d), the absolute calculated error is increased to 0.58 pixels. This is primarily due to the centroiding method that calculates the weighted center of a mass of pixels. If there are missing readouts inside the pixel mass, the calculated center will be shifted, resulting in the increase of distance calculation error.

4.2.5.2 Discussion

The two threshold voltages that form the readout window are critical parameters. According to our simulation and measurement results, the readout window is supposed to be as large as possible to reduce the possibility for a pixel to fall out of the range. As for the bottom threshold, it should be kept as low as possible to expand the readout window. Normally, it should be kept at a value slightly higher than the saturation level so that the "marked-off" pixels will not trigger the readout twice falsely. In this design, the bottom threshold can be set as low as 180 mV, which is slightly above the saturation voltage of

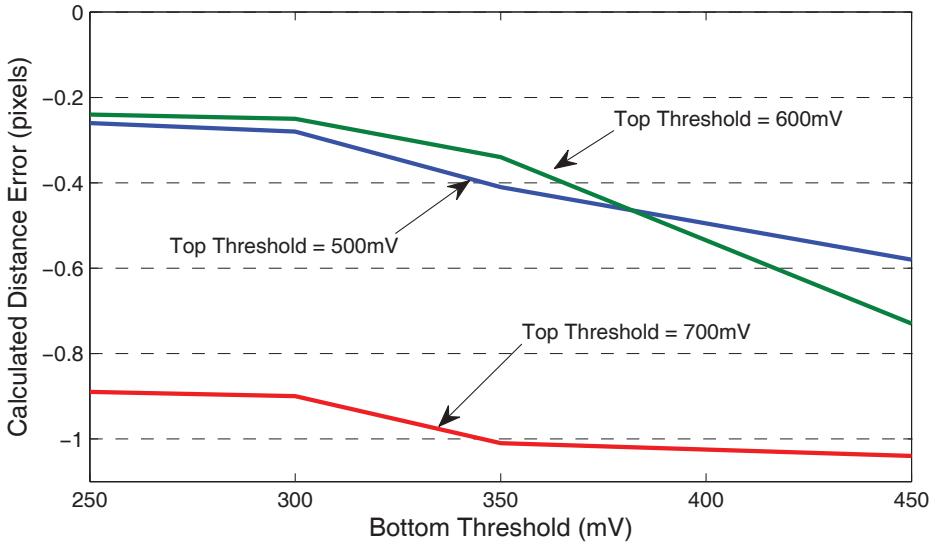


Figure 4.17: Calculated distance error with different top threshold voltage.

the pixel (150 mV after the source follower according to the simulation results). This voltage slack is big enough to avoid false detection. Top threshold, on one hand, should be high enough to guarantee a large readout window to initiate readout of "bright" pixels quickly after the exposure so as to reduce readout congestion for the rest of the pixels. On the other hand, top threshold also restricts the minimal signal magnitude, which has a critical effect on the SNR. The higher the top threshold, the easier it is for the pixels to fall into the readout window. Pixels are likely to have small signal magnitudes when they are sampled. This results in degraded SNR for those pixels. The test results shows that the "stars" can be barely captured when the top threshold is above 700mV, which appears falsely merged with the dark background. For all "star" images taken with 10 klux light source, the top threshold is supposed to be set near or below half of the signal swing so that the "stars" can receive enough photons before readout to maintain acceptable SNR.

There is possibility that pixel voltage falls out of the readout window between two rounds of scanning. This can happen when a large block of pixels have similar intensity

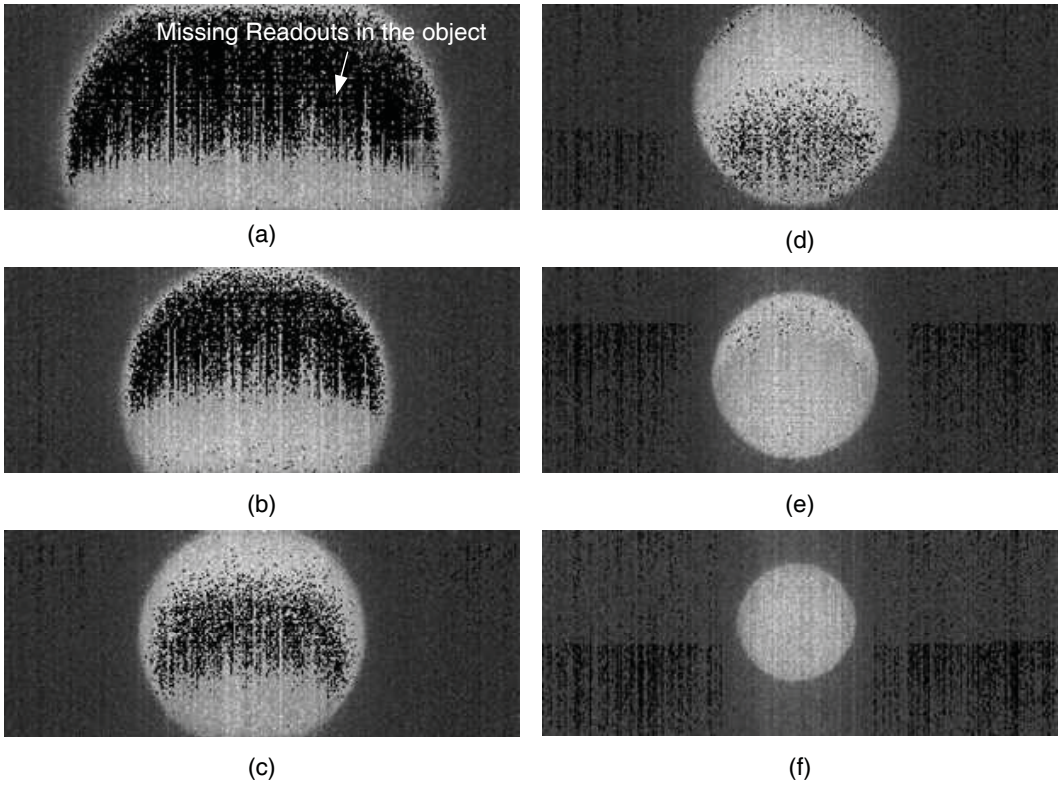


Figure 4.18: Example images of uniform circular objects with different size.

and thus takes longer time to finish the scan. Therefore higher readout speed or more readout channels should be used for a higher resolution image sensor. Fig.4.18 shows captured images of uniform-intensity circles with different size under aforementioned readout window size and Fig. 4.19 shows the readout percentage for the pixels inside the objects, respectively. When the circle is small, similar to the size of the "star" objects, the readout is able to handle all the readout requests in time. When the size of the object increases, black pixels inside the object appear since these pixel are missing during the readout and hence are regarded as dark pixels. It is worthy to note that the worst case happens if the entire pixel array is projected by a uniform intensity. The long waiting time may cause other pixels to saturate, or in other words, to fall out of the readout window.

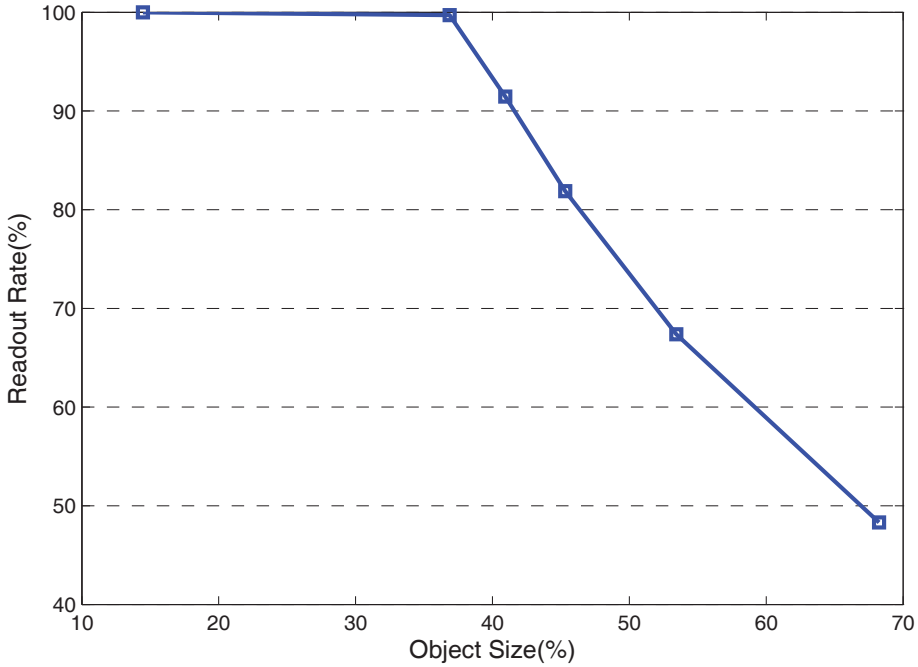


Figure 4.19: Readout percentage for the pixels inside the objects.

4.3 A Wide Dynamic Range CTIA Pixel with Dual-Exposure Charge Subtraction Scheme

This section introduces another wide dynamic range sensor architecture based on capacitive transimpedance amplifier (CTIA) pixel. The sensitivity requirement for starlight detection in star trackers is firstly discusses. Next, it describes the pixel architecture and wide dynamic range algorithm. This is followed by the implementation details and measurement results.

4.3.1 Sensitivity Requirement of CMOS Image sensors in Star tracker

Detecting a limited number of photons generated by stars is always challenging for conventional 3T APS. Due to the direct charge accumulation on the photodiode, the large photodiode capacitance results in a small voltage change, and thus low sensitivity. Also,

it is difficult to perform correlated double sampling (CDS) to suppress the dominant reset noise in a 3-Transistor APS, rendering the SNR unsuitable when high centroiding accuracy is required. One straightforward way to increase SNR is to increase the integration time.

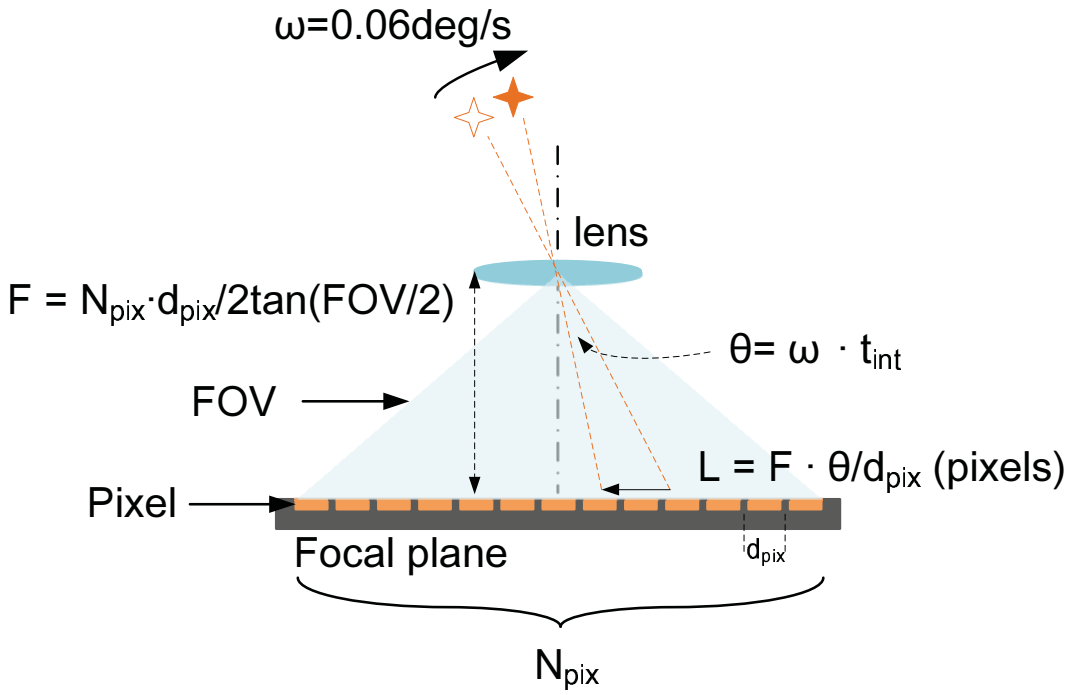


Figure 4.20: Stars travel on the focal plane during integration due to the satellite's orbit. The travel distance L is expressed in pixels in one dimension, where d_{pixel} is the pixel pitch.

However, increasing the integration time does not help increase the signal magnitude because of the dynamic condition of the orbiting satellite, as shown in Fig. 4.20. The satellite's orbital movement causes the star spot to move in a reverse direction on the focal plane, and the resulting "tail effect" induces systematic error. The travel distance on the focal plane can be expressed in terms of pixels as:

$$L = \frac{N_{pix} \cdot \omega \cdot T_{\text{int}}}{2\tan(FOV/2)} \qquad \text{(Eq. 4.3)}$$

where N_{pix} is the pixel number in one dimension of the pixel array, ω is the angular rate,

T_{int} is the integration time and FOV is the star tracker field of view (FOV). A low-earth orbit (LEO) satellite at an altitude of 600 km has an angular rate of 0.06 deg/s. For a CMOS image sensor with 1 K pixels in one dimension and 20° FOV, a 200 ms integration time can produce a shift of 0.6 pixels. Further increasing the exposure time will not increase the signal magnitude on one pixel (see Fig. 4.21). Instead, the incident photons will spread over more pixels and the signal magnitude will be limited by this shift. In addition, it also increases the systematic error when the centroiding algorithm is applied on the octave spot.

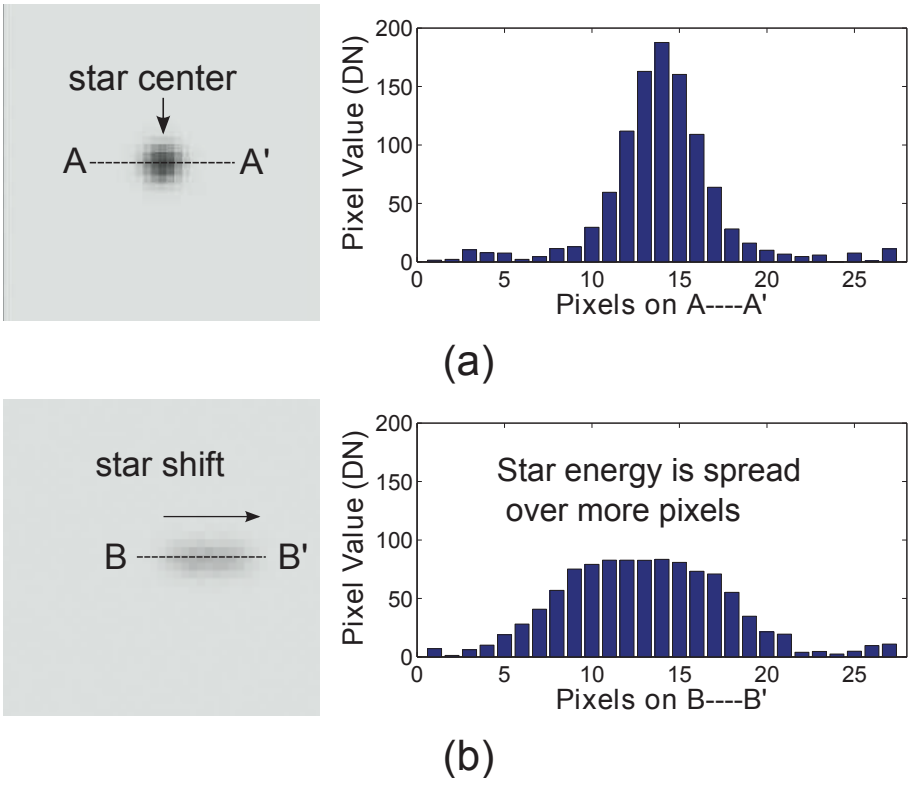


Figure 4.21: (a) and (b) are simulated static star images and integration results, respectively. (c) and (d) are simulated dynamic star images and integration results with star shift, respectively. They are captured with the same integration time. When the star center moves to its neighboring pixel during integration, the star energy is then spread over more pixels. The resulting "tail effect" does not increase the signal magnitude.

Therefore, constrained by the integration time, it is necessary to increase the sensi-

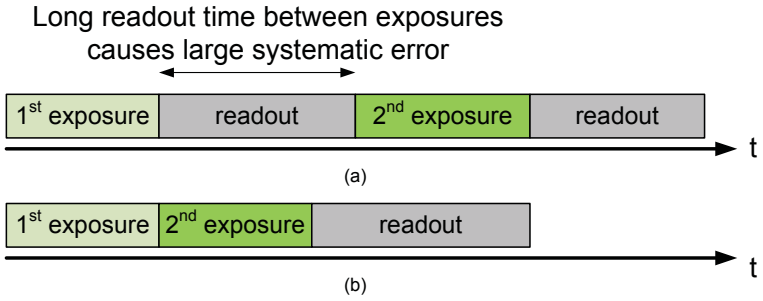


Figure 4.22: Global-shutter timing difference between (a) conventional and (b) proposed dual exposure high dynamic range method. In conventional method, there is a frame readout between two exposures. The readout time can be several milliseconds long. For example, 100 ms is expected if we assume an array of 2M pixels with 20MHz clock frequency. It causes a shift of 0.3 pixels on focal plane between two exposures, which adds to the centroiding error.

tivity against the shortened exposure time. Although, high sensitivity can easily cause bright stars to saturate, which again causes centroiding error. The extension of dynamic range is thus required. As a result, the solution to all the contradictions is a CMOS image sensor with both high sensitivity and high dynamic range. We propose a new sensor architecture based on CTIA pixel [89] [90] [91] [92] for high sensitivity. High dynamic range is achieved by a dual-exposure in-pixel charge subtraction scheme. The first exposure measures the light intensity with a saturation threshold and if saturation is found, a packet of charges is subtracted from the integration results during the second exposure. The resulting effective well capacity is increased and a wider range of photocurrent can be quantized. As shown in Fig.4.22, the scheme differs from the conventional dual exposure method in that there is no readout time in two exposures, which would otherwise be long due to large pixel array. This will minimizes the systematic error and is better suited for this application.

4.3.2 Pixel Architecture

Fig.4.23 illustrates the functional block diagram of the pixel architecture. The pixel has an integrator to accumulate the photocurrent. The output of the integrator (V_o) of

the first exposure is compared with a threshold reference to denote whether the pixel is saturated. Its result is latched in the DFF and used to decide whether to apply charge subtraction in the consecutive second exposure. If the pixel is saturated, an externally-produced voltage (V_{sub}) is subtracted from V_o.

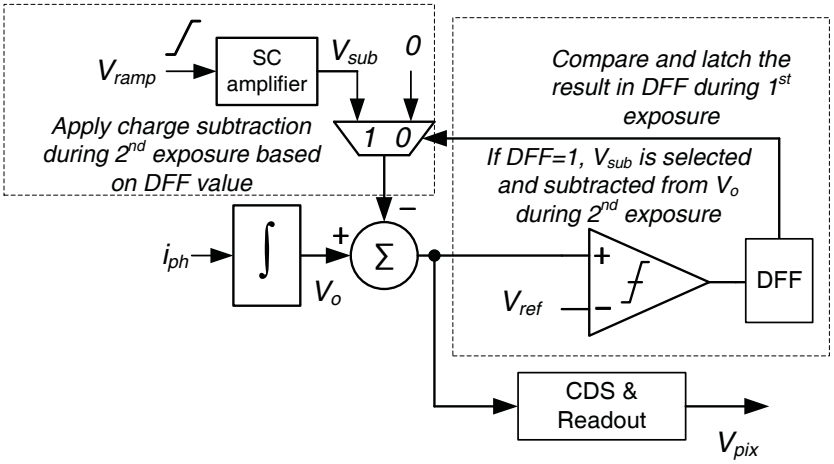


Figure 4.23: Pixel functional block diagram.

The proposed CTIA pixel schematic is shown in Fig. 4.24. The pixel consists of a fundamental CTIA pixel, circuits for charge subtraction, a comparator with D flip flop

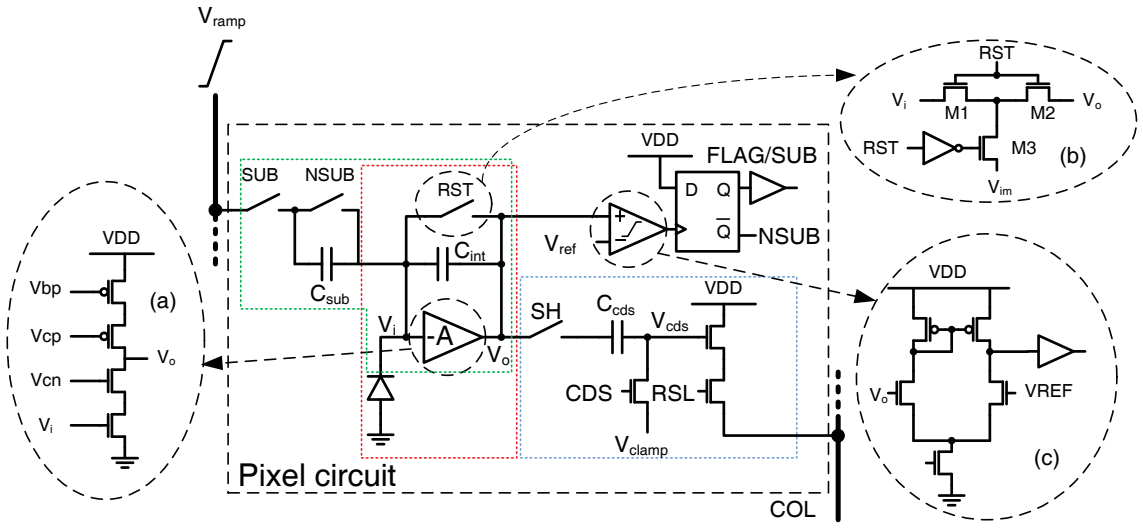


Figure 4.24: The schematic of the pixel circuit. (a) the schematic of the OTA, (b) the reset switch and (c) the comparator are shown respectively.

(DFF), and readout circuits. In CTIA pixel, the photodiode is held at a constant voltage and photocurrent is integrated on C_{int}. The output follows:

$$V_o \approx \frac{1}{C_{int}} \int I_{ph} dt \qquad \text{(Eq. 4.4)}$$

The schematic of the OTA (Fig. 4.24 (a)) is a single-ended cascode common-source amplifier. The reset switch (Fig. 4.24 (b)) consists of three NMOS transistors and an inverter instead of one simple NMOS transistor. During integration, the node between $M1$ and $M2$ is tied to an externally-produced bias voltage (V_{im}) close to V_i. So the leakage path from V_o to V_i is eliminated when V_o builds up. The comparator (Fig. 4.24 (c)) is a five-transistor OTA used in open-loop configuration followed by a digital buffer.

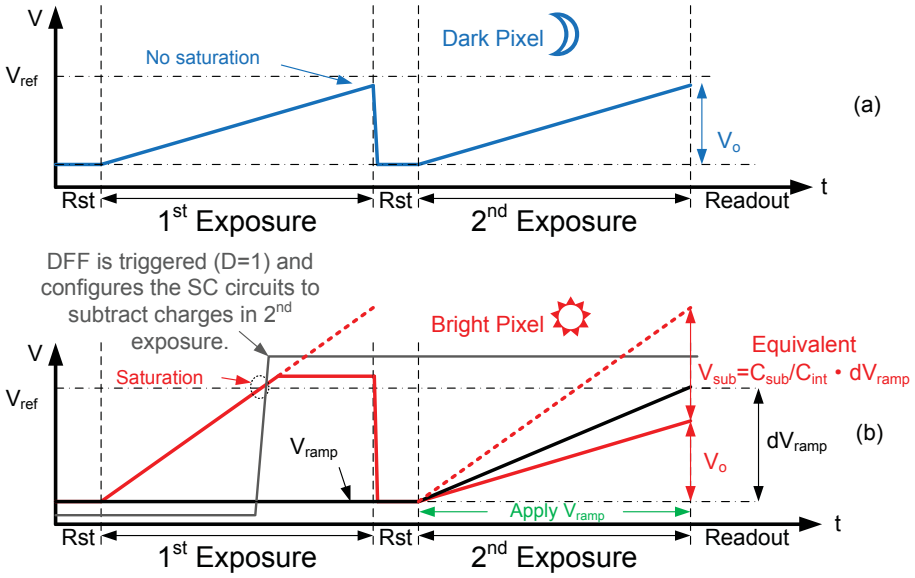


Figure 4.25: Pixel operation timing diagram.

Fig. 4.25 shows the timing diagram of the pixel. The pixel has two equal-length exposures (T_{int}). In first exposure, pixel voltage is compared with a reference threshold V_{ref} to determine whether the pixel requires charge subtraction. If the photocurrent is small, the comparator does not toggle, as the case in Fig. 4.25 (a), the DFF will not be

triggered to reconfigure the pixel circuit. Hence, both exposures have the same response. The photocurrent can be simply expressed as:

$$I_{ph} = \frac{C_{int} \cdot V_o}{T_{int}} \quad \text{(Eq. 4.5)}$$

Once V_o reaches V_{ref} in the first exposure, as the case in Fig. 4.25 (b), the DFF will then reconfigure the switches associated with C_{sub}. It connects C_{sub} to a column bus driven by a ramp signal (V_{ramp}). V_{ramp} rises as the second exposure starts, which continuously subtracts the charges from the integration results. The amount of subtracted charges is designed to be the well capacity of the pixel. The photocurrent can then be expressed as:

$$I_{ph} = \frac{C_{int} \cdot V_o + C_{sub} \cdot dV_{ramp}}{T_{int}} \quad \text{(Eq. 4.6)}$$

Since the DFF stores the information whether the pixel conducts charge subtraction, the pixel outputs both pixel voltage (V_o) and digital signal ($FLAG$) for image reconstruction.

4.3.3 Prototype Chip and Measurement Results

Fig. 4.26 (a) shows the test setup with the prototype chip. The sensor is illuminated by back-lit point sources in a dark room. Fig. 4.26 (b) and (c) show the prototype chip with 4×4 pixels and pixel layout implemented in 3.3 V devices with Global Foundries 65 nm mixed-signal CMOS process, respectively. The pixel is 22×22 μm^2 and uses a N-well/P-sub photodiode. C_{int} and C_{sub} are designed to be 10 fF. The value of C_{cds} is 28 fF. Fig. 4.27 shows the measured photocurrent with incident light intensity. The sensitivity is about 3.8 V/lux·s. With charge subtraction, DR increases about 12 dB. Table. 4.2 summarizes the sensor performance and comparison with a commercial star sensor (Cypress STAR-1000).

Three point sources are projected at the centers of pixel A, B, and C to simulate "star" signals, as shown in Fig. 4.26(b). The lens is slightly defocused to spread the signal in

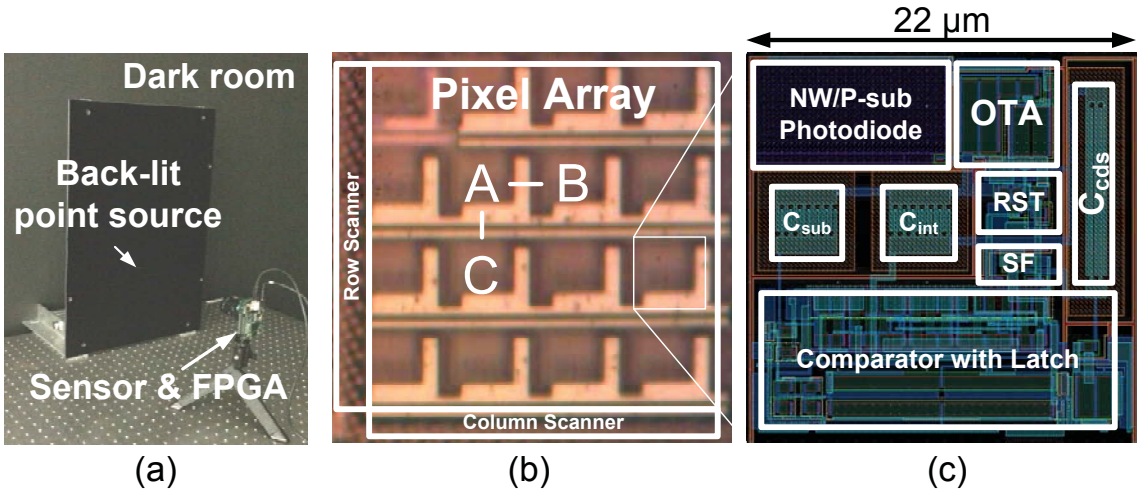


Figure 4.26: (a) Test setup, (b) chip microphotograph and (c) pixel layout.

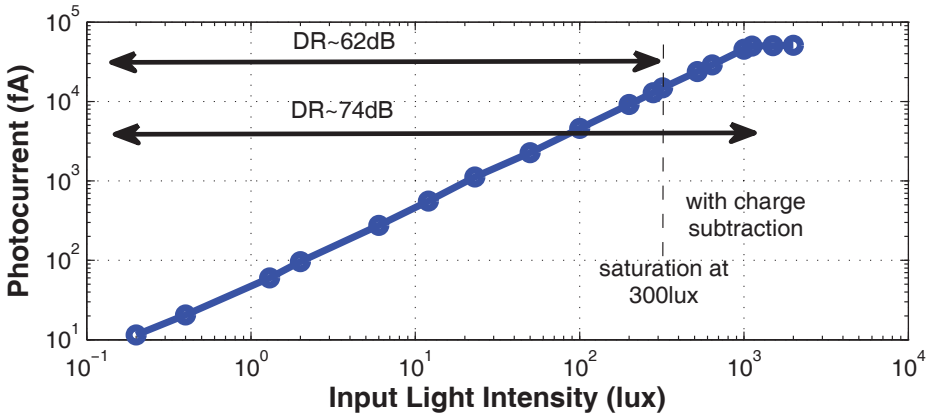


Figure 4.27: Measured photocurrent with regard to incident light intensity. The pixel saturates at around 300 lux. With charge subtraction, the dynamic range increases by approximately 12dB and saturates at around 1100 lux.

a 3 × 3 pixel region. The centroids are calculated by center-of-mass algorithm in this region [1]. Centroid distance AB and AC are compared. Fig. 4.28 shows this distance error at different exposure time. The centroiding accuracy increases with exposure time due to increased signal magnitude and its SNR. After pixel saturation, no further obvious improvement on centroiding accuracy is observed. With charge subtraction, the pixel can still accurately quantize the photocurrent and the centroiding accuracy continues improving.

Table 4.2: Performance Summary and Comparison

Specification	STAR-1000	This work
Technology	NA	GF 65 nm CMOS
Pixel Size	15×15 μm^2	22×22 μm^2 (FF = 14%)
Conversion Gain	11.4 μV/e-	16 μV/e-
Signal Swing	1.1 V	1.38 V
Dark Current	223 pA/cm^2	992 pA/cm^2
Random Noise	35 e-	980 μV (61 e-)
FPN	0.56%	0.73%
SNR	NA	62 dB at full swing
Dynamic Range	72 dB	62 dB (74 dB with charge subtraction)

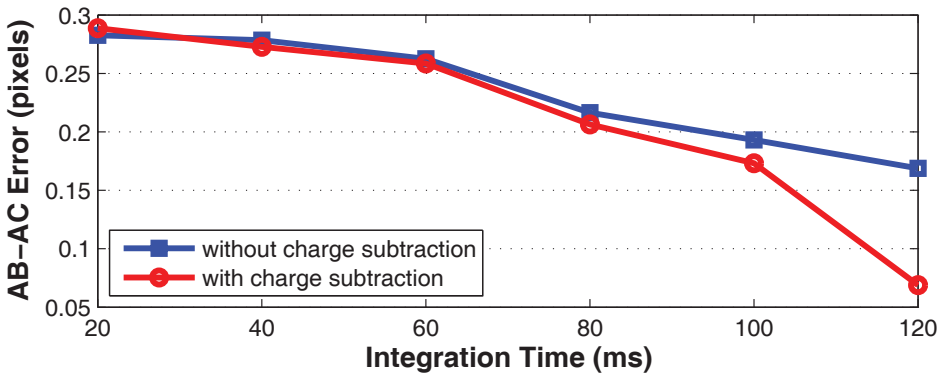


Figure 4.28: Measured $AB - AC$ distance error at different integration times. "star" pixels does not saturate when integration time is small, so charge subtraction does not improve the error obviously. However, saturation occurs in "stars" after about 80 ms. With charge subtraction, centroiding accuracy improves much better compared with the saturated one.

4.4 Conclusion

Two novel wide dynamic range CMOS image sensor architectures are proposed for star trackers. The first novel wide dynamic range star sensor architecture allows adaptive integration time for each pixel by means of a cyclic checking process during integration. Brighter pixels will be detected and read out at an earlier time to avoid saturation and dimmer pixels can have longer integration time. Due to the voltage detection nature

of the sensor architecture, it can be categorized into the saturation detection scheme. Compared with other solutions in this category, the pixel maintains compact footprint and high fill factor. The shrinking size of the pixels can be beneficial to high-resolution integration to increase the field of view in star tracker. A proof-of-concept chip has been fabricated in Global Foundries 0.18 μm 1P6M CMOS technology. According to our simulation and experimental results, the architecture demonstrates a great potential for star tracker applications where pixel intensities are sparsely distributed. Due to the use of readout window and cyclical scanning, a pixel has the chance to fall out of the readout window between two consecutive rounds of scanning. The possibility of the missing readout is related to readout bandwidth and pixel intensity distribution across the pixel array. Higher readout speed or more readout channels should be adopted for high resolution integration.

In addition, another new sensor architecture is proposed based on high sensitivity CTIA pixel in consideration of constrained exposure conditions in star trackers. Making use of calculation capability of the CTIA pixel, an in-pixel charge subtraction algorithm is proposed for dynamic range improvement. A proof-of-concept chip has been fabricated in Global Foundry 65 nm CMOS process. Measurement results show that the sensor achieves 3.8 V/lux·s sensitivity with a 22×22 μm^2 pixel and 12 dB increase of dynamic range. After performing charge subtraction, the centroiding accuracy of saturated stars is improved by over 0.1 pixels.

Chapter 5

A Global-Shutter Star Centroiding Measurement Sensor

5.1 Introduction

The positions of star centroids are crucial information in rebuilding the angular information for attitude determination. There are many factors that influence centroiding accuracy, such as optical system design, centroiding measurement and centroiding algorithm. While some of these factors contributes to a systematic error, which can be calibrated or improved from the system perspective, the centroiding error due to starlight measurement adds to a random contribution, which can affect the overall centroiding error significantly.

The centroiding accuracy is highly dependent on the star sensor's performance. In addition to the radiation tolerance and dynamic range requirement, the measurement accuracy can be improved by increasing the SNR of star sensor. Enhanced VLSI architectures for star sensors require exploring since conventional APS presents limited SNR in such low illumination conditions as starlight detection. Therefore, in search of VLSI solutions that enables to improve the accuracy of centroid measurement, this chapter introduces a new CMOS image sensor architecture for star centroid measurement. A novel SNR improvement algorithm is proposed with the new architecture. Unique to this

application, it allows SNR improvement in star regions on the focal plane. The sensor is able to segment star regions and background by means of global thresholding. A reference is generated for each star region by calculating its mean level. The difference between the star signals and this local reference is then amplified, effectively increasing the SNR. In the following sections, the operation principle, sensor architecture, implementation details as well as measurement results are reported, respectively.

5.2 Focal-Plane SNR Improvement Algorithm

The proposed algorithmic process of the star-SNR improvement scheme is illustrated in Fig. 5.1. It shows in one dimension two "star" responses with different intensity profiles. The sensor is firstly able to locate "star pixels" on the focal plane by means of global thresholding. It segments different star regions and filters the background. To increase the SNR in each region, these pixels are clustered to generate a local reference by calculating their mean levels ($AVG1$, $AVG2$). Each star will have its own reference adaptive to its starlight intensity. Star signals can thus be amplified with their own reference. Unlike a global reference, the local reference acts like an "AC ground" and only the differences between star signals are amplified.

5.3 Sensor Architecture

The block diagram of the sensor architecture is shown in Fig. 5.2. It comprises a 128×96 pixel array, column-level CDS and centroiding gain circuits, selective row and column scanners with address encoders and a main controller. The pixel array performs global thresholding during integration. In the pixel array, each pixel has cluster interconnections with its four neighbouring pixels. It is also connected to two $RCFG/CCFG$ buses. The buses are reset to high. Once a "star" is detected, the horizontal $RCFG$ bus is pulled down and the shift register chain in the row scanner is configured. The shift register

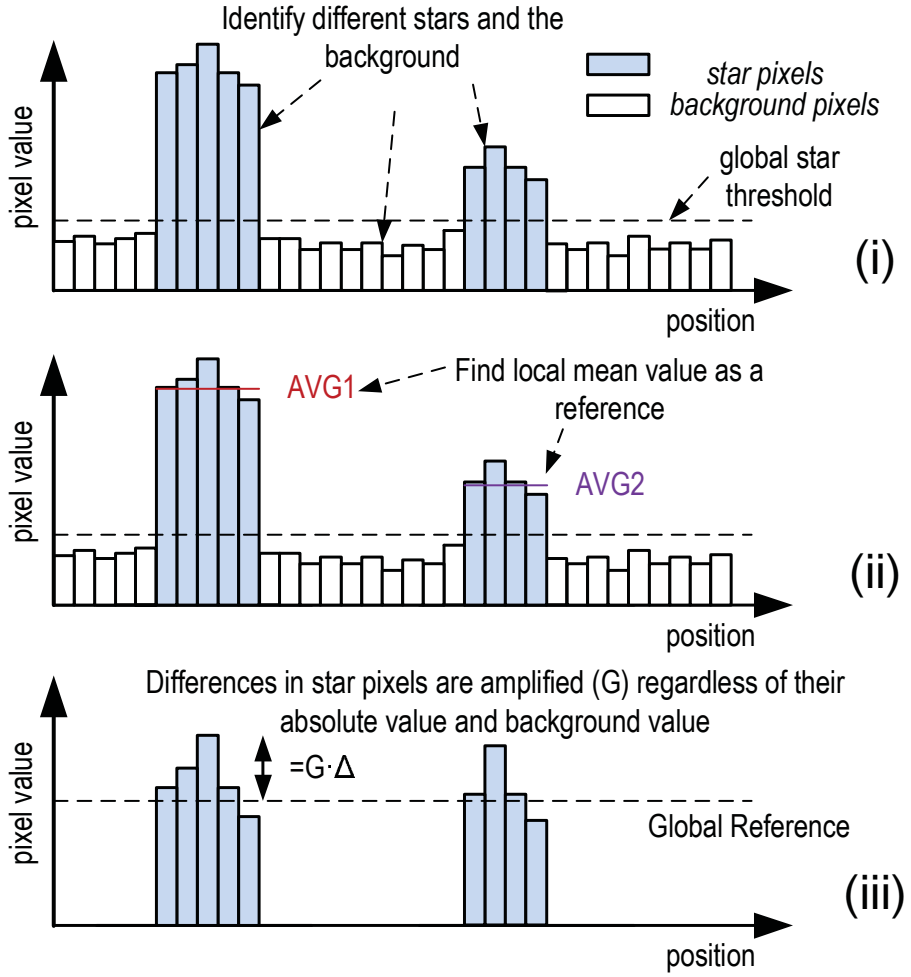


Figure 5.1: Star thresholding and local average calculation. The global star threshold is used to locate star region, and the mean value is calculated within the region. In this way, each different star will have an individual mean value. This mean value is then used as a local reference for signal amplification.

is similar to the one in [93] and can be bypassed if the $RCFG$ bus is high. Likewise, the $CCFG$ bus is pulled down when this row is selected during readout. The selective readout can only report the pixels in the ROI. The configuration latch in the shift register can also be overridden by external command to force a sequential scan so that the sensor can also output the snapshot frame. Correlated Double Sampling (CDS) and star signal amplification are performed in column-level circuits.

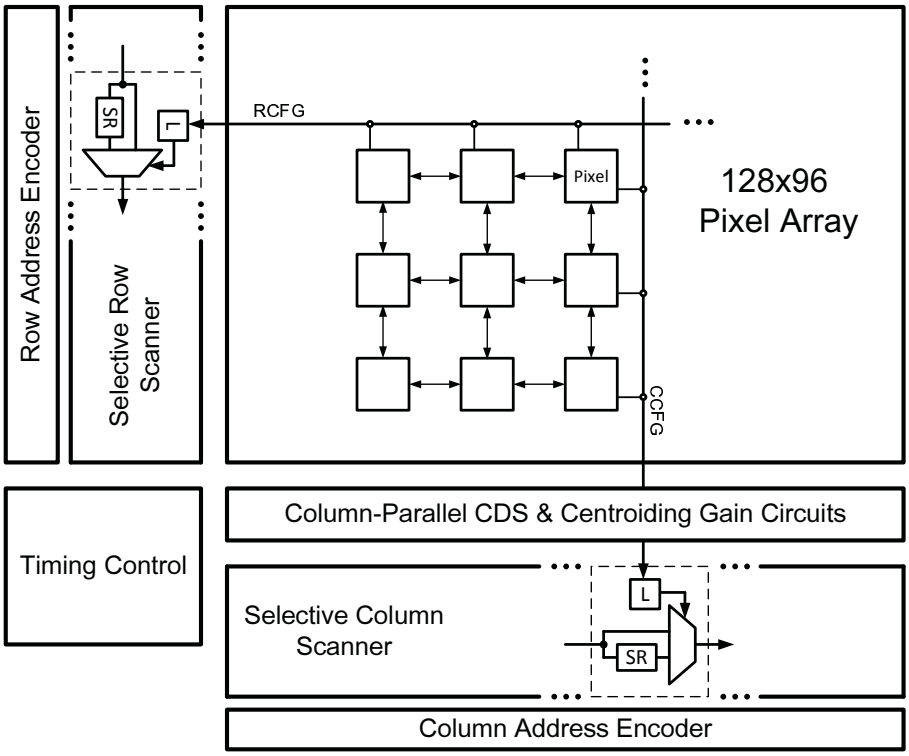


Figure 5.2: Block diagram of the proposed sensor architecture.

5.3.1 Pixel Circuits and Operation

Fig. 5.3 shows the schematic of the pixel circuits. A CTIA pixel is used as the starlight detector. By designing a small value of the integration capacitor, the sensitivity to starlight can be increased. The reset switch is a T-type switch. It consists of three NMOS transistors and an inverter. The node between M1 and M2 is tied to an externally-produced bias voltage (V_{im}) close to V_i during integration. So the leakage path from V_o to V_i is eliminated when V_o builds up. Otherwise, a single NMOS transistor would inject a subthreshold leakage current from output of the OTA to the photodiode. This leakage current can be as large as the photocurrent in low-light condition. The same switch structure is also applied to $SH0$, because V_{rst} must hold for the entire integration time before it is read out. The OTA is a two-stage seven-transistor operational amplifier. The pixel has three MOS capacitors ($C0$, $C1$, $C2$) as analog memories to temporarily

store the pixel values V_{rst}, V_{sig} and V_{avg}, respectively. Each capacitor is connected to a source follower to drive a column bus. The latched-type comparator compares V_{sig} with global threshold V_{star}. The comparison result, denoted as $flag$, controls four switches that connect to its four neighbour pixels. It also controls the switches that pull down the RCFG bus and CCFG bus.

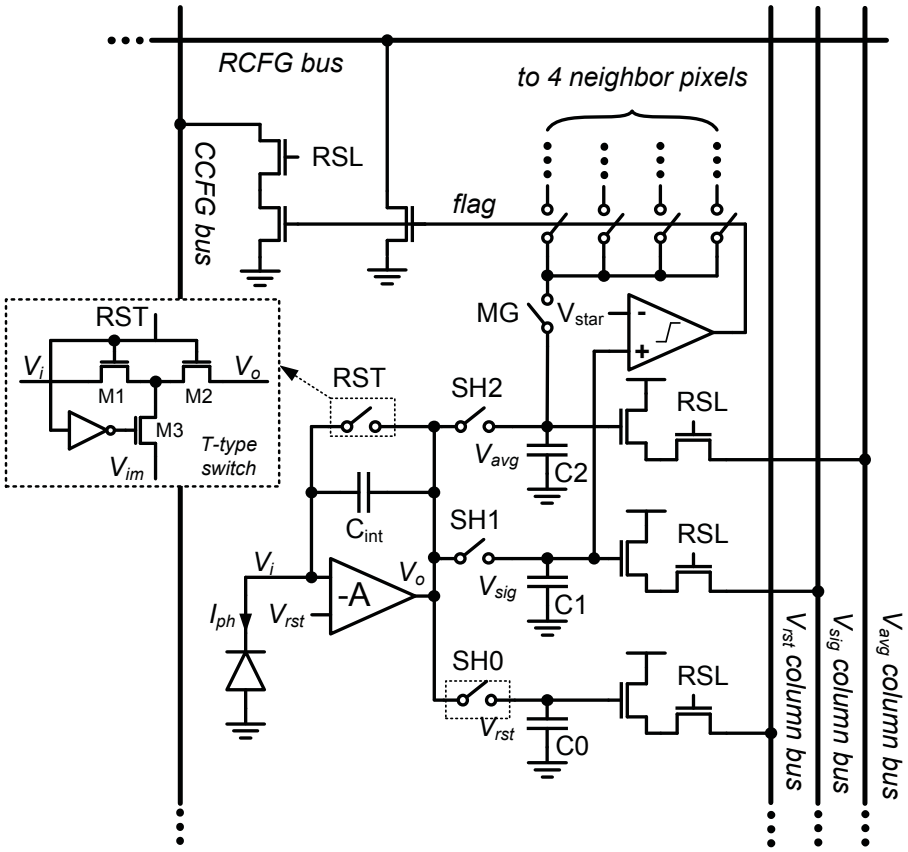


Figure 5.3: Schematic of the pixel circuits. A T-type switch is used for RST switch.

The timing diagram of the pixel operation is shown in Fig. 5.4. The pixel array is globally reset initially. To cancel the reset noise, $SH0$ is turned off slightly after pixel reset. The reset level of the CTIA pixel, including the negative charge injection of the reset switch, the reset noise and the OTA offset, is sampled on $C0$ (at T0). During integration, once V_{sig} is larger than V_{star}, the comparator toggles and raises $flag$. It turns

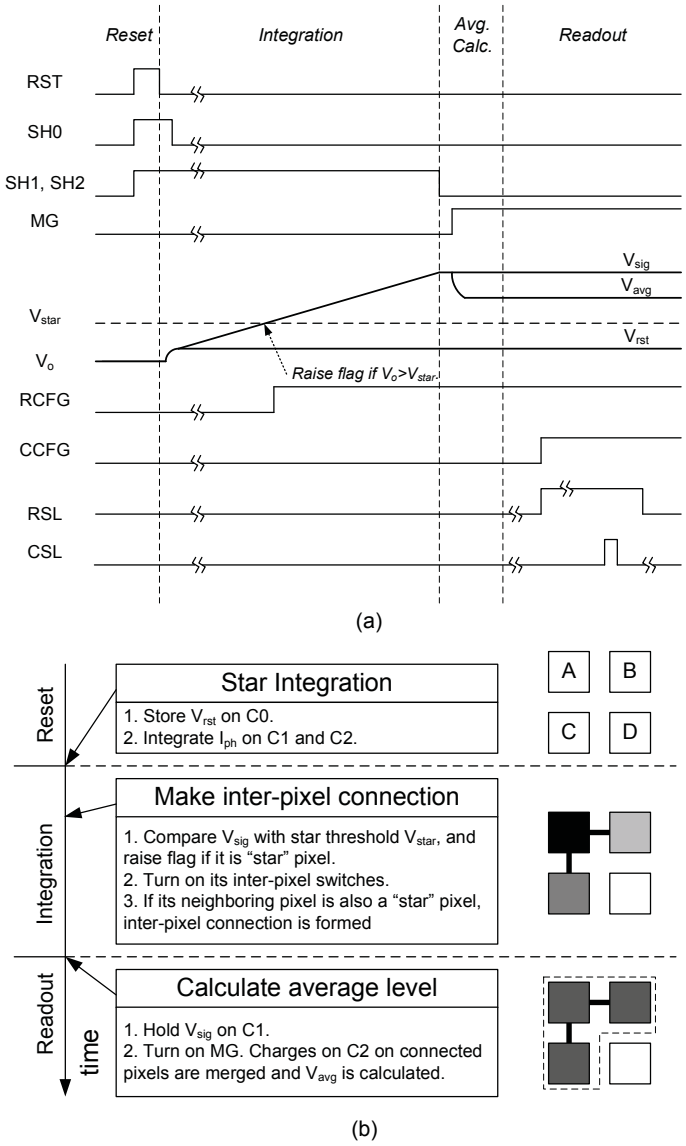


Figure 5.4: (a) Timing diagram and (b) operation flow of the pixel circuits. An example block diagram of 2 × 2 pixel array demonstrates the inter-pixel operation. Before integration, pixel reset values are sampled on the C0 capacitor in order to perform. During integration, pixels that reaches star threshold make connection with its neighboring pixels. pixels can make such connections until the end of integration. At the end of the integration, the connected pixels formes a star cluster (pixel A, B and C). When the MG is turned on, charges on C2 of these pixels are merged and averaged. The local reference V_{avg} is accordingly calculated.

on the pass switches to its four neighbour pixels. If its neighbour pixels also triggers $flag$, a connection is formed (e.g. pixel A and pixel B at T1). Until the end of the integration, at T2, pixels can make connections. The process finally forms a "star" pixel cluster. When MG is turned on at T3, charges on C3 of all connected pixels are merged and averaged so that a local average reference is formed.

5.3.2 Pixel Implementation

Fig.5.5 shows the layout of the pixel with every building block highlighted. The top routing layers (M3 and M4) are not shown for clarity.

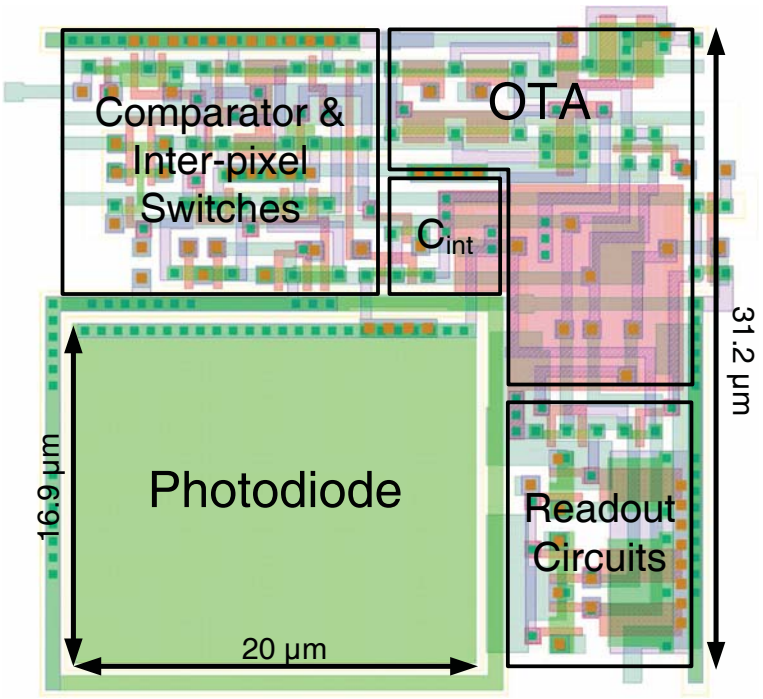


Figure 5.5: Pixel layout.

The pixel features the footprint of 31.2 μm × 31.2 μm. A 20 μm×16.9 μm N-well/P-sub photodiode is used and surrounded by the guard ring. The resulting fill factor is about 34.7%. An anti-reflective coating layer is placed above the photodiode in order to improve the responsivity. The integration capacitor is designed to be 4.6 fF and

implemented in a PIP capacitor. The size of sampling NMOS capacitors are designed to be 25 fF. They are placed next to each other for better matching. They are also shielded from signal wires with GND metal plates. All bias and reference voltages are supplied externally.

5.3.3 Pixel Noise Analysis

This section discussed the pixel noise analysis. Major noise sources in the CTIA pixel include OTA noise, reset noise and readout noise. Inside pixel, the noise at the output of the CTIA can be estimated as:

$$\overline{v_{no,ota}^2} = \left(1 + \frac{C_{pd}}{C_{int}}\right)^2 \overline{v_{ni,ota}^2} \qquad \text{(Eq. 5.1)}$$

where $\overline{v_{ni,ota}^2}$ is the input-referred noise power of the OTA.

The reset noise on C_{int} is expressed as:

$$\overline{v_{n,rst}^2} = \frac{kT}{C_{int}} \qquad \text{(Eq. 5.2)}$$

In order to cancel this reset noise, the pixel requires to sample both the reset value and signal value onto C_{rst} and C_{sig}, respectively. This will induce additional sampling noise. The following sampling noises are added:

$$\overline{v_{n,sh}^2} = \frac{kT}{C_{rst}} + \frac{kT}{C_{sig}} \qquad \text{(Eq. 5.3)}$$

If we make the size of both capacitors equal, that is $C_{rst} = C_{sig} = C_{sh}$. The resulting differential sampling noises are then:

$$\overline{v_{n,sh}^2} = 2\frac{kT}{C_{sh}} \qquad \text{(Eq. 5.4)}$$

Since the reset noise $\overline{v_{n,rst}^2}$ is dominant noise component due to small size of C_{int}, it is still beneficial to perform CDS even the sampling noise is doubled. The added

sampling noise can be suppressed by using large C_{sh}. For example, if sampling capacitor are designed to be 30fF, the differential sampling noise is then 0.53 mV_{rms} at room temperature (T=300K), about half of that of reset noise with $C_{int} = 4fF$.

Accordingly, with the cancellation of the reset noise by CDS, the input-referred noise of the CTIA pixel is then:

$$\overline{v_{n,pix}^2} = 2\left(1 + \frac{C_{pd}}{C_{\text{int}}}\right)^2 \overline{v_{n,ota}^2} + 2\frac{kT}{C_{sh}} + 2\overline{v_{sf}^2} + \overline{v_{n,col}^2} \qquad \text{(Eq. 5.5)}$$

where $\overline{v_{n,col}^2}$ is the input-referred noise power of the column-level circuits and $\overline{v_{sf}^2}$ is the noise power of the in-pixel source follower.

5.3.4 Column Signal Path

The circuits and timing diagrams of the column signal path are shown in Fig. 5.6 and Fig. 5.7, respectively. The column circuits mainly have two stages of charge amplifiers and a mode multiplexer. The first stage samples V_{rst} and V_{sig} and perform CDS with gain of one. The second charge amplifier samples CDS result V_{cds} and V_{avg} and outputs the amplified star signal with variable gain. This stage has a gain of 1, 2, 4 or 8, which is controlled externally by gain select signals ($G0$, $G1$ and $G2$). The mode switches SM

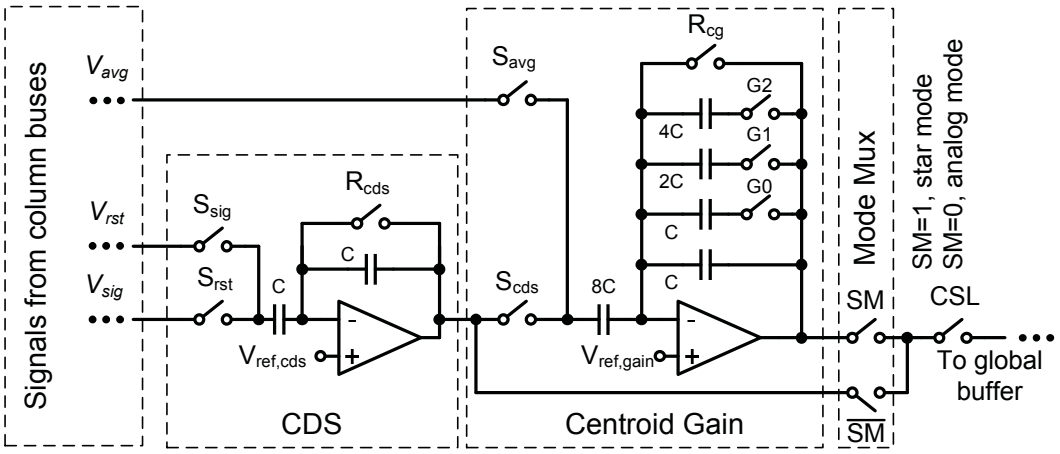


Figure 5.6: Column signal path which is composed two-stage switched-capacitor circuits.

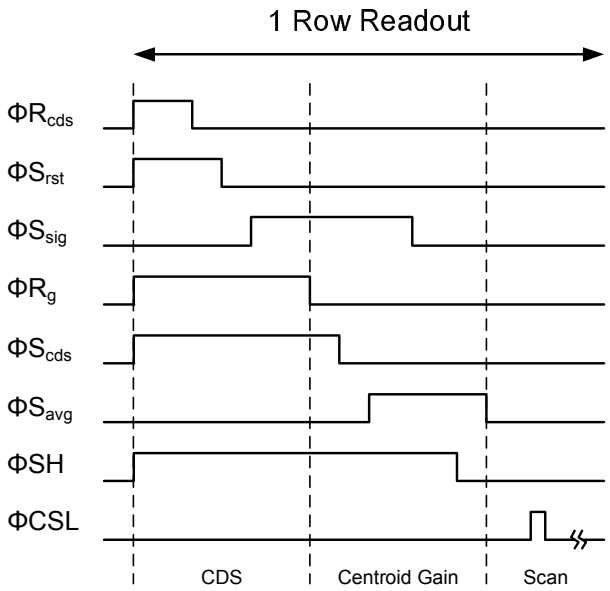


Figure 5.7: Timing diagram of column signal path for readout of one row.

select the output of either stage. Hence, it enables either imaging mode or centroiding readout mode.

5.4 Measurement Results

A proof-of-concept chip was fabricated using a 0.35 μm 2-poly 4-metal CMOS mixed-signal process. Fig. 5.8 shows the chip microphotograph where the main building blocks are highlighted. The core of the chip is 4.7 mm $\times$ 4.6 mm large. The sensor is interfaced with a FPGA test platform. The FPGA provides clock and control signals to the sensor. The system clock frequency to drive the sensor is 10 MHz. The sensor's outputs are converted to digital data by an off-chip 12-bit ADC and collected by a RAM on the test platform.

The sensitivity is characterized with an integrating sphere. the sensor was exposed at fixed integration time (6 μs) without mounting the lens at different luminous levels. At each step of illumination, we sampled 100 frames to obtain the averaged pixel response. The averaged pixel response (in ADC units) versus different luminous exposures is shown

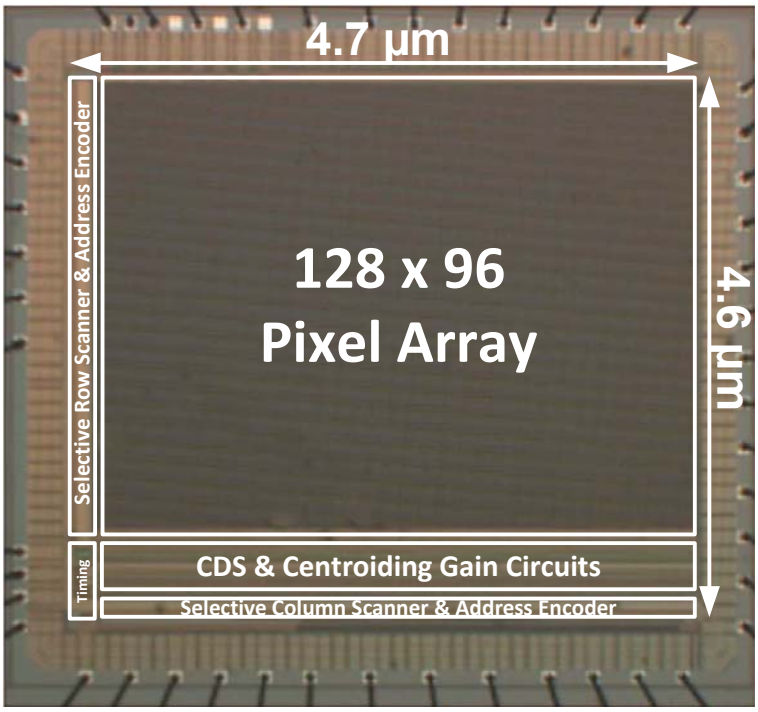


Figure 5.8: Chip microphotograph.

in Fig. 5.9. The slope of the curve is therefore the sensitivity. The measured sensitivity is 10.9 V/lux·s. The conversion gain is 33.6 μV/e-. The temporal noise is measured to be 3.4 mV_{rms} and the dynamic range is 55.7 dB. Other characterization results are summarized in Table 5.1.

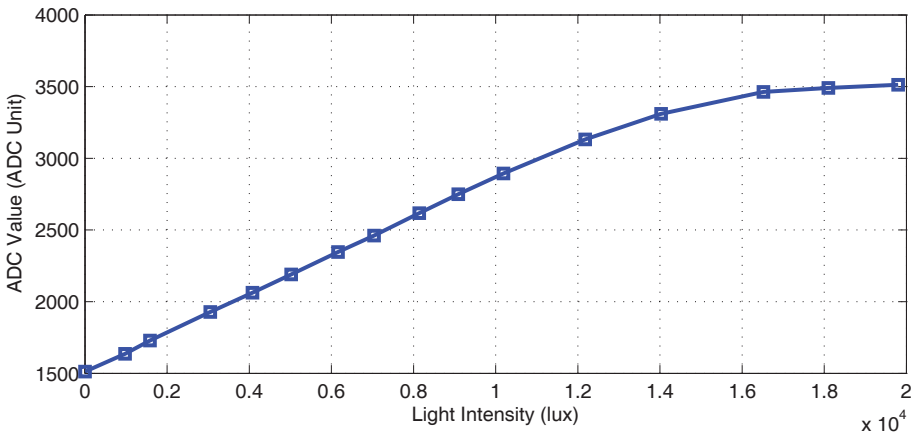


Figure 5.9: Pixel response curve.

Table 5.1: Performance Summary of the Sensor

Technology	AMS 0.35 μm mixed-signal CMOS
Pixel Size	31.2×31.2 μm^2
Photodetector Type	N-well/P-sub
Photodetector Size	20×16.9 μm^2
Fill Factor	34.7%
Photodiode Capacitance	64.68 fF
Photodiode Responsivity	0.32 A/W @ 632 nm
Dark Current	1.15 fA/μm^2
Integration Capacitance	4.76 fF
Conversion Gain	33.6 μV/e-
Signal Swing	1.2 V
FPN	0.72%
Temporal Noise	3.4 mV_{rms}
Sensitivity	10.9 V/lux·s
Dynamic Range	50.9 dB

The snapshot frame can be obtained by switching to imaging mode in column signal path and forcing a sequential scan in row and column scanners. Fig. 5.10 shows two sample images. They were captured with 4 ms integration time in ambient lighting condition (300lux).

Figure 5.10: Sample images in snapshot mode.

The centroiding test was performed in a dark room. The test setup is shown in Fig.

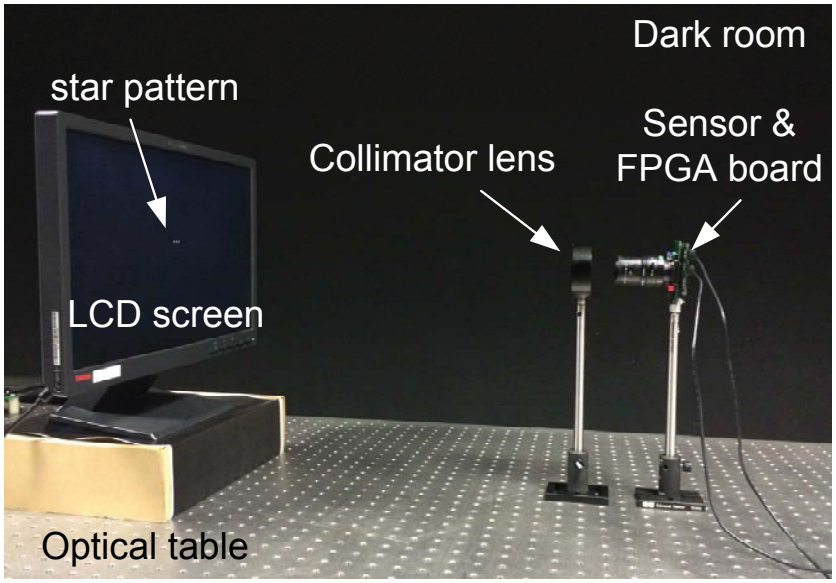


Figure 5.11: Centroid measurement setup.

5.11. The test equipments are placed on an optical table. The sensor was placed behind a collimator lens. The main purpose of the collimator lens is to convert the divergent light beams from the light source (LCD screen) to become parallel to simulate starlight. The star pattern were three circular spots at equal distances on a LCD screen. The reason of using LCD screen is because it is the most accurate test pattern with ground truth distance. The details of the test pattern are illustrated in Fig. 5.12. Four different patterns have been used. We have varied the test patterns in either spot profile or the spot size. Both uniform profile and 2-D quasi-gaussian profile were tested. The distance of AB or BC are 12 pixels. Each circular spot has a diameter of eight LCD pixels. Spot C was replaced with a 12-pixel-diameter spot in pattern B and pattern D while the spot pitch is still 12 pixels. The sensor was mounted with a lens (12 mm focal length and aperture = f/4). The lens is then slightly defocused to spread each spot over 7×7 ROI. The COM centroiding algorithm was applied to calculate the respective centroids. After that, the relative distance error $AB/BC - 1$ was measured to evaluate the centroiding accuracy.

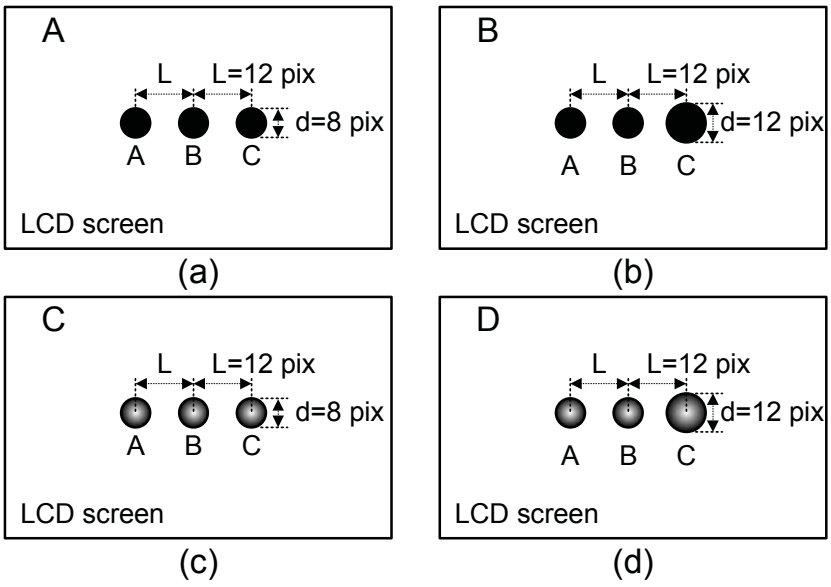


Figure 5.12: Test pattern: three circular spots at equal distance on a LCD screen. (a) Pattern A: uniform profile and uniform size. (b) Pattern B: uniform profile and different size. (c) Pattern C: gaussian profile and uniform size. (d) Pattern D: gaussian profile and different size.

Fig. 5.13 shows the measured relative distance error. The number is averaged from 100 frames captured continuously by the sensor. The centroiding accuracy increases with the centroiding gain. It implies that higher centroiding gain leads to higher SNR in the star region, which in turn demonstrates higher centroiding accuracy. We tested different scenarios with various background levels for the proposed sensor. Even with high background level (2/3 signal swing), it still can achieve good centroiding accuracy at higher centroiding gain.

In addition, using the same lens system, the centroiding performance is also compared with a commercial CMOS image sensor Aptina MT9M032. We have calculated relative error under three different integration time. Each result is averaged from 100 captured frames. The comparison results of different patterns are summarized in Table 5.2, respectively. In all tested scenarios, MT9M032 shows relatively poor centroiding accuracy with short integration. The relative errors are above 1% when the integration is below

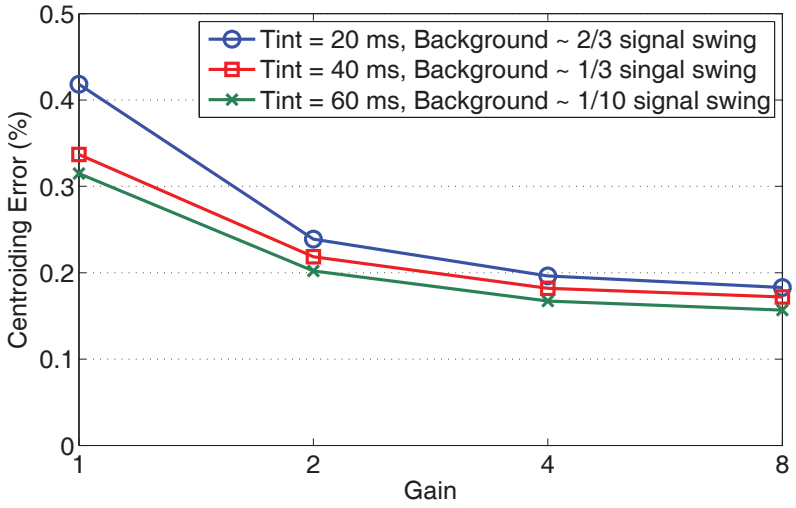


Figure 5.13: Measured relative distance error.

5 ms. When the integration is higher, it becomes comparable with the proposed sensor. It is primarily because MT9M032 utilizes 3T APS pixel structures which has a rather low sensitivity (2.1 V/lux-sec in monochrome mode). 5 ms is not enough for the pixel to collect enough charges to attain acceptable SNR. The proposed sensor has about 5 times better sensitivity and thus leads to better centroiding accuracy. The improvement is even large when higher centroiding gain is applied.

Table 5.3 shows the centroiding accuracy improvement with FPN cancellation. The FPN cancellation is performed by subtracting a dark reference frame. The dark frame which stores the digitized offset voltage is captured during calibration phase. It is averaged from multiple frames to eliminate the temporal noise. FPN has also effects on the centroiding error. Under all tested patterns, the centroiding errors decreases with FPN cancellation.

5.5 Conclusion

This chapter presents a smart CMOS image sensor for centroid measurement. To improve the centroiding accuracy, The proposed focal-plane algorithm and pixel architecture allow

"star pixels", pixels that are above a global star threshold, to cluster to create a local reference. The star signals are then amplified in relation to this reference. This increases the SNR in star regions in line with starlight intensity and regardless of background level. A proof-of-concept chip with a 128×96 pixel array was fabricated in a 0.35 μm mixed-signal CMOS process. Measurement results show that the device's centroiding accuracy increases with higher centroiding gain. Compared with a commercial image sensor, its relative centroiding performance with limited integration time is more than 1% higher.

Table 5.2: Centroiding accuracy comparison with Aptina MT9M032

Pattern A	Relative error [AB/BC-1]		
Integration	MT9M032	This sensor	
		Gain=1	Gain=4
3 ms	1.72%	0.63%	0.31%
5 ms	0.63%	0.52%	0.19%
10 ms	0.12%	0.14%	0.06%
Pattern B	Relative error [AB/BC-1]		
Integration	MT9M032	This sensor	
		Gain=1	Gain=4
3 ms	0.74%	0.73%	0.71%
5 ms	0.58%	0.48%	0.36%
10 ms	0.12%	0.12%	0.11%
Pattern C	Relative error [AB/BC-1]		
Integration	MT9M032	This sensor	
		Gain=1	Gain=4
3 ms	1.53%	0.39%	0.24%
5 ms	1.04%	0.18%	0.13%
10 ms	0.15%	0.12%	0.08%
Pattern D	Relative error [AB/BC-1]		
Integration	MT9M032	This sensor	
		Gain=1	Gain=4
3 ms	1.62%	0.42%	0.26%
5 ms	1.72%	0.34%	0.15%
10 ms	0.14%	0.15%	0.10%

Table 5.3: Centroiding Accuracy Improvement with FPN cancellation

Int. time	Pattern A	Pattern B	Pattern C	Pattern D
3 ms	-0.04%	-0.09%	-0.12%	-0.03%
5 ms	-0.04%	-0.09%	-0.02%	-0.02%
10 ms	-0.03%	-0.03%	-0.03%	0.00%

Chapter 6

Conclusion and Future Work

6.1 Concluding Remarks

The thesis investigates several design aspects of CMOS image sensors for star trackers. A star tracker must have radiation tolerance, high dynamic range and high SNR, both to survive in the radiation environment and to provide a high level of accuracy in terms of centroiding measurement. With this in mind, the thesis mainly focuses on exploring VLSI solutions to address these issues at different design levels.

The first work investigates radiation-tolerant pixel design, employing a variety of radiation hardening techniques as a countermeasure to the total ionizing effects. Four pixel variants were proposed, based on pinned photodiode 4T Active Pixel Sensors (APS). They varied primarily in the layout parameters of the photosensitive sites inside the pixel, making it possible to validate techniques and optimize design parameters for robust radiation hardness. The design and radiation characterization of these pixels is fully described. The pixels were characterized after the test chip had been irradiated by 60Co-rays up to 170 krad (Si). Our experimental results showed an increase in dark current and non-uniformity after radiation. The major cause of dark current increase was found to be the Enclosed Layout Transistor (ELT) transfer gate (TX). Dark current increase attributed to shallow trench isolation (STI) around the photodiode can be mitigated by a recessed-STI photodiode structure when the total dose is low. A large floating diffusion

(FD) capacitance shows more immunity to radiation-induced leakage current and random noise.

Secondly, two novel wide dynamic range CMOS image sensor architectures were proposed. The first featured the operating principle of adaptive integration time based on the concept of "saturation detection". This permits the integration voltage of each pixel to be cyclically sampled and checked in a row-wise manner during exposure. Bright pixels that quickly fell into the threshold window were therefore detected and read out first. Both sampling time and checked voltage were used to reconstruct the image. The most significant advantages of the new architecture were the reductions in its pixels complexity and size compared with those of their time-domain peers. Each pixel comprised just five transistors and had a small footprint and a large fill factor. As a result, it allowed high resolution integration while maintaining a dynamic range of over 120 dB. A multiple readout method corresponding to the sensor architecture was also proposed and devised, for the purpose of improving readout throughput and hence reducing the rolling period. The architecture is fully described and simulation proof, silicon implementation and chip measurement are discussed. The analysis showed that short integration time is preferable due to the dynamic conditions during star imaging, but is not preferable in terms of noise performance, which in turn, affects centroiding accuracy. A method is needed which allows both high sensitivity and high dynamic range. In another architecture, therefore, a CTIA pixel combined with a charge subtraction scheme method was proposed as a means of combining high sensitivity and high dynamic range in one pixel.

Thirdly, in search of high-accuracy centroid measurement solutions, a novel CMOS star sensor architecture was proposed. The new architecture was based on a focal-plane adaptive star region SNR improvement algorithm. Inter-connections between pixels were used to allow pixels that were above a global star threshold to cluster to create a local reference voltage, which was later used as the amplification reference for those pixels

during readout. This improved the SNR in the "star" region in line with the incident intensity transmitted. An adaptive region-of-interest readout architecture was also proposed, which reported star regions only, instead of the entire frame. The proof-of-concept chip was fabricated using a 0.35 μm CMOS mixed-signal process. The measurement results showed that centroiding accuracy increased with higher amplification gain. Within a limited exposure time, relative centroiding accuracy can surpass that of a commercial image sensor by more than 1%.

6.2 Future Research

The ongoing development of star tracker technologies continues to pose new challenges for CMOS image sensor design. The various design solutions discussed in this thesis all pursue high centroiding accuracy. The foremost important future research is to integrate the presented techniques, which are radiation tolerance, wide dynamic range and centroid measurement into one sensor. Radiation tolerance can be achieved straightforwardly by layout improvement at the expense of increasing the pixel size. Nonetheless, to achieve both high sensitivity and high-accuracy centroid measurement and wide dynamic range at the same time is nontrivial. One possible way of resolving the trade-off may be the CTIA pixel, thanks to its inherent high sensitivity and calculation capability: algorithms that extend dynamic range and algorithms that improve centroiding accuracy could thus be united into a single chip. In the quest for wide dynamic range solutions in these kinds of applications, one another interesting field of research remains. It is thought that a qualified star sensor can cover a dynamic range as wide as about 160 dB for different celestial bodies in the same scene.

Moreover, different process nodes are used to fabricated the sensors in the thesis. Among them, TSMC 0.18 μm CIS process demonstrates best sensitivity and noise performance thanks to optimized process parameters and specialized pixel devices. But they

are not suited for smart image sensors because of TSMC's constrain on the use of the devices in the pixel. AMS 0.35 μm CIS process, on the other hand, provides more flexibility while maintaining advantages of improved sensitivity. It is cost effective, which benefits from standardized CMOS process. Although the down size is that the pixel size would be normally larger due to large transistor feature size, it would not be of primary concern in space applications. AMS 0.35 μm CIS can be considered as best suited for future star sensor design.

Another possible avenue of future research would be to integrate more smart functions capable of recognizing star patterns: for example, the smart ROI windowing function, which can generate the ROI around star pixels and report the star region instead of reporting the entire frame, discarding redundant background data and facilitating the readout and processing of useful pixel values. Future research might also look at how two adjacent stars can be distinguished on a focal plane where some pixel responses are overlapped, or focus on hitherto unexplored functions, like star identification.

Publications

Patents

(1) Shoushun Chen, Kay Soon Low and **Xinyuan Qian**, "A High Dynamic Range CMOS Image Sensor System With Adaptive Integration Time and Multiple Readout Channels," filed with application number: US 13/946,567.

Journal Papers

(1) **Xinyuan Qian**, Hang Yu and Shoushun Chen, "A Global-Shutter Centroiding Measurement CMOS Image Sensor with Star Region SNR Improvement for Star Trackers," *accepted at IEEE Transactions on Circuits and Systems for Video Technology*, 2015.

(2) **Xinyuan Qian**, Hang Yu, Shoushun Chen and Kay-Soon Low, "A High Dynamic Range CMOS Image Sensor with Dual-Exposure Charge Subtraction Scheme," *IEEE Sensors Journal*, vol. 15, no. 2, pp. 661,662, Feb. 2015.

(3) **Xinyuan Qian**, Hang Yu, Shoushun Chen and Kay-Soon Low, "An Adaptive Integration Time CMOS Image Sensor with Multiple Readout Channel," *IEEE Sensors Journal*, vol. 13, no. 12, pp. 4931-4939, 2013.

(4) Hang Yu, **Xinyuan Qian**, Menghan Guo and Shoushun Chen, "An Anti-Vibration Time Delay Integration CMOS Image Sensor with Online Deblurring Algorithm," *accepted at IEEE Transactions on Circuits and Systems for Video Technology*, 2015.

(5) Vigil Varghese, **Xinyuan Qian**, Shoushun Chen, Zexiang Shen, Qijie Wang, Jin Tao and Guozhen Liang, "Track-and-Tune Light Field CMOS Image Sensor," *IEEE Sensors Journal*, vol. 14, no. 12, pp. 4372-4384, Dec. 2014.

Conference Papers

(1) **Xinyuan Qian**, Hang Yu, Shoushun Chen and Kay-Soon Low, "Design and Characterization of Radiation-Tolerant CMOS 4T Active Pixel Sensors," in *Proc. 14th International Symposium on Integrated Circuits (ISIC)*, Singapore, pp. 412-415, Dec. 2014.

(2) **Xinyuan Qian**, Menghan Guo, Hang Yu, Shoushun Chen and Kay-Soon Low, "A Dual-Exposure in-Pixel Charge Subtraction CTIA CMOS Image Sensor for Centroid Measurement in Star Trackers," in *Proc. IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, Okinawa, Japan, pp. 467-470, Nov. 2014.

(3) **Xinyuan Qian**, Hang Yu, Shoushun Chen and Kay-Soon Low, "An Adaptive Integration Time CMOS Image Sensor with Multiple Readout Channels for Star Trackers," in *Proc. IEEE Asian Solid-State Circuits Conference (A-SSCC)*, Singapore, pp. 101-104, Nov. 2013.

(4) **Xinyuan Qian**, Hang Yu, Shoushun Chen and Kay-Soon Low, "Design of a Radiation Tolerant CMOS Image Sensor," in *Proc. 13th International Symposium on Integrated Circuits (ISIC)*, Singapore, pp. 412-415, Dec. 2011.

(5) Hang Yu, **Xinyuan Qian**, Menghan Guo, Shoushun Chen, and Kay-Soon Low, "A Time Delay Integration CMOS Image Sensor with Online Deblurring Algorithm," in *Proc. International Symposium on VLSI Design, Automation and Test (VLSI-DAT)*, Taiwan, pp. 1-4, Apr. 2015.

(6) Hang Yu, Vigil Varghese, **Xinyuan Qian**, Menghan Guo, Shoushun Chen and Kay-Soon Low, "An 8-Stage Time Delay Integration CMOS Image Sensor with On-Chip Polarization Pixels," *International Symposium on Circuits and Systems (ISCAS)*, Lisbon, Portugal, May 2015.

(7) Vigil Varghese, **Xinyuan Qian**, Shoushun Chen and ZeXian Shen, "Linear Angle Sensitive Pixels for 4D Light Field Capture," in *Proc. 10th International SoC Design Conference (ISOCC)*, Busan, Korea, pp. 72-75, Nov. 2013.

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