A 64 × 64 Pixels UWB Wireless Temporal-Difference Digital Image Sensor

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***Abstract*—In this paper we present a low power temporal-difference image sensor with wireless communication capability designed specifically for imaging sensor networks. The event-based image sensor features a 64 × 64 pixel array and can also report standard analog intensity images. An ultra-wide-band radio channel allows to transmit digital temporal difference images wirelessly to a receiver with high rates and reduced power consumption. The sensor can wake up the radio when it detects a specific number of pixels intensity modulation, so that only significant frames are communicated. The prototype chip was implemented using a 2-poly 3-metal AMIS 0.5 μm CMOS process. Power consumption is 0.9 mW for the sensor and 15 mW for radio transmission to distance of 4 m with rates of 1.3 Mbps and 160 fps.**

***Index Terms*—CMOS image sensor, motion detection, temporal-difference, ultra-wide-band (UWB), wireless sensor network.**

I. Introduction

DESPITE the tremendous progress in CMOS image sensor design and wireless communications recently, the integration of wireless video sensor network remains a challenge. The limited energy capacity and extended lifetime requirements demand that all aspects designed in low power fashion. Simple estimation shows that in order to have a couple of AA batteries last about two weeks, the sensor node is constrained to consume power no more than 10 mW. In an image sensor network, the operation of an imager node consists in image sensing, local data processing and wireless transmission. To extend the battery life, in addition to the power minimization of the imager itself [1], [2], special efforts should be aimed at reducing the power consumed during the wireless data transmission. This further translates into the requirements of reduced amount of data and energy-efficient wireless communication protocol. Smart image sensors must be employed in order to abstract meaningful information out of the raw image data. At the same time, there is trade-off between a variety of design parameters such as imager resolution, complexity of on-chip image processing, data encoding strategy (sequential scanning or asynchronous address event (AE) [3]–[5] and communication protocol (Zigbee, Bluetooth, or UWB):

- To avoid communication of raw data over wireless channels, on-chip image processing must be employed. Many image processing are computation and memory intensive tasks. Energy efficiency is the primary concern on the choice of processing. For instance, in terms of image compression [6]–[9], though discrete cosine transform (DCT) and wavelet transform (WT), among various block transforms, are popular in image/video compression standards such as JPEG, MPEG, H.261, and H.263. However, implementation of these transforms on-chip with the sensor is expensive in both power and silicon area. In addition to image compression, a variety of on-chip image processing have been reported, such as contrast extraction [10], [11], motion vector estimation [12], histogram equalization [13], etc. In this work, we chose motion detection due to its wide applications in surveillance, traffic control and environmental monitoring. A motion sensor can be used a trigger and wake up the other devices when there are movements. Recently, a number of low power imagers with focal plane motion detection have been proposed [14]–[16].
- In the selection of data encoding strategy, trade-offs should be taken among scanning and asynchronous address event readout approaches. In [16], each pixel independently and in continuous time quantizes local relative intensity changes to generate spike events. Pixel events are queued and wait their turn for access to a shared arbitrated bus and appear at the output as an asynchronous stream of digital pixel addresses (15 bit/pixel), known as address events. In [11], the sensor performs on-chip contrast extraction and off-chip temporal detection. Pseudo-asynchronous row-based raster scan approach is employed and each address event is represented by a 7-bit column address and 1-bit additional information such as end-of-row, end-of-frame. In this image sensor, we used a sequential scanning readout scheme rather than asynchronous address event (AE) to reduce the bandwidth requirement. This design choice is derived from the number of bits required to represent each event, which is 1 using scanning approach while 13 using AE format, for a 64 × 64 imager. When significant percentage $(1/13 = 7.7\%)$ of pixels in the scene are triggered, larger bandwidth will be

required using AE approach. The percentage threshold will be lower when the resolution of the imager grows.

- Power efficiency and bandwidth are the major criteria to choose a wireless communication protocol. The event rate of a temporal motion detector in this design requires 1–10 Mbps data rate while the power consumption should be at ∼10 mW level. UWB is drawing much attention from both academia and industry. Its performance in low power and high speed in short range wireless communications makes it the ideal candidate. Other wireless technologies, such as bluetooth (v2.0) with less than 2 Mbps practical data rate or WiFi with hundreds of mW power consumption, are not appropriate in the battery powered wireless image sensor application. There are three kinds of UWB system: MB-OFDM UWB, coherent impulse radio (IR) UWB, and non-coherent IR UWB. Compare to MB-OFDM UWB and coherent IR UWB technology, the non-coherent IR UWB system is more attractive to the wireless image sensor system to avoid the need for complex synchronization blocks and incoming pulse shape estimation [17]. Though the transmission data rate of non-coherent UWB (10–20 Mbps) [18] is lower than MB-OFDM UWB (100 Mbps) [19] and coherent IR-UWB (50 Mbps) [20], it is enough for the application in the smart image sensor system. Moreover, without template pulse generator and quadrature frequency synthesizer, the transmission unit is able to enter into sleep mode during a large percentage of the operation [21]. This will significantly reduce the system power consumption by taking advantage of the low duty-cycling property of temporal difference sensor output.

With the above considerations, we designed and fabricated a wireless image sensor that captures compressed motion-based temporal difference digital images, and is capable of wireless data transmission by means of an ultra-low power, high-bandwidth radio based on ultra-wide-band (UWB) pulse radio communication. The sensor was implemented using a 2-poly 3-metal AMIS 0.5-μm CMOS process. It performs temporal-difference calculations between two frames, while continuously monitoring for photocurrent changes. Each pixel responds with a binary event that represents whether a fractional increase/decrease in intensity that exceeds a tunable threshold (ONE) or not (ZERO). Therefore, moving objects (ONE pixels) can be easily identified out of the static, whatever complicated background (ZERO pixels). In the next stage, the binary event stream is modulated by the Manchester Encoder and UWB transmitter. The wireless data link is based on a non-coherent UWB impulse radio.

The main innovative contribution of this work is the seamless integration of a motion detection sensor and ON/OFF keying UWB radio, enabling a custom low power and high frame wireless sensor node for applications such as assisted living monitors, security cameras and robotic vision. A short version of this paper was first reported in [22]. The rest of this paper is organized as follows. Section II introduces the system architecture, pixel design and temporal difference event generation. Section III describes the wireless data transmitter design.

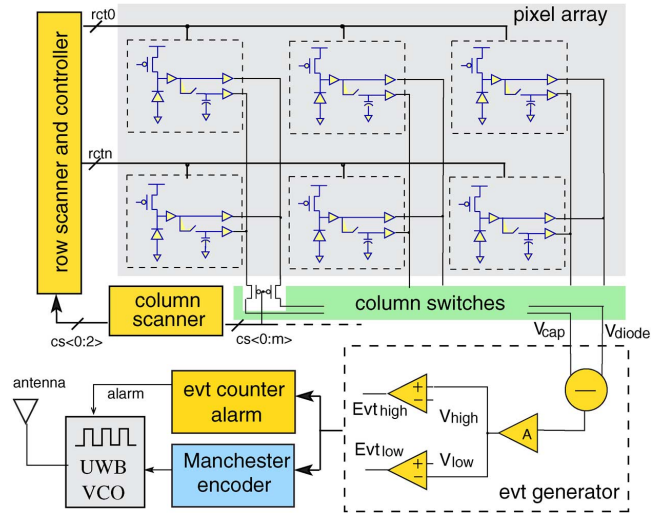

Fig. 1. Block diagram of the wireless image sensor.

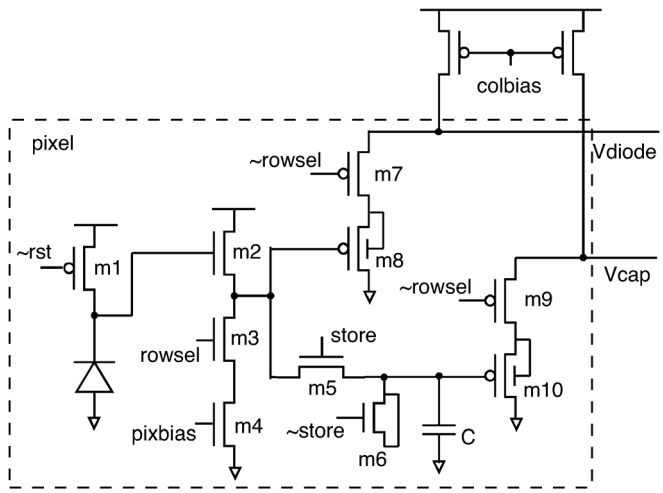

Fig. 2. Schematic of the pixel.

Section IV reports the experimental results and Section V concludes this paper.

II. Temporal Difference Imager

A. Imager Architecture

Fig. 1 reports the system diagram of the autonomous sensor. Main building blocks include an array of 64 × 64 pixels, global event generator, Manchester encoder, UWB transmitter, row and column scanners. Each pixel is equipped with an analog memory (capacitor) and the whole array is hence capable of storing the current frame as a reference image. The rows are first sequentially selected for reset. Later at another round of scanning, the rows of pixels are selected for readout sequentially. Each pixel will output both the new integration voltage on its photodiode and the previous voltage stored on its capacitor. The two voltages are fed into an global event generator circuit which is composed of a global amplifier with a temporal-difference computation circuit based on dual comparison. The event generator computes the difference between the two voltages, and compares it to a positive and negative threshold. A digital event

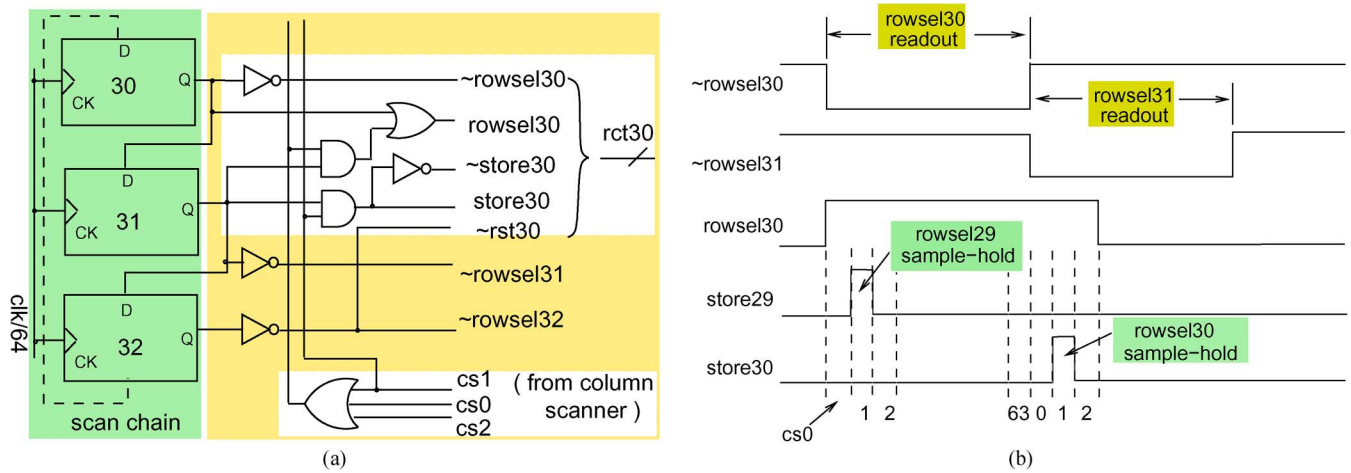

Fig. 3. (a) Row scanner architecture. A set of control signals are produced for each row, rct30 for row30 in the figure. The scanner output is directly used to select the row for readout while the other signals can be generated by cross-coupling from other rows. cs0–cs2 are column selection signal for the first three columns. (b) Example timing diagram. Row31 is selected for "readout" after row30 is finished. In parallel with that, row30 enters into the "sample-and-hold" mode, but only during the second cycle.

is generated if this difference exceeds the thresholds. The event bit stream together with the clock are first encoded by a Manchester encoder circuit. The encoded digital code is converted into an impulse sequence in the UWB transmitter.

A simple but efficient wireless power saving scheme is built in the imager. An on-chip 12-bit counter monitors the number of events per frame and will generate an "alarm" signal when that number exceeds a programmable threshold. Only when the "alarm" signal is triggered, the UWB transmitter circuit will be enabled to transmit the events of the next frame. Most of the time, the wireless part is in standby mode, saving power. Bias voltages are internally generated and are used to operate the sensor. No external biasing DAC are needed.

B. Pixel Design and Readout

Fig. 2 shows the block diagram of the proposed pixel. Each pixel includes a photosensitive element (photodiode), a reset transistor (m1), a source follower (m2–m4), a sample-and-hold path composed of (m5, C), and two sets of readout circuits (m7–m8, and m9–m10). Transistor m3 is used as a power saving device to turn OFF the source follower path when the pixel is not selected for any operation. P-type MOS transistors are used in the readout source follower circuits (m7–m8, and m9–m10) to compensate the DC level shift due to the N-type source follower (m2). They are fabricated in dedicated N-Wells with bulk voltage tied to the source nodes to reduce body effect.

The pixel's operation follows a sequence of "reset", "integration", "readout", "sample-and-hold", "reset". First, a "reset" operation is performed and transistor (m1) is turned ON, initializing the photo detector to the power supply voltage. Then transistor (m1) is turned OFF and the "integration" phase starts. At the end of the "integration" phase, the pixel is selected for "readout" by the ($\sim$ rowsel) signal. Both the new integration voltage on the photo detector and the stored voltage on the capacitor will be read. After that, a "sample-and-hold" operation will be performed: transistor (m5) will be turned ON, and the current integration voltage will be stored on the capacitor, overwriting the old value.

The "reset", "integration", "readout", "sample-and-hold" operations can be described as a row-based rolling shutter. Fig. 3(a) shows how the control signals are generated. In the sensor, there are two sets of scanning chains: row-wise and column-wise. The column-wise scanner is driven by a clock 64 times faster than that driving the row scanner. Each node of the row scanning chain directly produces the control signal ($\sim$ rowsel) for one row, which will initiates the "readout" process. All of the pixels in the row will output their voltages to the column bus. The column scanner then switches the multiplexers from one column to another. After all the pixels are readout, the capacitors in the current row can be written into new value, i.e., "sample-and-hold" operation. This happens at the moment when the row scanner selects the next row for "readout". However, special care should be taken to control the ON/OFF sequences of the control signals. It should be noted that, in the pixel both transistors (m3 and m5) should be ON to enable the "sample-and-hold" path. They can be turned ON simultaneously, but must be turned OFF at a different time. Turning OFF transistor (m3) before (m5), will introduce some charge loss from the capacitor (C) due to the malfunction of the source follower (m2–m4). In order to avoid this, we propose to perform "sample-and-hold" operation only for a very short period. Transistor m3 is activated only for the first three cycles while transistor m5 is turned ON only at the second cycle. This is illustrated in an example timing diagram of Fig. 3(b). The control signal for m3 (rowsel30) is active not only during the 64 cycles when the 30th row is selected for readout, but also during the first 3 cycles when the 31rst row is readout. This is because the source follower (m2–m4) needs to be enabled for successful "sample-and-hold" operation for the 30th row. During those three cycles, the store30 signal, is activated only at the moment of $\mathrm{column\_address} == 1$. The implementation of this control scheme is illustrated in Fig. 3(a). The select signal for the first three columns together with the row scanner can produce all the control signals.

Efforts were made to reduce the noise generated by the switches (m5 and m6) to the capacitor (C). Transistor m6 is

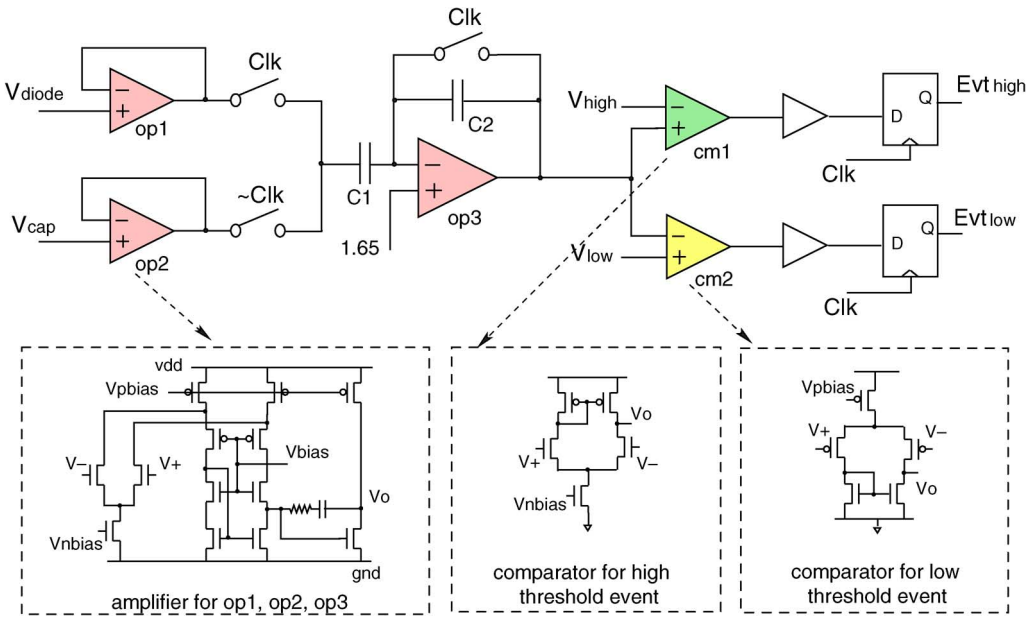

Fig. 4. Event generation circuits with detailed diagram for each the building block. The operational amplifiers op1–op3 are based on the same architecture but designed with different gain-bandwidth product for different loading and speed requirement. In order to cover the full voltage swing, the comparator for high/low threshold comparison has nMOS/pMOS input stage, respectively.

employed as a charge injection cancellation device for m5. The rise/fall time of store and ∼store is intentionally slowed down [23] by properly sizing their drivers. This can reduce the feed-through due to coupling between these two signals and the anode of the capacitor (C).

One may also note that, in "readout" operation the pixels are selected in a column by column manner while in "sample-and-hold" and "reset" operation the whole row of pixels are selected in parallel. This is due to the absence of column selection switches in each pixel, which leads to reduced pixel area and column bus routing resource, but at the expense of minor column-wise integration time mismatch.

C. Event Generation

The two pixel output voltages, one from the photodiode $(V_{\rm diode})$ and the other from the cap $(V_{\rm cap})$, are copied onto two column-wise buses and their difference is computed. As shown in Fig. 4, the mixed-signal temporal differencing unit [24] is composed of four stages: 1) unity gain buffer; 2) switched-capacitor-based AC differentiator; 3) comparator; and 4) digital signal sampling circuits.

The closed loop gain of the switched-capacitor differentiator is $A = C2/C1$. The AC amplifier computes the difference of the two signals and amplifies it by $C2/C1$. The operational amplifiers op1–op3 are based on the same architecture but designed with different gain-bandwidth product. The overall current consumption of the event generation unit is about 160 μA. op3 is designed with the largest output current due to larger capacitive loading at the output ($C2 =\sim$ 1 pF). The output signal from the differentiator, centered around $(vdd/2)$, will then be compared with two tunable threshold voltages $(V_{\rm high})$ and $(V_{\rm low})$. In order to cover a large voltage swing, nMOS and pMOS comparators are used to accept high and low dc voltage, respectively. The

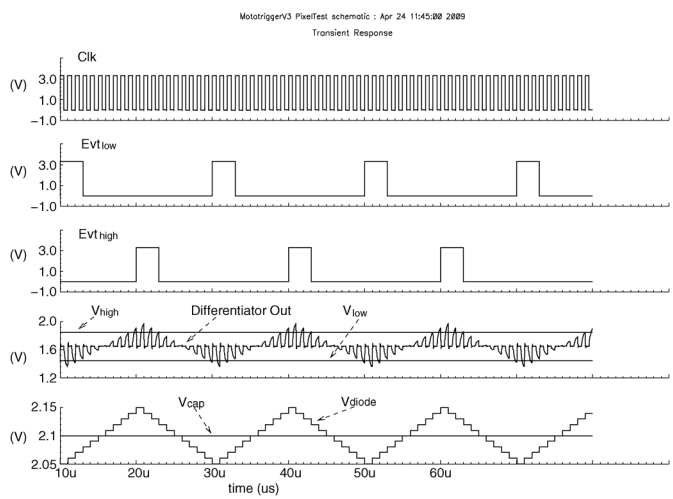

Fig. 5. Event generation simulation example.

comparison results are finally sampled by digital flip-flops and turned into digital events $(Evt_{\rm high}, Evt_{\rm low})$.

Fig. 5 shows the timing diagram of the temporal difference unit. In the simulation, the voltage on the capacitor $(V_{\rm cap})$ is assumed to be constant and the voltage on the diode $(V_{\rm diode})$ is modeled by a stair function. To model the pixel array's operation, the transition of the voltage on the diode is synchronized to the clock (Clk). The output of the switched-capacitor AC amplifier is centered at the reference of 1.65 V, and the two comparators $(cm1, cm2)$, thresholds $(V_{\rm high}, V_{\rm low})$ are symmetrically programmed around this reference. When the output voltage, is higher than $(V_{\rm high})$ or lower than $(V_{\rm low})$, the two corresponding comparator will be triggered and digital events $(Evt_{\rm high}, Evt_{\rm low})$ are produced.

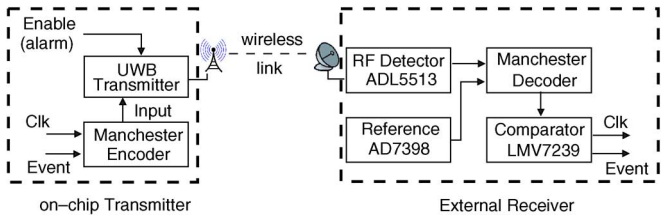

Fig. 6. Building blocks of the wireless data link of the whole system, including clock and data encoding, pulse modulation, pulse detection, clock, and data recovery.

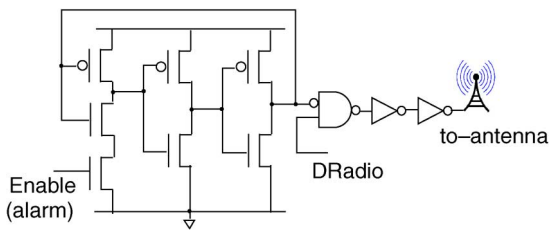

Fig. 7. Schematic of integrated UWB transmitter. A voltage controlled oscillator generates impulse to the output according to the ON/OFF keying modulation.

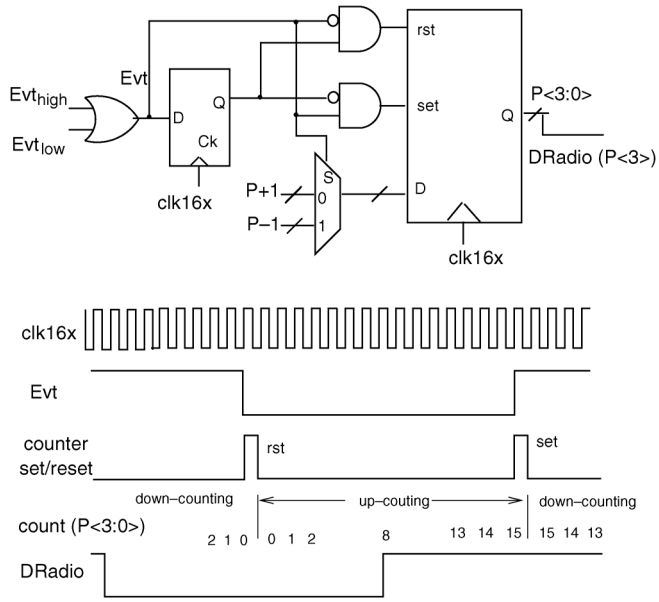

Fig. 8. Manchester encoder and timing diagram. The counter is driven by a clock 16× faster than the input event data and its MSB bit is directly tapped as the encoding output. The code bit has a high-to-low transition when $Evt = 1$, and low-to-high transition when $Evt = 0$, respectively.

III. UWB Wireless Transmission

Fig. 6 shows the building block of the wireless data link for the sensor, which contains clock and data encoding, pulse modulation, pulse detection, clock and data recovery. The integrated transmitter first feeds the event bit stream and clock into the Manchester encoder circuit. The encoded digital signal is converted into an impulse sequence in the UWB transmitter. At the receiver side, a commercially available RF detector (ADL5513) reconstructs the energy envelope from the impulse sequence, and then the output is compared with a tunable threshold voltage. The digital output from the comparators is connected to a Manchester decoder, which will recover the event bit stream and clock. Frame synchronization between the transmitter and receiver is implemented by the insertion of a dummy row of pixels embedded with a special pattern of event data.

The transmitter generates impulses using a voltage controlled oscillator and operates in the ON/OFF keying mode [25]. The transmitter circuit is shown in Fig. 7. The frequency control terminal to the VCO, denoted as "Enable", is now a digital signal which can switch the VCO to fully geared or off. When the VCO works ("Enable" $= 1$), a high input bit will send a burst of impulses to the external antenna. The minimum pulses duration is 10 ns, which is determined by the turn-on and turn-off response time of the VCO. One can note that the transmitter can be set to standby mode and consume no power. It is only active when significant amount of motion pixels detected, by the alarm generator.

In order to reconstruct frames out of the event bit stream, two levels of synchronization are performed. First, in order to identify the start/end pixel of each frame, a row of dummy pixels are built as the last row of the array. A dummy pixel with V_{DD} on its diode node and V_{SS} on its capacitor node will produce an event of "1" under whatever illumination and motion conditions. While one dummy pixel with its diode and capacitor nodes shorted will always produce an event of "0". Therefore this row of dummy pixels can be embedded with a fixed, special pattern of event data. The start/end pixel can then be easily found by searching for the special pattern from the bit stream. Secondly, in order to achieve each single bit of clock and data recovery over the wireless link, Manchester encoding is employed, due to its low cost and simplicity. After encoding, each code bit will have at least one transition and occurs at the same time. Fig. 8 shows the design of the Manchester encoder. The main building block is a 4-bit up/down counter, which is driven by a 16× faster clock. The counter works as a counter or decounter depending on the input event data (Evt). By reset/set the counter can change the operation mode each time when there is transition in the event bit stream. Therefore, the MSB bit will have a high-to-low transition when $Evt = 1$, and low-to-high transition when $Evt = 0$, respectively.

IV. Experimental Results

The prototype chip was implemented using a 2-poly 3-metal AMIS 0.5μm CMOS process, on a 3×3 mm^2 die. Fig. 9 shows the chip with all building blocks highlighted. The pixel contains 10 transistors and a MOS gate capacitor. pMOS reset transistor is employed for higher photodiode voltage swing but must be implemented in a separate N-Wells. Between the two N-Wells, the photodiode's N+ diffusion is geometrically designed to be as square as possible to reduce the junction perimeter to minimize the dark current [26]. P+ guard ring is employed around the photodiode. Each pixel occupies an area of 33×33 μm^2 with a fill-factor of 11.5%. The wireless part, which includes the UWB VCO and Manchester encoder, only occupies a very small footprint of 140×85 μm^2.

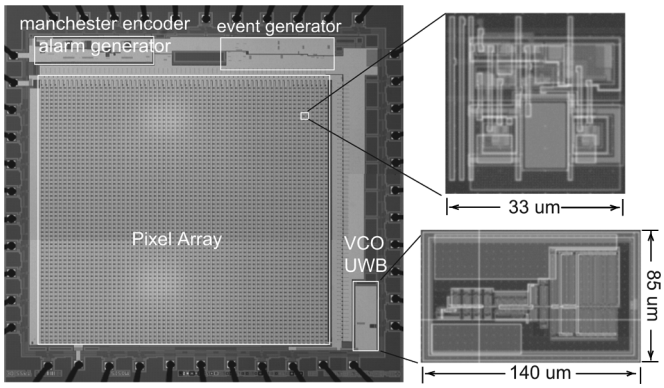

Fig. 9. Microphotography of the chip with main building blocks highlighted.

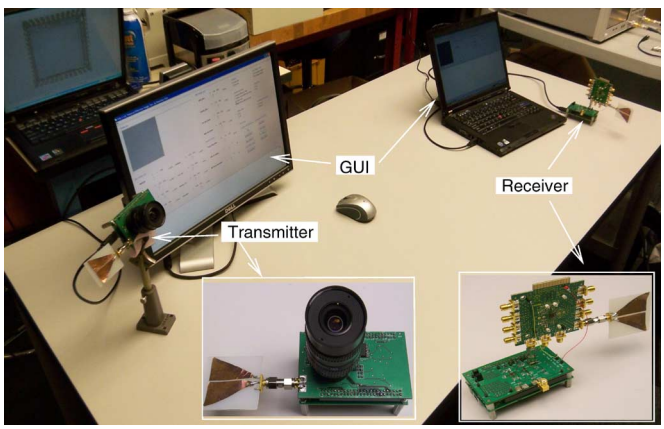

Fig. 10. Experimental setup of the whole system including transmitter and receiver.

A testing platform, as shown in Fig. 10, including both the wireless sensor (transmitter) and a receiver was developed. At the transmitter side, the sensor was interfaced with an Opal-Kelly XEM 3001 FPGA board. The FPGA is configured to provide input control signals, temporarily store the baseband data and communicate with a local host PC through USB link. At the receiver side, wireless pulses are first processed by an Analog Device ADL5513 Logarithmic RF detector, and then turned into a stream of digital bits by means of a comparator. Further baseband processing such as Manchester decoding and frame synchronization was done using another FPGA board. At both sides, the system utilizes a graphic user interface to control the bias voltages and transmission data rate. The sensor is able to operate at dual modes: normal intensity mode and temporal difference mode. Intensity mode is mainly designed for calibration purpose and therefore an on-board 12-bit ADC (AD7476) is used. At this mode, the sensor must use external clock to synchronize the ADC and the on-chip scanner. The photodiode dark current was measured to be around 7.84 fA based on the estimated photodiode capacitance (∼67 fF). Fixed pattern noise (FPN) was 3.83 mV when running at 80 fps. At temporal difference mode, the chip will operate autonomously. The power consumption of the sensor alone is only 0.9 mW, while the UWB radio consumes 15 mW when operating at 160 fps and 1.3 Mbps.

To save wireless power, we propose to turn on the UWB radio only when significant amount of motion events are detected

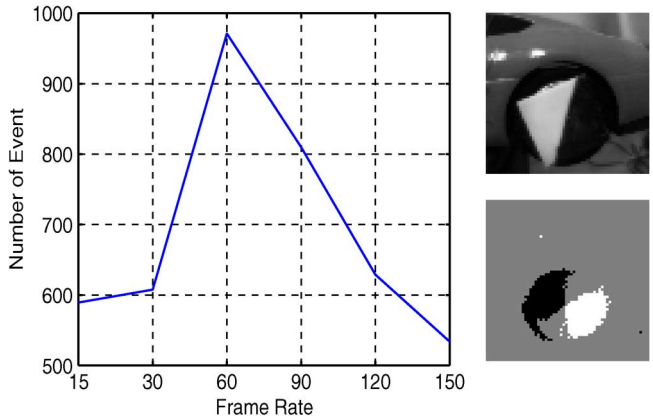

Fig. 11. Measured average number of events per frame with a spinning plate, with respect to different frame rate. The plate has a fixed spinning speed around 30 round-per-second.

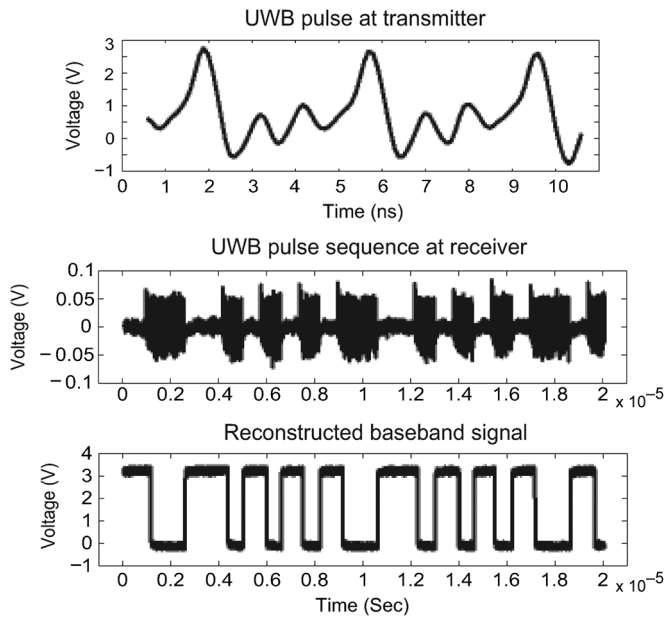

Fig. 12. (top) UWB pulse waveform at transmitter with 270 MHz pulse repetition rate. (middle) Encoded pulse sequence with 1.3 Mbps data rate at transmitter. (bottom) Reconstructed digital waveform at receiver.

by an programmable counter. In fact, however, the number of events per fame depends on a few operational conditions, such as object type, size and distance, motion speed and direction, frame rate, light condition, threshold voltage of the event generator. In this work, the threshold value is manually calibred. A future improvement direction is to enable a scheme to set the threshold adaptively. Fig. 11 reports the measured number of events per frame with an example spinning object, respect to different frame rate. The measured number reaches the peak when the frame rate is half of the spinning speed, due to aliasing effect. This in fact presents an intrinsic band-pass characteristic of the frame-based temporal difference algorithm: changes that happen faster than the frame-rate, can get lost and also changes that happen slower than the chosen frame-rate, may get lost. On the contrary, in [16] each pixel continuously monitors illumination change and asynchronously encodes the voltage transition

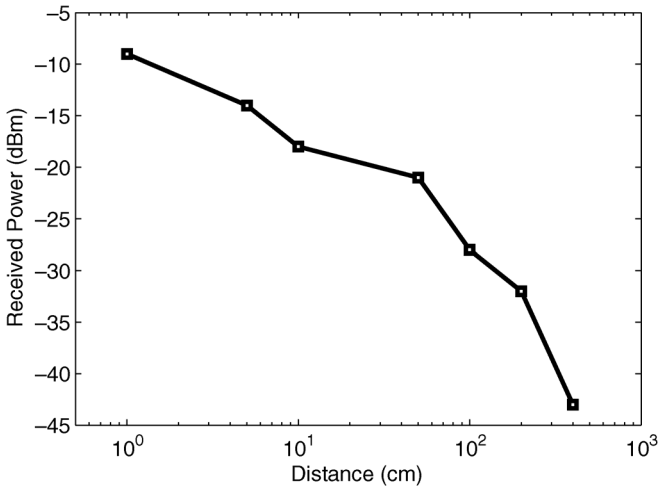

Fig. 13. Received radio power versus the distance between TX and RX antenna.

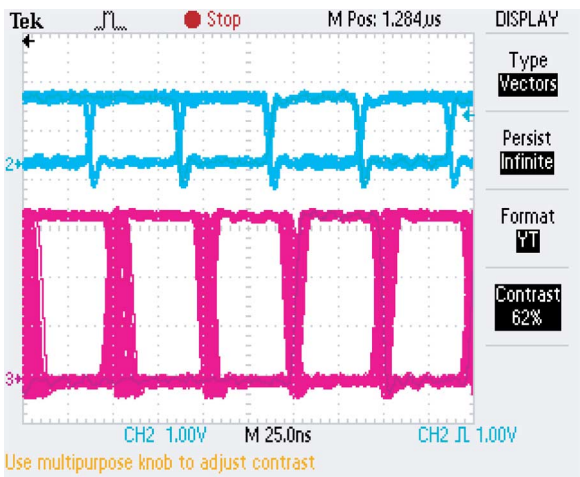

Fig. 14. (top) Transmitted and (bottom) received baseband data with data rate of 20 Mbps. Vertical scale: 1 V/div; horizontal scale: 25 ns/div.

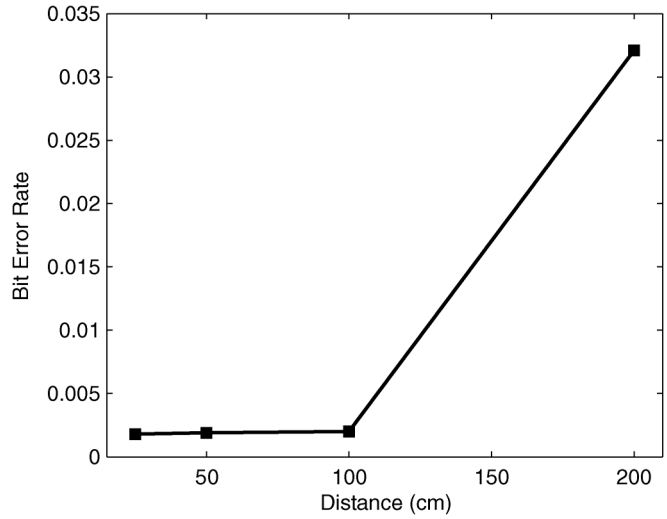

Fig. 15. Measured BER versus transmission distance. In the experiment, the data rate is 10 Mbps.

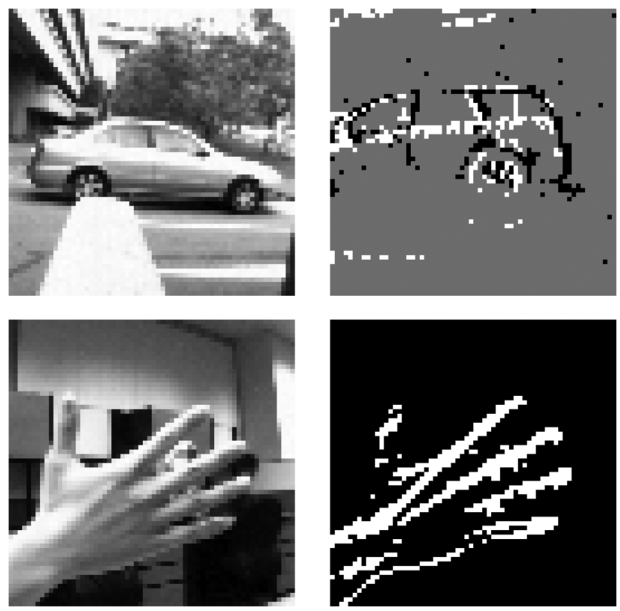

Fig. 16. Sample pictures captured in different environments. Top: normal intensity and baseband differential image, outdoor, 20 k lux, 100 fps. Bottom: normal intensity and wireless differential image, indoor, 400 lux, 30 fps. In the baseband differential image background pixels are in gray color, while brighter (evt_{low}) and darker (evt_{high}) motion pixels are in white and black color, respectively. In the wireless differential image both type of motion pixels are in white color.

into digital events. This will remove the aliasing effect, however, loss of intermediate events still happens due to the delay in processing the concurrent events by time-multiplexing a single output bus.

The wireless data link is then characterized. The transmitted pulse waveform and reconstructed digital waveform are shown in Fig. 12. The wireless link is using sub-GHz UWB band. The transmitted energy level is below -40 dBm to meet the FCC mask of UWB impulse radio system. At the receiver side, we measured the received power as a function of the distance between antennas, as shown in Fig. 13. It is converted from the output voltage to received power according to the ADL5513 data sheet. A commercial -80 dBm wide-band RF power detector can receive the signal from our UWB transmitter over 4 m distance. Fig. 14 shows the eye diagram with 20 Mbps data rate. Fig. 15 shows the bit error rate (BER) measured result with transmission distance at 10 Mbps. The BER increase with distance because of the multi-path and fading. The BER drops when either the data rate or distance reduces. At the distance of 2 m, the reliable data rate is 2 Mbps. While at the distance of 4 m, the system works fairly robust at a reduced data rate of 1.3 Mbps.

Fig. 16 reports a few sample images from the wireless sensor, two temporal difference images, and two intensity images, one of each is taken under normal office light condition (400 lux) and outdoor sunny day light condition (20 k lux). The motion images are noisy, especially in the outdoor environment. This is indeed limited by the temporal difference algorithm itself. This scheme compares two consecutive image frames and outputs those pixels whose illumination changes by an amount larger than a predefined threshold. It is specialized in rejecting static background and is intended for indoor usage. For outdoor, the

TABLE I
PERFORMANCE SUMMERY AND COMPARISON OF THE PROPOSED SENSOR WITH OTHER WORKS REPORTED IN THE LITERATURE [16] AND [27]

	[27] ISSCC'05	[16] JSSC'08	This Work
Functionality	temporal difference	temporal difference	wireless temporal difference
Technology	0.5μm 3M 2P	0.35μm 4M 2P	0.5μm 3M 2P
Array Size	90×90	128×128	64×64
Pixel Size	25.2×25.2 μm^2	40×40 μm^2	33×33 μm^2
Pixel Fill Factor	17%	8.1%	11.5%
FPN	0.5%	2.1%	0.2%
Readout Strategy	sequential scan	asynchronous AER	sequential scan
Max Frame Rate	30fps	not available	160fps
Data Rate	243k event/s (1 bit/event)	∼1M event/s (15 bit/event)	640k event/s (1 bit/event)
Supply Voltage	3 V	3.3 V	3.3 V
Power Consumption	4.3 mW@30fps	24 mW	sensor 0.9 mW (speed insensitive) UWB 15 mW (@160fps, 1.3Mbps(clock+data))

motion image can be unacceptably worse when there is wind or the background moves too much. Even indoor, light intensity can vary by ten times or more. In order to compensate different lighting intensities, the autonomous on-chip threshold generation will be essential.

Table I summarizes and compares the performance of the proposed imager with other devices reported in the literature [16] and [27].

V. CONCLUSION

We report a proof-of-concept design of a single chip event-based CMOS image sensor with low complexity wireless communication capability. The sensor is capable of delivering frame-differencing (motion detection) at the focal-plane, while consuming less than 1 mW power. On chip UWB wireless radio consumes 15 mW when operating at 160 frames/s and 1.3 Mbps. Low power was achieved by seamless integration of the image sensing, motion detection, clock/data/frame encoding and synchronization, and UWB wireless transmission. In particular, the wireless link can turn to standby mode when there is little motion in the scene. It can be reactivated when the on-chip alarm generator detects enough motion that exceeds a programmable threshold. Therefore the sensor can serve as an ultra-low power trigger to external high-resolution cameras for taking timely snapshots. The proposed design is an ideal candidate of wireless sensor network node, for applications such as assisted living monitors, security cameras and even robotic vision. Future improvements include the integration of error correction encoding, autonomous threshold voltage adaption and the translation to deeper submicrometer fabrication process.

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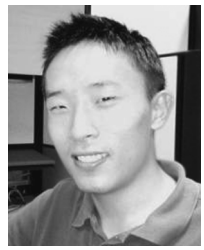

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