

A Compact Reconfigurable Counter Memory for Spiking Pixels

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Abstract—In this letter, a compact reconfigurable counter memory (RCM) is proposed for spiking pixels. In contrast to conventional in-pixel counter circuitry, the proposed RCM does not rely on a flip-flop-based circuit but instead uses a very novel circuit structure that combines a combinational incrementer together with static and dynamic memory cells. The proposed RCM provides counting as well as in-pixel storage functionalities allowing for intermediate readout of digital pixel values. Reported experimental results validate the novel concept of RCM-based spiking pixel in AMIS 0.35- μm CMOS technology. The proposed pixel architecture is inherently insensitive to power supply voltage scaling and is thus well suited to submicrometer CMOS processes.

Index Terms—CMOS imagers, dynamic range, fill factor, spiking pixel.

I. INTRODUCTION

IN recent years, we have seen the rapid emergence of CMOS imaging technology as the technology of choice for portable digital imaging products [1]. It is the use of the semiconductor industry standard CMOS fabrication process that has enabled the concept of a CMOS imager, i.e., camera on chip, resulting in reduced manufacturing costs, compactness, and low-power operation [1]. Furthermore, the use of a CMOS-compatible imaging technology enables the integration of signal processing circuits at the pixel level to improve the quality of the acquired image or to implement specific machine vision tasks, such as edge detection or motion detection. Digital pixel image sensors (DPS), which integrate a pixel-level analog-to-digital converter (ADC) [2], benefit from the ongoing technology scaling with an improved fill factor [3]. However, as new technological process solutions are being introduced to define increasingly smaller patterns, power supply voltage is seen to drop with device scaling from typically 5 V in a 0.7- μm standard CMOS process down to currently 1.2 V in a deep submicrometer 0.13- μm CMOS process. This continuous reduction in supply voltage, in turn, limits the available analog signal swings, degrading the sensor signal-to-noise ratio (SNR) as well as the achievable dynamic range. Spiking pixels, also referred to as pulse-modulated pixels, can ensure a relative insensitivity to the ongoing aggressive reduction in power supply, which is ex-

pected to continue for the next generation of deep submicrometer silicon processes [1]. A spiking pixel is a light-controlled oscillator, which encodes illumination information into a stream of spikes or pulses [4]. The brightness value for a spiking pixel can be obtained by simply counting the number of pulses generated during a fixed period of time. Under constant illumination conditions, the pulse count is directly proportional to the incident light. In addition to a linear characteristic, the spiking pixel can provide a very high intrascene range if the in-pixel counter resolution is increased. Unfortunately, building DPS based on a spiking pixel architecture requires implementing both a counter and a memory at the pixel level, resulting in a degraded fill factor and a large pixel area. In this letter, we propose a compact reconfigurable counter memory (RCM) for spiking pixels. In contrast to conventional in-pixel counter circuitry, the proposed RCM is not based on a silicon area consuming flip-flop circuitry, which degrades fill factor dramatically (e.g., 0.5% for a pixel size of $50 \times 50 \mu\text{m}$ in [5]). Instead, the proposed counter memory combines a combinational incrementer and static and dynamic memory cells to achieve better compactness while still providing in-pixel memory functionality.

In the next section, the proposed RCM, together with the architecture and operation of an RCM-based spiking pixel, is presented. Experimental results are reported in Section III. Finally, concluding remarks and perspectives are given in Section IV.

II. RCM SPIKING PIXEL

The proposed RCM is shown in Fig.1(a). It combines a combinational incrementer, an 8-bit SRAM (bits B0–B7), and an 8-bit DRAM (bits A0–A7). The RCM circuitry has two functions, namely: 1) counting the number of incoming spikes or pulses Clk and 2) storing the digital pulse count value. The RCM operates as follows [Fig. 1(b)]. Each time a spike or pulse is detected (Clk high), pulse count X is updated ($X = X + 1$) in the SRAM by incrementing the previous pulse count stored in the dynamic memory cell. This is achieved through the XOR gates of the combinational incrementer. At the end of the pulse (Clk low), the updated pulse count is latched back into the dynamic memory cell. Note that in the proposed operation scheme, the static and dynamic memories remain connected when Clk is low. This means that simple capacitors can be used to store the previous pulse count (A0–A7), which is, in turn, fed back to the combinational incrementer. The storage capacitors are only kept floating for Clk high, which corresponds to a very short period of time in the case of a spiking pixel because of

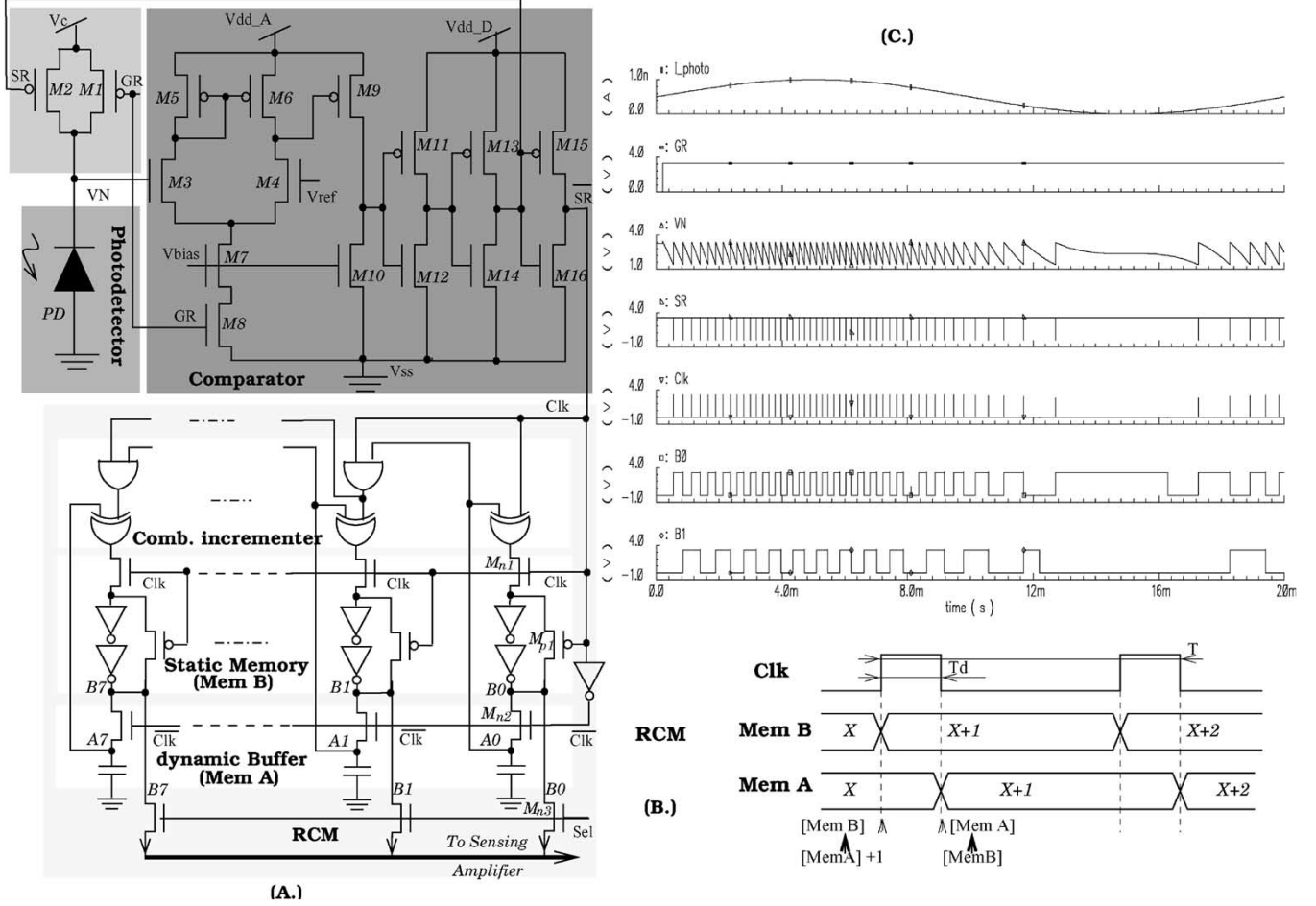


Fig. 1. RCM-based spiking pixel: (left) architecture and (right) simulation results.

its feedback architecture. As a result of the proposed operation scheme, a robust dynamic memory cell can be implemented by means of simple capacitors (Fig. 1), leading to improved compactness.

An RCM-based spiking pixel [Fig. 1(a)] comprises a reverse-biased photodiode PD, a reset circuit (M1–M2), a comparator (M3–M10), and a CMOS inverter delay chain (M11–M16). The operation of the RCM-based spiking pixel can be described as follows. Initially, the photodiode is reverse biased with the voltage at the sensing node $V_N = V_C$. The illumination pulse encoding process is triggered by an external control signal GR, which enables the comparator and causes the photodiode to be floating. Next, photo-generated electron–hole pairs are collected, causing a decrease of the voltage V_N at the sensing node. When V_N reaches the reference voltage V_{ref} , the output of the comparator goes high, driving the voltage at the sensing node back to V_C through the reset transistor M2. The CMOS inverter delay chain (M11–M16) ensures that the photodiode is reset back to V_C before the output SR goes low and the reset transistor M2 is turned off. As a result of this self-reset operation, a pulse is generated at the output SR each time V_N reaches V_{ref} . Here, the output of the inverter chain is used as a clock signal for the RCM circuit. Fig. 1(c) gives the simulation results obtained for a sensed photo-current varying as a sine wave. Note that the frequency of the generated spikes

[Clk signal in Fig. 1(c)] increases with the illumination level. If we assume that illumination remains constant during the integration phase (GR high), then the RCM pulse count will be a linear function of the pixel illumination level, which is the stored digital value being read out at the end of the GR pulse. Two modes of operations are used in the DPS array, namely: 1) the integration mode in which the pixel is enabled and spikes are counted using the RCM and 2) the readout phase in which the memory is accessed using a pass transistor connected to nodes B0–B7. In addition to the pass transistor required, an additional gate is needed in order to set the READ or WRITE operation mode for the pixel.

III. EXPERIMENTAL RESULTS

To verify its functionality, the proposed RCM-based spiking pixel has been implemented and fabricated using AMIS 0.35- μm CMOS process (5 M, 3.3 V power supply). A microphotograph of an RCM-based spiking pixel is shown in Fig. 2. The photo-sensing element is an n+-diff/p-well photodiode chosen for its high quantum efficiency. The resolution of the in-pixel RCM is 8 bits. The fill factor is better than 15% for a pixel size of $50 \times 50 \mu\text{m}$, integrating a total of 162 transistors. This number of transistors per 8-bit spiking DPS remains acceptable when considering other digital pixel

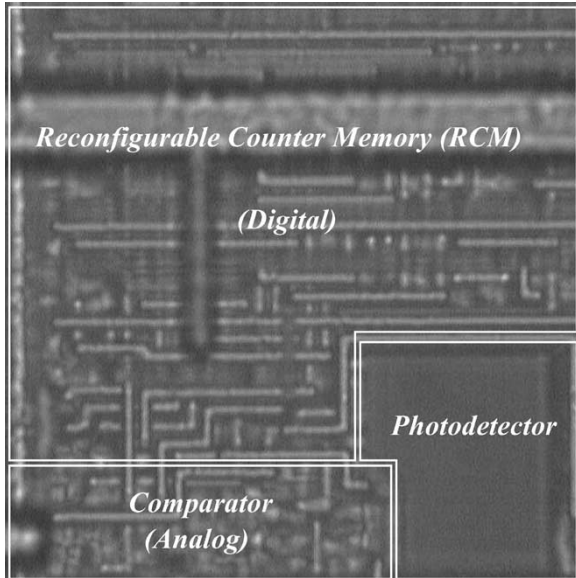


Fig. 2. Microphotograph of the spiking pixel ($50 \times 50 \mu\text{m}$).

implementations (214 transistors reported for Andoh's digital image sensor [5]). The fill factor of the RCM-based spiking pixel can be improved while reducing the pixel size by using sub- $0.25\text{-}\mu\text{m}$ CMOS processes. For instance, based on the layout design redrawn in sub- $0.25\text{-}\mu\text{m}$ processes, pixel sizes of about 23, 17, and $13 \mu\text{m}$ are achievable, for a fixed fill factor of 20%, using 0.18- , 0.13- , and $0.09\text{-}\mu\text{m}$ CMOS processes, respectively. Using three-transistor (3T) and one-transistor (1T) DRAM structures would allow to further decrease the pixel size and improve the fill factor. However, using DRAM would require the design of refresh circuits. Furthermore, the design of 1T DRAM is not compatible with our standard CMOS process. In order to precisely evaluate the dynamic range of our sensor, the frequency of the output signal was measured as a function of the illumination level. Experimental results reported in Fig. 3 show that the fabricated spiking pixel exhibits a quasi-linear characteristic as a function of the incident illumination. The RCM-based sensor operates successfully for 5 decades of variation in illumination levels. The achievable dynamic range is better than 100 dB inasmuch as our experimental setup did not bring the sensor to saturation. The dark current was estimated by operating the sensor in dark condition and measuring the average firing rate recorded at about 34 s. The pixel was also tested with scaled voltage supplies and performed successfully down from the nominal 3.3 to 2.1 V.

IV. CONCLUSION

In this letter, a compact RCM is proposed to enable the full potential of spiking pixels in submicrometer CMOS processes. The proposed RCM-based spiking pixel architecture uniquely combines counting and memory functions into a single compact

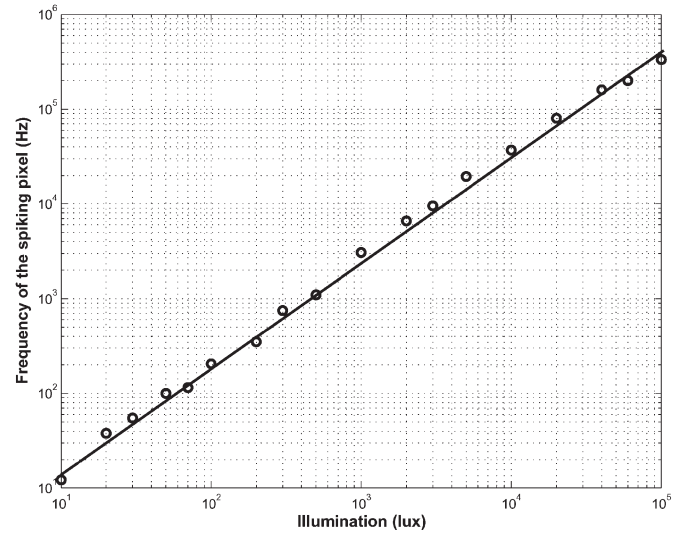


Fig. 3. Spiking pixel response as a function of illumination.

circuit. Other significant advantages of RCM-based spiking pixels include a relative insensitivity to the ongoing aggressive reduction in supply voltage, together with an in-pixel memory, allowing for intermediate readout of pixel digital values. Reported experimental results validate the novel concept of an RCM-based spiking pixel operating with a significantly scaled down supply voltage and featuring a dynamic range above 100 dB and a mean dark firing rate of 34 s. The RCM-based spiking pixel occupies an area of $50 \times 50 \mu\text{m}$ with more than 15% fill factor in AMIS $0.35\text{-}\mu\text{m}$ CMOS technology. The proposed pixel is expected to benefit significantly from CMOS technology scaling trends, particularly when using DRAM technology.

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