Low-Power Column-Parallel ADC for CMOS Image Sensor by Leveraging Spatial Likelihood in Natural Scene

Lifen Liu, Hang Yu and Shoushun Chen
VIRTUS IC Design Center of Excellence, School of EEE
Nanyang Technological University, Singapore

***Abstract*—This paper presents the architecture, algorithm and implementation of a low-power column-parallel analog-to-digital converter (ADC) for CMOS image sensor. The analysis of most natural scenes shows that neighbor pixels have strong correlations. In this paper, a prediction scheme was proposed based on this spatial likelihood in natural scenes. The scheme predicts the MSBs of the selected pixel using previous-row pixel A/D conversion data, which enables significant reduction of A/D conversions steps on MSBs and the power consumption. The simulation results show that up to 20%-30% power saving can be achieved for most natural scenes. A prototype CMOS image sensor (CIS) chip, including a 98×98 pixel array and a 9-bit column-parallel successive approximation register (SAR) ADC array, was fabricated using 0.35μm CIS technology. The silicon size is 3.5×1.8 mm^2.**

***Keywords*—CMOS image sensor, low-power, SAR ADC, common MSBs, prediction scheme**

I. Introduction

The concept of smart cameras has evolved from simple devices to today's complex vision systems over the past decades. The broad range of applications has been realized in many different markets, including sensor networks, consumer electronics, digital surveillance, biomedical imaging and star trackers[1][2].

Integration of column-parallel analog-to-digital (ADC) technology on the CMOS image sensor has become a norm, in particular for consumer electronics. The expansion of this markets has continuously driven the design technologies toward higher performance but low-power consumption. Readout circuits, in particular column-parallel ADC, play a key role in the total power consumption of a CMOS image sensor. In an image sensor, traditional A/D conversions operate in the same manner, repeating across row to row, column to column, and frame to frame, regardless the property of the scene[3][4][5].

In this paper, a prediction scheme is proposed that leverages the spatial likelihood of natural scenes to achieve a low-power column-parallel ADC system. For the selected-row pixels in a frame, their most significant bits (MSBs) are predicted by previous-row pixels, where the A/D conversion steps originally applied for the predicted MSBs are disabled. This enables significant savings on the total A/D conversion steps and power consumption of the column-parallel ADC system.

The rest of this paper is organized as follows: Section II introduces the algorithm for this prediction scheme. Section III illustrates the image sensor architecture and ADC circuitry.

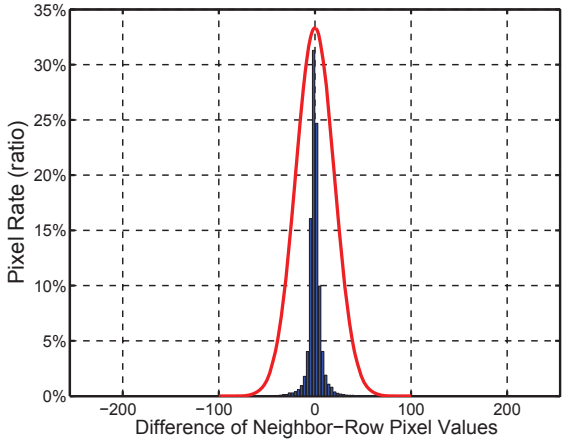


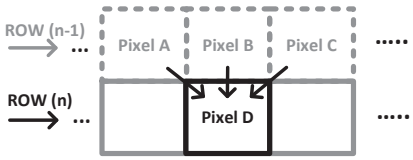
Fig. 1. Distribution graph of neighbor-row-pixel difference for an image (Lena 512×512). The difference is mainly located in the range from -50 to 50 within [-255,255] full scale. The graph of blue-color bar is the distribution ratio of pixels in total pixels of a frame, and red-color curve is the enveloped Gaussian curve.

Section IV describes the simulation and experimental results. Finally, conclusions are drawn in Section V.

II. Algorithm Consideration

Considering the property of spatial likelihood in natural scenes, hundreds of natural images were simulated to calculate the differences in neighbor-row pixels through the Matlab program. The high similarity of neighbor-pixel values was realized, as a group of pixels are occupied by the same object in a scene. And the differences distribute around a value of 0. The simulation result of one example (Lena 512×512) is shown in Fig. 1, where the pixel differences mainly locate at [-50,50] range with a full-scale value from -255 to 255. This means that the differences are mainly contributed by the least significant bits (LSBs) in terms of digital expression of pixel values.

The algorithm proposed in this paper is a prediction scheme, which is based on the strong correlation between consecutive rows in the natural scenes. In an image sensor system, the prediction scheme operates row by row, and the MSBs of each row are predicted by the previous row. In terms of one selected pixel, its MSBs are predicted by using its neighbor pixels in the previous row, which is illustrated in Fig 2(a). The pixel D is the selected pixel, and pixel A, B and



(a) ADC conversion of Pixel D is based on previous-row Pixel (A, B, C) results.

Pixel A	1	0	1	0	1	1	0	0	0
Pixel B	1	0	1	0	0	1	0	1	0
Pixel C	1	0	1	0	1	0	1	1	1
Common MSBs (m bits)	1	0	1	0	X	X	X	X	X
Predicted MSBs (m-1 bits)	1	0	1	X	X	X	X	X	X

(b) Common-MSB of pixel (A, B, C) is estimated as reference voltage level.

Fig. 2. (a) Operating principle of using previous-row pixel data to predict MSBs for a selected pixel. (b) Methodology of generating predicted MSBs for a selected pixel.

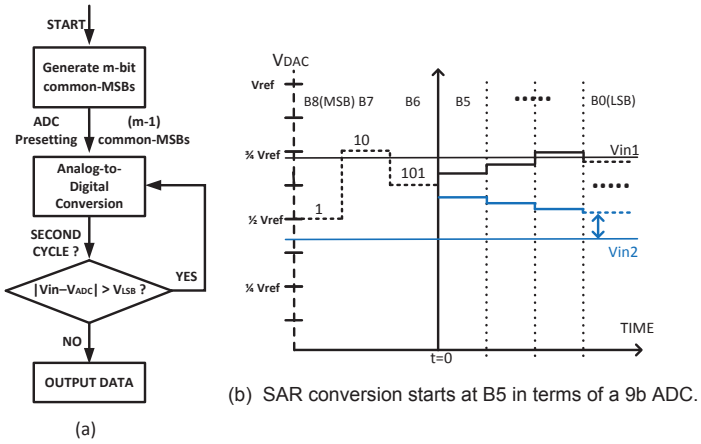


Fig. 3. (a) Operating algorithm of the ADC system based on the prediction scheme. (b) The detail 9-bit SAR ADC conversion steps with predicted MSBs (101XXXXXX).

C are the neighbor pixels in the previous row.

As the differences of neighbor-row pixels are mainly contributed by LSBs, the common MSBs of neighbor pixels in the previous row can be assigned as the predicted MSBs for the selected pixel. In order to increase the accuracy of this prediction scheme, one bit less of the common MSBs are assigned as the predicted MSBs. As shown in Fig 2(b), the predicted MSBs (101XXXXXX) for pixel D are one bit less than common MSBs (1010XXXXX) of pixel A, B and C.

The operating principle of this prediction scheme is illustrated in Fig. 3. According to the operating algorithm as shown in Fig. 3(a), for a selected pixel, its MSBs are first estimated and preset into the ADC. Later the conventional A/D conversion steps are used to derive its left LSBs. At the end, the correctness of the prediction is evaluated, by checking the difference of the corresponding analog value of the complete ADC output including the predicated MSBs (V_{ADC}), and the analog input (V_{in}). If the prediction is successful, their difference shall be smaller than the corresponding analog value of one LSB (V_{LSB}). As stated above, in most natural

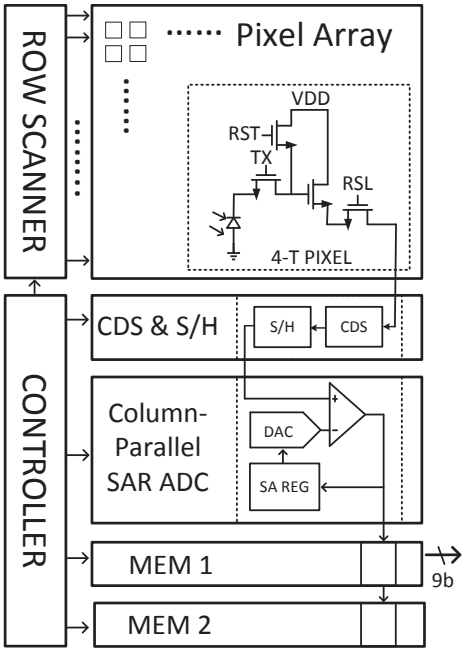


Fig. 4. Block Diagram of the CMOS image sensor with prediction scheme.

scenes, the pixel difference between neighbor rows is small and therefore in most cases the predication is correct and no further A/D conversion steps are needed for the MSBs. In the case of failure, however, the ADC should start over and run a complete (MSBs+LSBs)-bit conversion steps. Two examples are shown in Fig. 3(b), two analog inputs namely V_{in1} and V_{in2}, starting from the same predicted MSBs, 101XXXXXX. After last bit conversion, V_{in1}'s MSBs were found to be predicted corrected, while V_{in2} has to discard the predicted MSBs as incorrect prediction.

For a selected row, each pixel has different predicted MSBs and its starting point of A/D conversion for the left LSBs is also different. That means the architecture of ADC required in this application should be able to start A/D conversion from different reference level, without affecting the ADC resolution. Successive approximation register (SAR) ADC will be the best choice for this proposed prediction scheme comparing with other architectures, as its operating algorithm is based on binary search trees [6].

III. Image Sensor Architecture

Fig. 4 shows the block diagram and the signal path of a CMOS image sensor with the proposed algorithm. It consists of a 98×98 pixel array (4-T APS), a correlated double sampling (CDS) and sample-hold (S/H) circuitry, a column-parallel SAR ADC array and two sets of memories. One memory is used to store the A/D conversion data for readout, the other one is used for the prediction scheme. The row scanner and controller provide all the control signals to the whole image sensor system.

A. Architecture of SAR ADC

Fig. 5(a) shows the simplified block diagram of a SAR ADC system with the proposed prediction scheme. Only

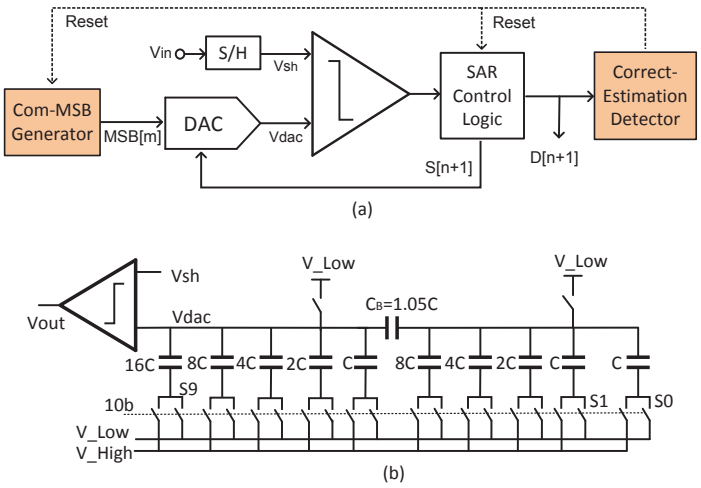


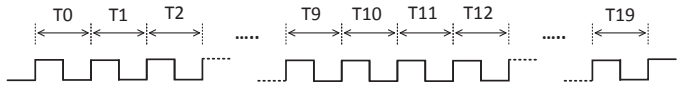
Fig. 5. (a) Block diagrams of a column-parallel SAR ADC with proposed algorithm. (b) Circuit architecture of the SAR DAC with comparator.

two function blocks, the Com-MSB Generator and Correct-Estimation Detector, are added inside the SAR ADC architecture. They are used to generate the predicted MSBs and determine the correctness of predicted scheme respectively. The predicted MSBs are generated before the operation of the SAR ADC system, and the correctness of prediction scheme is checked after the operation of SAR ADC system. Even for the triggered second A/D conversion, both of them will be disabled. As such, they will have minimum effect on the original SAR ADC system, like linearity, resolution, effective number of bits (ENOB), etc.

Fig. 5(b) presents the circuit architecture of the digital-to-analog (DAC) in the proposed SAR ADC system. It is a split-capacitor DAC, and has 48.05 unit capacitors (C) in total for 9-bit resolution. The maximum equivalent load capacitor observed between the top and bottom plate capacitor array is 32 C. Therefore, the power consumption for the SAR DAC and silicon array is greatly reduced compared with a conventional DAC architecture. In addition, the capacitor array here is split into 5-bit/4-bit arrays, with digital control bits from S9 to S1. The extra bit (S0) is used for checking the correctness of the predicted MSBs, without affecting the ADC resolution, since it is not treated as a quantization output of the ADC.

B. Timing Diagram of SAR ADC

The timing diagram of the proposed SAR A/D conversion is illustrated in Fig. 6. The first cycle T0 is used to generate common-MSBs of the previous row, and (m-1) bits of them are assigned as predicted MSBs for the selected row. T1 to T9 are 9-bit SAR ADC conversion cycles, and only T5-T9 are used for A/D conversion if 4-bit predicted MSBs are assigned inside. T10 is used for extra-bit conversion (S0 in Fig. 5(b)), which is used to check the correctness of the predicted MSBs. If prediction is incorrect, another 9 cycles (T11 to T19) will be required for a new SAR A/D conversion to generate the accurate quantization results. Otherwise, T11 to T19 will not be used, and the digital data with predicted MSBs will be stored into memory for readout and the next prediction cycle.



T0 : Preset the (m-1) bits common-MSB into DAC
T1—T9 : Successive Approximation Conversion
(If there are 4b common MSBs preset into DAC, then only T5 to T9 are used, and ADC use the 4b common-MSB during T1 to T4)
T10 : Determine the correctness of prediction scheme
(If S_dum has same value as S0, it is wrong estimation; otherwise, it is correct estimation.) (Refer to Fig. 3)
T11—T19 : Another Successive Approximation Conversion
(If it is wrong estimation, T11 to T19 are used for another A/D conversion cycle; otherwise, T11 to T19 are not used.)

Fig. 6. Conversion-step sequence of the SAR ADC with control logic for proposed algorithm.

TABLE I. PERFORMANCE SUMMARY OF THE IMAGE

Process technology	0.35μm AMS CIS (2P4M)
Pixel size/Fill Factor	3.5×1.8 mm^2/ 35%
Sensitivity	0.33A/W
Dark current	11mV/s
Dynamic range	44.12dB
FPN	1.24%
Power supply	3.3V
Power consumption	42.3mV
ADC resolution	9 bits
ADC input range	2V
ADC clock frequency	20MHz
Data rate	20Mp/s
ADC DNL/INL	(+0.55,-0.91)/(+1.34,-1.8)
ADC SNR	49dB

IV. SIMULATION RESULTS

A. Power Consumption Analysis

For analysis of the power consumption of the SAR ADC with the proposed algorithm, the capacitor switching power of the DAC block should be discussed as it contributes the most to total power consumption [7]. The switching energy for each bit is illustrated in Table II, which shows that the switching power is mainly contributed by A/D conversion steps on MSBs. For the proposed algorithm, the total A/D conversion steps are saved significantly, and the MSBs conversion steps are saved the most. As such, the capacitor switching power saved for one frame is also significant.

Therefore, several groups of natural scenes were simulated by Matlab based on the proposed algorithm. The power consumption and A/D conversion steps saved are shown in Fig. 7. Up to 20% to 30% savings on conversion steps, and 20% to 35% power saving had achieved for most of the pictures.

TABLE II. SWITCHING POWER OF EACH BIT

Switched Step	S9	S8	S7	S6	S5
Switching Power (CV_{ref}^2)	8	2	1/2	1/8	1/32
Switched Step	S4	S3	S2	S1	
Switching Power (CV_{ref}^2)	1/64	1/128	1/256	1/512	

Image folder 1

Image folder 2

Standard Test Image

(17 images)

Reference:

www.imageprocessingplace.com/root_files_V3/image_databases.htm

Conversion Steps Saved	Switching Power Saved	Conversion Steps Saved	Switching Power Saved	Average Conversion Steps Saved	Average Switching Power Saved	Average Conversion Steps Saved	Average Switching Power Saved	Average Conversion Steps Saved	Average Switching Power Saved
23.72%	23.72%	23.72%	23.72%	23.72%	23.72%	23.72%	23.72%	23.72%	23.72%

Fig. 7. Conversion cycles and switching power saved based on prediction scheme compared with traditional SAR ADC operation (a N-bit SAR ADC has N A/D conversion steps in traditional way). Image folder 1 contains 62 photos taken at Singapore Zoo, image folder 2 contains 47 images taken at Venice.

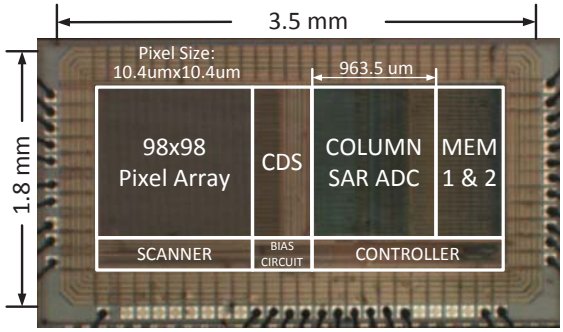


Fig. 8. Chip microphotograph. Die size is 3.5 $\times$ 1.8 mm^2.

Parameter	Saved
D8	50.75%
D7	28.53%
D6	20.05%
D5	16.00%
D4	14.72%
D3	14.22%
D2	13.85%
D1	13.73%
D0	-5.72%

Fig. 9. Sample image taken by the prototype CMOS image sensor. Conversion steps saved is 18.57%, and switching power saved is 22.36%.

B. Experimental Results

A CMOS image sensor with the column-parallel SAR ADC system for this prediction scheme was implemented with 0.35 μm AMS CIS (2P4M) technology. The die micrograph of the fabricated sensor chip is shown in Fig. 8. The sample image taken by this fabricated image sensor is shown in Fig. 9. The power consumption for this image is saved up to 22.36% compared to a traditional design without this prediction scheme. The measured performance of the implemented sensor is summarized in Table I.

V. Conclusion

A CMOS image sensor with the proposed prediction scheme that leverages spatial likelihood in natural scenes is presented in this paper. This proposed algorithm is implemented in a compact 9-bit column-parallel SAR ADC system, where a redundant bit was introduced inside to check the correctness of this prediction scheme. The simulation results show that it can achieve 20%-30% savings in total A/D conversion cycles and 20%-35% savings in switching power of the SAR DAC. Furthermore, the experiment results showed that total power consumption is reduced by up to 22% compared to an image system without the prediction scheme.

VI. Acknowledgement

This work was supported by ACRF Project grant (M4020153.040).

References

[1] J. Fürtler, E. Bodenstorfer, M. Rubik, K. J. Mayer, J. Brodersen, and C. Eckel, *High-Performance Smart Cameras*. Springer, 2010.

[2] X. Qian, H. Yu, S. Chen, and K. S. Low, "An adaptive integration time cmos image sensor with multiple readout channels for star trackers," in *Solid-State Circuits Conference (A-SSCC), 2013 IEEE Asian*. IEEE, 2013, pp. 101–104.

[3] D. G. Chen, F. Tang, and A. Bermak, "A low-power pilot-dac based column parallel 8b sar adc with forward error correction for cmos image sensors," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 60, no. 10, pp. 2572–2583, 2013.

[4] M. F. Snoeij, A. J. Theuwissen, K. A. Makinwa, and J. H. Huijsing, "Multiple-ramp column-parallel adc architectures for cmos image sensors," *Solid-State Circuits, IEEE Journal of*, vol. 42, no. 12, pp. 2968–2977, 2007.

[5] T. Randall, I. Mahbub, and S. K. Islam, "A low power auto-reconfigurable pipelined adc for implantable biomedical applications," in *Sensors, 2013 IEEE*. IEEE, 2013, pp. 1–4.

[6] W.-S. Liew, L. Yao, and Y. Lian, "A moving binary search sar-adc for low power biomedical data acquisition system," in *Circuits and Systems, 2008. APCCAS 2008. IEEE Asia Pacific Conference on*. IEEE, 2008, pp. 646–649.

[7] B. P. Ginsburg, "Energy-efficient analog-to-digital conversion for ultra-wideband radio," Ph.D. dissertation, Massachusetts Institute of Technology, 2007.