## Ultra-low power series input resonance differential common gate LNA

## T.T.N. Tran, C.C. Boon, M.A. Do and K.S. Yeo

In the 2.4 GHz IEEE 802.15.4 standard, the noise figure (NF) requirement can be relaxed to minimise power consumption. A fully differential gm-boosting common-gate (CG) low-noise amplifier (LNA) with a series inductor input matching network is proposed. The LNA consumes less than 1 mA from 1 V power supply and achieves a measured gain of 15.5 dB. The series inductor input matching CGLNA is attractive for low-power fully integrated applications in CMOS technologies.

Introduction: The series RLC input matching network in the commonsource (CS) LNA topology effectively boosts the transistor's transconductance,  $g_m$ , to  $Q_L g_m$  where  $Q_L$  is the quality factor of the input matching network [1]. This is the key to its high gain and low NF. These benefits come at a cost of large chip area since at least two inductors are needed at the gate and source of the input device. The CGLNA normally requires a less number of on-chip inductors than the CSLNA. It also exhibits good reverse isolation and stability since the gate terminal of the input device is AC grounded. However, its parallel RLC input matching network limits its noise and gain performance. Matching the input impedance of the CGLNA to the source impedance restricts the choices of power consumption and device size [1]. In many narrow band LNAs, the CS topology is widely used owing to its high gain and low NF advantages. However, in the 2.4 GHz IEEE 802.15.4 standard, the NF requirement can be relaxed to minimise power consumption [2]. In this Letter we propose a new ultra-low power LNA scheme which will fully utilise the above property of the IEEE 802.15.4 standard. Its main advantages include: (a) adding an additional degree of freedom to the input matching design and (b) improving the NF when the power consumption is low.

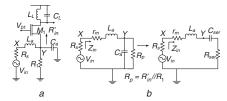


Fig. 1 CGLNA with series input matching (Fig. 1a), and equivalent input matching network of CGLNA with series input matching network (Fig. 1b)

Theory and design equation of proposed LNA: Figs. 1a and b show schematic diagrams of the CGLNA with the series input network and its equivalent small signal circuit for input matching analysis. To reduce chip area, the source inductor was replaced by resistor  $R_1$ .  $C_a$  is the total capacitance at node Y. Resistor  $r_m$  is the loss of the inductor  $L_a$ .  $R'_{in}$  is the impedance looking into the transistor source terminal from node Y which is:

$$R'_{\rm in} = (r_{ds} + R_L)/(1 + g_m r_{ds}) \tag{1}$$

where  $R_L$  is the equivalent output impedance and  $r_{ds}$  is the transistor drain source resistance. The input impedance is:

$$Z_{\rm in} = j\omega_0 L_a + \frac{1}{j\omega_0 C_{ser}} + R_{ser} + r_m \tag{2}$$

In (2), 
$$R_p = R'_{in}//R_1$$
,  $R_{ser} = \frac{1/K_p}{(1/R_p)^2 + \omega_0^2 C_a^2}$  and

 $C_{ser} = C_a + \frac{1}{C_a (R_p \, \varpi_0)^2}$ . In the conventional CGLNA, if the  $g_m$  value is different from  $1/R_s$ , the input impedance is not matched to the

is different from  $1/R_s$ , the input impedance is not matched to the source impedance. In our LNA, capacitance  $C_a$  adds an additional degree of freedom to the input matching design. The impedance can be easily matched to the source by setting  $Z_{in}$  equal to the source impedance  $R_s$ . The series matching topology enhances the overall voltage gain by  $G_{ser}$  times, which is:

$$G_{ser} = \sqrt{[R_{ser}/(R_{ser} + r_m)]^2 + [\omega_0 L_a/(R_{ser} + r_m)]^2}$$
(3)

The NF of the conventional CGLNA including the effect of  $R_1$  and  $C_a$  is:

$$F_{CGLNA} = 1 + A_1 \frac{\gamma g_m}{\alpha R_s} \left(\frac{1}{g_m + 1/r_{ds}}\right)^2 + \frac{R_s}{R_1}$$
(4)

where

$$A_1 = (1 + R_s/R_1)^2 + (\varpi_0 C_a R_s)^2$$
(5)

In (4),  $\gamma$  is the coefficient of the channel thermal noise and  $\alpha$  is the ratio of the transconductance to zero VDS channel conductance. If  $R_1 \rightarrow \infty$ ,  $r_{ds} \rightarrow \infty$  and  $C_a \rightarrow 0$ ,  $F_{CGLNA} = 1 + (\gamma/\alpha)/(g_m R_s)$ , which is consistent with the classical result. The drain current noise and the thermal noise of  $R_1$  account for the second and third term in (4), respectively. The total NF of the proposed LNA is derived as follows:

$$F_{L-CGLNA} = 1 + A_2 \frac{\gamma g_m}{\alpha R_s} \left(\frac{1}{g_m + 1/r_{ds}}\right)^2 + \left[\frac{R_s}{R_1} \left(1 + \frac{r_m}{R_s}\right)^2 + \frac{(\omega_0 L_a)^2}{R_1 R_s}\right] + \frac{r_m}{R_s}$$
(6)

where

$$A_{2} = [1 + (R_{s} + r_{m})/R_{1} - \omega_{0}^{2}L_{a}C_{a}]^{2} + (\varpi_{0}C_{a}R_{s} + \varpi_{0}L_{a}/R_{1} + \varpi_{0}C_{a}r_{m})^{2}$$
(7)

The second term in (6) is introduced by the drain current noise. The third and fourth terms are by the thermal noise of  $R_1$  and  $r_m$ . The use of series input inductor  $L_a$  introduces extra noise to the circuit owing to the inductor loss  $r_m$ . However, the negative component which is  $(-\omega_0^2 L_a C_a)$  in the expression of  $A_2$  helps to lower the noise contribution of the drain current noise when compared to the conventional CGLNA. A conventional CGLNA was designed to compare its NF with our CGLNA with series input matching. The NF simulation results are shown in Fig. 2. There is great improvement of NF.

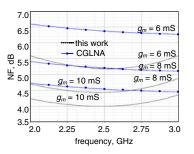


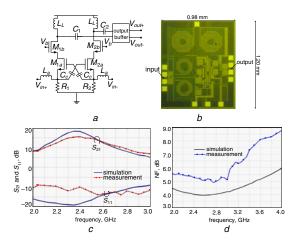
Fig. 2 NF at different  $g_m$  values in 0.18  $\mu m$  RF CMOS technology

*Experiment:* To demonstrate the idea, a LNA was designed and fabricated in a standard 0.18  $\mu$ m RF CMOS technology. To improve further the gain performance of the circuit, two big capacitors  $C_c$  were placed across the two sides of a differential input stage to effectively boost the transistor's transconductance value without requiring extra DC current [1]. This increases the voltage gain by two times, making the total improvement in voltage gain becoming  $2G_{ser}$ , and the total NF is reduced to:

$$F_{L-CCC-CGLNA} = 1 + \frac{A_2}{2} \frac{\gamma}{\alpha} \frac{g_m}{R_s} \left(\frac{1}{g_m + 1/r_{ds}}\right)^2 + \left[\frac{R_s}{R_1} \left(1 + \frac{r_m}{R_s}\right)^2 + \frac{(\omega_0 L_a)^2}{R_1 R_s}\right] + \frac{r_m}{R_s}$$
(8)

The complete schematic of the LNA and its chip micrograph are shown in Figs. 3*a* and *b*. Total chip size is  $0.98 \times 1.2 \text{ mm}^2$ . Figs. 3*c* and *d* show the measured  $S_{11}$ , voltage gain and the NF of the LNA. The LNA has better than -10 dB input matching over the desired band. At 2.4 GHz, the voltage gain is 15.5 dB and the NF is 5.2 dB. The LNA core consumes only 0.98 mW power from a 1 V supply voltage. The measured IIP3 of the LNA core is -19 dBm. Comparisons of this LNA with published 2.4 GHz LNAs are summarised in Table 1. The LNAs in [3–5] have better NF but consume much more power than ours. Moreover, such low NF is not necessary for our application [2]. The LNA in [2] has better FOM than ours

owing to the higher gain. This high gain is achieved by using a large load resistor which results in a requirement of high supply voltage at 1.8 V. The LNA in [2] cannot operate at low supply voltage such as 1 V.



**Fig. 3** Complete schematic of proposed LNA (Fig. 3a); chip micrograph of proposed LNA (Fig. 3b); measured and simulated  $S_{11}$  and  $S_{21}$  of LNA (Fig. 3c); measured and simulated NF of LNA (Fig. 3d)

Table 1: Performance summary and comparisons of 2.4GHz LNAs

	Technology (µm)	Frequency (GHz)	Gain (dB)	NF (dB)	S <sub>11</sub> (dB)	IIP3 (dBm)	Vdd (V)	Differential	Pdc (mW)	FOM**
[2]	0.18		21.4	5.2	-19	-11	1.8	No	1.13	10.7
[3]	0.13		13	3.6	-14	n/a	1.2	No	6.5	1.28
[4]*	0.18	2.4	14.6	3.7	-24.1	2.6	1.8	No	12.2	0.78
[5]	0.18		10.1	2.9	-10.1	4	1.8	No	11.7	0.69
This work	0.18		15.5	5.2	-11	-19	1	Yes	0.98	6.3

\*simulation results; \*\*FOM =  $[Freq_{(GHz)} Gain_{(mag)}]/[(F - 1)_{(mag)} P_{DC(mW)}]$ 

Conclusion: An ultra-low power low-voltage series input resonance with a gm-boosting technique differential CGLNA was designed for the IEEE 802.15.4 standard. Unlike the conventional CGLNA, the  $g_m$  value of this LNA is not fixed by the input matching condition which makes optimising for low power possible. The LNA shows excellent trade-off between NF and power consumption. The measured power consumption is among the lowest in the current literature. The proposed technique makes the CG topology attractive for low-power fully integrated designs.

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doi: 10.1049/el.2011.0961

One or more of the Figures in this Letter are available in colour online.

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## References

- Zhuo, W., Li, X., Shekhar, S., Embabi, S.H.K., Gyvez, J.P.d., Allstot, D.J., and Sanchez-Sinencio, E.: 'A capacitor cross-coupled commongate low-noise amplifier', *IEEE Trans. Circuits Syst. II*, 2005, 52, (12), pp. 875–879
- 2 Do, A.V., Boon, C.C., Do, M.A., Yeo, K.S., and Cabuk, A.: 'A subthreshold low-noise amplifier optimized for ultra-low-power applications in the ISM band', *IEEE Trans. Microw. Theory Tech.*, 2008, 56, (2), pp. 286–292
- 3 Kaamouchi, M.E., Moussa, M., Delatte, P., Wybo, G., Bens, A., Raskin, J.P., and Vanhoenacker, J.J.: '2.4-GHz fully integrated ESD-protected low-noise amplifier in 130-nm PD SOI CMOS technology', *IEEE Trans. Microw. Theory Tech.*, 2007, 55, (12), pp. 2822–2831
- 4 Cheng, W.C., Jian, M.G., Yeo, K.S., and Do, M.A.: 'Design of a fully integrated switchable transistor CMOS LNA for 2.1/2.4 GHz application'. European Microwave Integrated Circuits Conf., Manchester, UK, 2006, Vol. 1, pp. 133–136
- 5 Lu, L.H., Hsieh, H.H., and Wang, Y.S.: 'A compact 2.4/5.2-GHz CMOS dual-band low-noise amplifier', *IEEE Microw. Wirel. Compon. Lett.*, 2005, **15**, (10), pp. 685–687