An Ultra-Wideband Receiver Front-end

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Abstract

The needs for short range and fine resolution communication systems has intrigued researchers to replace wire-line communications systems with ultra-wideband communications systems. The Ultra-wideband radio technology introduces significant advantages for short-range communications systems. This technology operates in a wide bandwidth, which allows for Gigabit data rates over short distances. Due to the low complexity of the ultra-wideband system and low transmit power, it benefits from low DC power consumption. However, with growing demands for wireless communications systems, more challenging requirements are faced with the ultra-wideband communications systems. Since ultra-wideband covers a wide range of frequency, it exhibits challenges in the design of building blocks, receiver front-end in particular. The scope of this thesis is to design a novel and innovative RF front-end receiver for ultra-wideband transceivers using CMOS technology.

A T-coil network can be implemented as a high order filter for bandwidth extension. This technique is incorporated into the design of the input matching and output peaking networks of a low-noise amplifier. The intrinsic capacitances within the transistors are exploited as a part of the wideband structure to extend the bandwidth. Using the proposed topology, a wideband low-noise amplifier with a bandwidth of $3-8$ GHz, a maximum gain of 16.4 dB and noise figure of 2.9 dB (min) is achieved. The total power consumption of the wideband low-noise amplifier from the 1.8 V power supply is 3.9 mW. The prototype is fabricated in 0.18 μm CMOS technology.

Furthermore, a two-stage down-conversion architecture for $3.1-8$ GHz ultra-wideband receiver front-end is designed which uses a local oscillator frequency equal to half the input frequency. A single stage low power single-to-differential low noise amplifier is designed to eliminate the need for an off-chip balun and increases the integrity level of the front-end receiver. Consecutively, the RF frequency is down-converted in two steps based on

half-RF architecture to produce baseband signal. The proposed architecture has many advantages such as linearity and good port-to-port isolation. The proposed technique is implemented in 0.18 μm CMOS technology which achieves a conversion gain ranges from 36.1−32.4 dB and noise figure of 5.4−8.3 dB across the bandwidth.

Chapter 1

Introduction

1.1 Motivation

Ultra-wideband systems are a new wireless technology capable of transmitting data over a wide spectrum of frequency bands for short distances with very low power and high data rates. Back to 1960s, ultra-wideband (UWB) came to be known for the operation of sending and receiving extremely short bursts of RF energy. It has outstanding ability for applications that requires precision distance or positioning measurement as well as high-speed wireless connectivity. The UWB technology delivers data rates in excess of 100 Mbps up to 1 Gbps. The UWB not only has the potential of carrying high data rate over short distance, but also it can penetrate through doors and other obstacles. The key advantages of the UWB systems over narrowband systems are: high data rate due to the large bandwidth, low equipment cost, low power and immunity to multipath.

A significant difference between traditional radio transmission and UWB radio transmission is that traditional communications systems transmit data by varying the power level, frequency, and/or phase of a sinusoid wave. However, in UWB radio, data is transmitted either as impulse radio (IR or multiband orthogonal frequency division multiplex (OFDM). The IR UWB transmits data based on the transmission of very short pulses. In some cases, impulse transmitters are employed where the pulses do not modulate a carrier. This technique results in lower-data rate and -design complexity compared to

the OFDM system. On the other hand, in the multiband OFDM technique each band with 528 MHz width encodes the data using QPSK modulation. Using this technique a data rate of 480 Mb/s can be achieved. However, the design of this system is more challenging.

The operation of the UWB is based on two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesirable operation. Regarding to the Federal Communications Commissions (FCC) UWB devices occupy more than 500 MHz of bandwidth in the 3.1 GHz$-$10.6 GHz band. The power spectral density (PSD) of the UWB transmitter measured in 1 MHz is limited to -41.3 dBm/MHz to avoid interference with existing standard [7].

Due to wideband requirements of the UWB transceiver's RF front-end, it is very challenging to design RF front-end receiver. In most applications, it is desirable to obtain wideband on-chip input matching to a 50 Ω antenna/filter, good linearity, and low power consumption. In addition, gain flatness over the entire frequency range of interest is necessary to meet the design specifications. These properties are the cornerstones of the wideband receiver front-end which affect the total broadband communication system characteristics. The scope of this dissertation is to design an innovative wideband RF front-end for UWB transceiver in CMOS technology.

1.2 Objectives

The objectives of this project are summarized as follows:

• To design a low power low noise amplifier in CMOS technology.

• To introduce a simple and an accurate lumped elements model for input/output matching.

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- To propose a single-to-differential conversion technique to overcome the need for differential input signal and reduce the bulky and lossy off-chip devices.

- To develop a low power quadrature mixer with high linearity and low noise figure.

- To integrate the RF front-end in order to realize UWB receiver front-end.

1.3   Outline

Chapter 2 is an introduction to the background and application of the ultra-wideband technology. This chapter reviews different topologies applicable for ultra-wideband systems, and introduces architectures and challenges of this technology. Furthermore, a basic introduction to the RF receiver front-end is reviewed.

Chapter 3 will briefly review some analog style amplifier designs, especially topologies that can provide high-frequency performance. In the microwave amplifiers, active elements such as transistors are treated as two-port device, which this element should be carefully matched to obtain the optimal performance. The classic tuned amplifier will be discussed, to introduce a strategy to compensate the headroom problem in cascode amplifiers. In continue, other methods of tuning amplifiers associated with resonance filters are explained, to bridge a gape between analog and RF amplifiers.

Chapter 4 presents the proposed low noise amplifier circuit for the front-end receiver. Based on the bandwidth enhancement techniques, which are explained step-by-step in this section, a wideband low noise amplifier is resulted. In brief, shunt peaking is a form of bandwidth enhancement in which a one-port network is connected across the amplifier and load. The shunt peaking technique is then further developed to a shunt-shunt network, to achieve a wideband peaking network at the output of the low noise amplifier. Similarly, the same technique is used for the input matching of the low noise

amplifier, to match the amplifier to antenna over a wide range of frequency. Finally, the simulation and measurement results are presented to prove the feasibility of the circuit.

Chapter 5 provides an overview of the active and passive mixer circuit design. The advantages and disadvantages of the different mixer architectures are shortly described. The important characteristics of the mixer including conversion gain, noise figure, linearity and distortion are included in this section.

Chapter 6 presents the integrated low noise amplifier with a two stage down-conversion mixer, to realize a wideband receiver front-end. The simulation and measurement results are discussed at the end of the chapter.

Chapter 7 summarizes the major contributions of this thesis and suggests the future work to be further developed.

Chapter 2

Introduction to Ultra-wideband (UWB) Systems

Ultra-wideband (UWB) radio potentially offers higher communication speeds than traditional narrowband transceivers which may be necessary in the near future to meet growing consumer demands for higher speed and better quality mobile links. In 1963 this standard was proposed by Ross [8]. Afterwards this technology was further defined by Federal Communications Commission (FCC) as any wireless scheme that transmits an extremely low-power signal at a fractional bandwidth of $BW/f_c >$20%, or more than 500MHz bandwidth, where BW is the communication bandwidth and f_c is the band center frequency. This prototype modulates data with binary phase shift keyed (BPSK) pulses over a wideband direct conversion front-end, and samples the received signal for modulation. This standard found applications in imaging systems, high-speed wireless communication, and particularly in short-range high-speed data transmissions suitable for broadband networks [9], [10]. In 2002, the FCC allowed UWB communication in the 3.1$-$10.6 GHz band having a $-$10 dB bandwidth greater than 500 MHz and a maximum equivalent isotropic radiated power spectrum density of -41.3 dBm/MHz to ensure negligible interference. The 3.1$-$10.6 GHz band is divided in 14 channels organized in five groups, as shown in Fig. 2.1. The 14 bands span the range of 3168 to 10560 MHz, and each band consists of 128 subchannels of 4.125 MHz. Bands 1$-$3 constitute "Group 1" and are mandatory
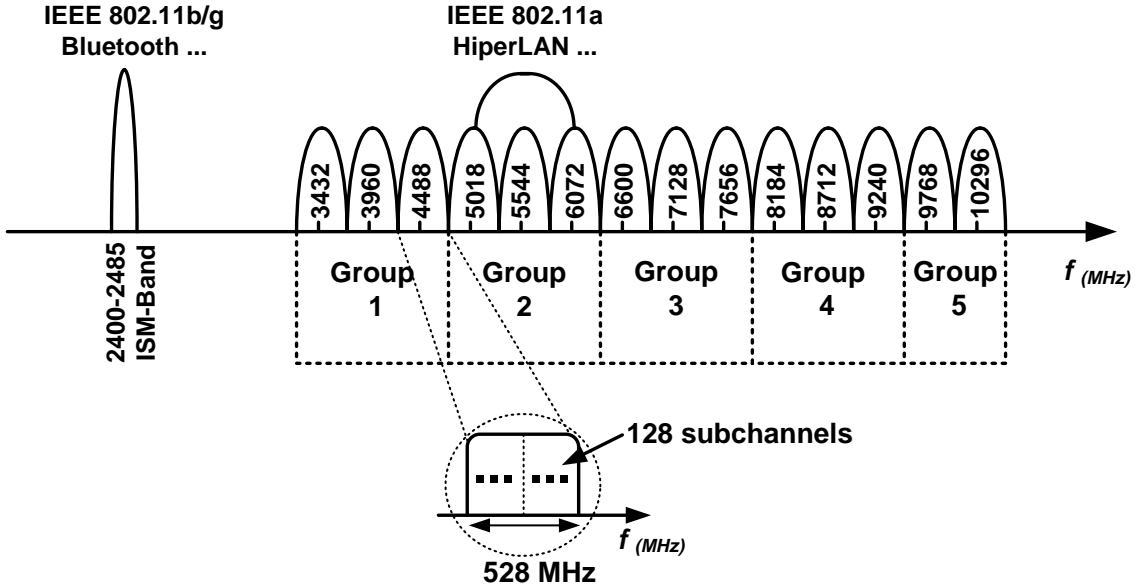
Figure 2.1: Frequency allocation of MB-OFDM UWB channels.

for operation, whereas the remaining bands are envisioned for high-end products [11]. In this band (3.1−10.6 GHz) two proposal on the operation of the UWB devices are being considered. One employs BPSK, providing data rates from 28−1320 Mb/s within the transmission bands from 3.1 GHz to 4.85 GHz and from 6.2 GHz to 9.7 GHz [12]. The other exploits the multi-band orthogonal frequency division multiplexing (MB-OFDM) approach, where information is encoded in 528 MHz wide channel using 122 quadrature phase shift key (QPSK) sub-carrier. The MBOA proposal for 802.15.3a uses OFDM modulation in a bandwidth of 528 MHz [12]. In contrast to IEEE 802.11a/g, MBOA employs only QPSK modulation in each subchannel to allow low resolution in the baseband analog-to-digital (ADC) and digital-to-analog (DAC) converters. The unlicensed band is intended to enable applications such as; ground penetrating radars, imaging/surveillance systems, and wireless home video data links.

The advantage of the UWB systems over narrowband systems is that the UWB transceiver benefits from low complexity, low power, multipath time resolution due to the large bandwidth. A significant difference between traditional radio transmissions and

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UWB radio transmissions is that traditional communication systems transmit data by varying the power level, frequency, and/or phase of a sinusoidal wave. This means that a baseband signal is mixed with higher frequency carrier to a radio frequency within a desired channel for data transmission. In the UWB radio data is transmitted as impulse radio based on the transmission of very short pulses by encoding the polarity of the pulses. In some cases, impulse transmitters are employed where the pulses do not modulate a carrier. Instead, the radio frequency emissions generated by the pulses are applied to an antenna, and the resonant frequency of the antenna determines the center frequency of the radiated emission. So the modulated signal is directly transmitted through the antenna to the air. This has greatly reduced the complexity of the transceiver architecture and RF front-end circuit design compare to the narrowband receivers. The frequency response characteristics of the antenna provides bandpass filtering, further affecting the shape of the radiated signal [13], [14]. As a result, UWB systems benefits from given standard as modulation schemes, multiple access techniques, and high data rates. Although the UWB standard, IEEE 802.15.3a, for wireless personal area network (WPAN) communications has not yet been finalized [15], but it is predicted that these systems will be capable of transmitting at higher data rate, up to 500 Mb/s with power consumption lesser than 1 mW [16] than WiFi technology IEEE 802.11b, with 11 Mb/s data rate and 200 mW power consumption [17]. Thus not only UWB technology can improve the broadband networks but also it can improve the electronic home devices like camcorders, video games and high-definition TV (HDTV) connected to the wireless UWB devices. Other applications of the UWB include portable wall-penetrating radar which is used for military application [18], surveillance systems, and radio frequency identification (RFID).

At part of IEEE P802.15, multiband orthogonal frequency division multiplexing (MB-OFDM) with fast frequency hopping is proposed as a means of high-rate wireless communication in the UWB spectrum [19]. For this mode, the spectrum shown in Fig. 2.1 is

divided into 528 MHZ bands spanning from 3.1−8.2 GHz. The features of such a system must be obtained at moderate power consumption, and to minimize cost on a single chip.

In below several challenges of the UWB system design compared to the narrowband receivers are highlighted.

2.1 UWB Transceiver Architectures

The UWB radios can be implemented either as multiband OFDM (MB-OFDM) or direct-sequence impulse radio (DS-IR). The IR system is relying on a very short duration of the pulses with several Gigahertz bandwidth. The main challenge facing with IR system, is the existence of the neighbor narrowband systems. Since IR receiver/transmitter systems are based on the short pulses, each narrowband signal with the same band from another system can fall on the IR fundamental band and disrupt the signal. A solution to this problem is to use a notch filter, however not only the design of a precise narrowband notch filter is very challenging but also the notch filter can simply disturb the useful signal. Therefore, IR systems need a very high linearity characteristic to rehabilitate the signal. The multiband OFDM on the other hand, can avoid this problem by switching from one band to the other band, not to be affected by the other adjacent channels, which are used by the other systems. Besides, a MB-OFDM has the ability to provide the data rates up to 480 Mbps and above, over a short distance.

2.1.1 Impulse Radio UWB

The UWB radios communicate with short pulses or cycles on the order of nanoseconds, spreading their energy over a wide swath of bandwidth, as opposed to modulated sinusoids whose energy is localized around a single frequency. A sample pulse is shown in Fig. 2.2. The IR UWB transmits data based on the transmission of very short pulses with several Gigahertz bandwidth. In some cases, impulse transmitters are employed where
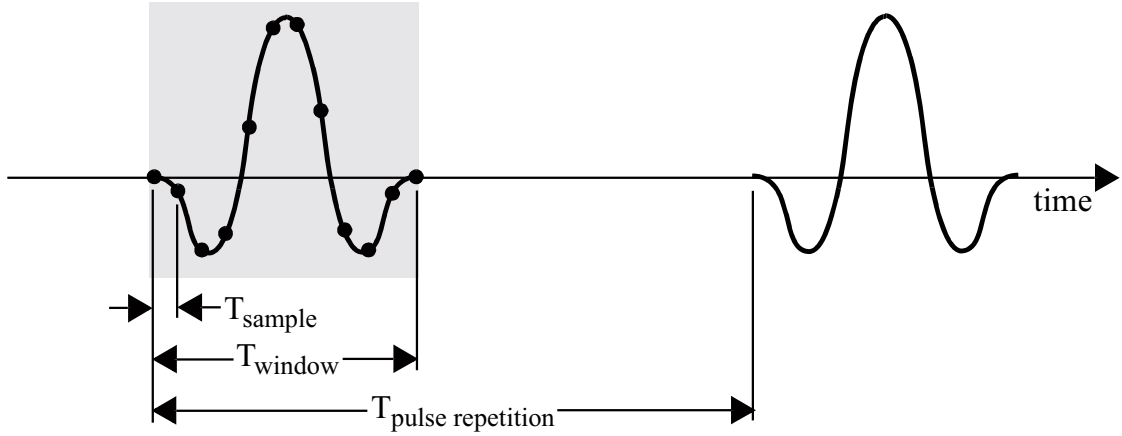
Figure 2.2: UWB impulse radio.

the pulse do not modulate a carrier. This technique results in lower-data rate and -design complexity. However, the main challenge facing with IR system, is the existence of the narrow band systems. A solution to this is to use a notch filter, however notch filter can simply disturb the useful signal. Therefore, IR systems need a very high linearity characteristic to rehabilitate the signal. An example of IR UWB transceiver is shown in Fig. 2.3 [1] with on-off keying modulation scheme for easy implementation and low power consumption. The transmitter is an all digital design, and a CMOS output buffer drives the antenna directly, which eliminates the need for an analog power amplifier. The receiver consists of an LNA and a clocked correlator. In order to reduce the power consumption, the LNA and correlator are operating intermittently. The clocked correlator consists of a mixer/integrator, comparator, template pulse generator, and delay controller. This is an example of power consumption technique, which some of the algorithms are combined with analog domain implementation. In this architecture, the clocked correlator saves the area and power which is normally required for an over-1-GHz ADC designed with conventional receiver architecture. The correlator converts the received RF signal to the baseband signal for further detection. When the received signal and the reference pulse

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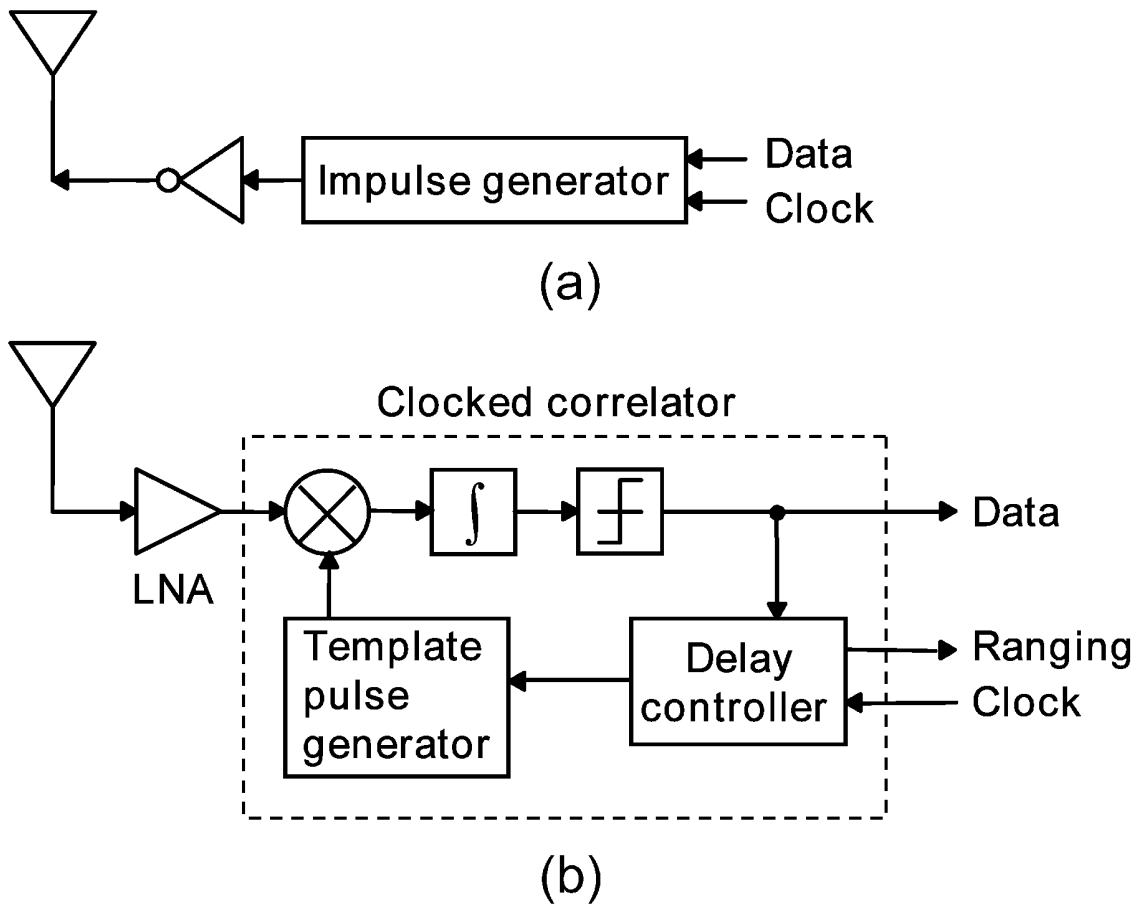
Figure 2.3: A UWB-IR transceiver architecture for (a) transmitter and (b) receiver [1].

are synchronized in phase, a peak emerges to complete the detection process. A transmitter with all digital block is shown in Fig. 2.4. The pulse trains with 2 ns width are modulated by input data with OOK modulation and the differential signal is provided to the antenna by the CMOS buffer.

2.1.2   Multiband OFDM (MB-OFDM) UWB

A block diagram of MB-OFDM UWB receiver is shown in Fig. 2.5, which consist of an LNA followed by a correlator. This architecture is presented as a direct conversion receiver. A preselect filter is placed right after the antenna, to reject the out-of-band signals, noise, and images thus passes only the desired UWB signal. Then the LNA and

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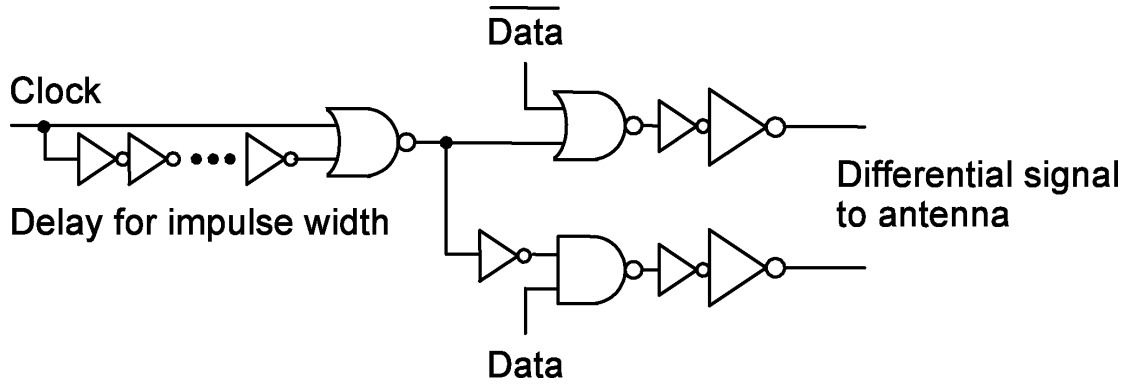
Figure 2.4: All digital transmitter [1].
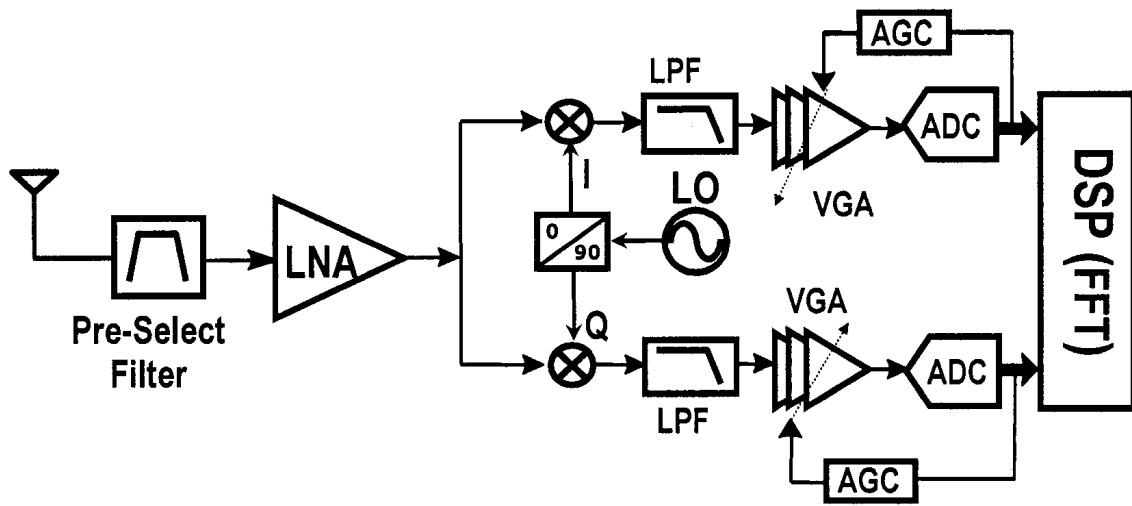
Figure 2.5: An example of MB-OFDM UWB receiver front-end.

downconversion mixer convert the RF signal to the baseband. The low pass filter (LPF) removes the adjacent signals and the level the signal is set by the voltage gain amplifier (VGA). After this, the ADC performs the fast Fourier transform (FFT) to allow for digital signal processing aimed at recovering the signal.

2.1.3 UWB Transceiver Design Challenges

Due to the stringent requirements of the UWB technology, there are challenges facing with the design of the UWB RF front-end circuit specially when it is implemented in the

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low cost CMOS process. In this section some of the constraints are addressed.

The UWB technology is susceptible to in-band interference from existing bands such as those used by 802.11a radios. In other word, when receiving one channel, signals in other channels enter the receiver and appear as blockers. Also, the allowed power spectral density (PSD) is low compared to the narrowband systems. Furthermore, UWB antennas present designers with new opportunities and challenges as; a UWB antenna must exhibit a nearly omnidirectional radiation pattern for a wide range of frequencies, a wideband impedance match, and a linear phase response (i.e., flat group delay). Another important aspect in the UWB system design is that of the interface between antenna and the RF front-end. The parasitic inductances and capacitances from interface can be absorbed into the filter/matching network between the antenna and circuit front-end. With analytical tools it is possible to examine the impact of the extracted matching network, so the impact on the wideband noise figure and gain can be analyzed. The UWB transmitted power levels are required to be below that of noise emission allowed for electronic equipment to increase the sensitivity of the receiver.

Since the bandwidth of the UWB licensed by FCC is from $3.1 - 10.6$ GHz, this implies that RF front-end including LNA and down conversion mixer, should be able to process a bandwidth over a wide range of frequency. From circuit design point of view, it is realized that the design of the UWB transceivers faces with the following challenges; 1) the need for LNA wideband input matching to a 50 Ω antenna, 2) gain flatness of the LNA; because the transmission and reception of the UWB pulse requires approximately constant group delay, 3) to design broadband receive/transmit switch at the antenna, 4) desensitization due to the WLAN interferences, and 5) fast band hopping. For example, in a frequency-hopping direct-conversion receiver, imperfections and mismatches in the RF chain result in undesired signal, as well as a fixed noise at the hopping frequency.

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Chapter 3

Introduction to UWB Low-Noise Amplifier

3.1 Broadband Amplifiers

The cost and integration advantages of CMOS technology have motivated extensive studies in the high speed CMOS design for wireless applications. Recently, many wideband LNA designs in CMOS technology have been reported [11]−[20]. The wideband LNA designs can be classified as multi-band LNAs, distributed amplifiers (DA), and broadband noise canceling LNAs. Among wideband LNA designs, distributed and common-gate amplifiers suffer from high noise figure. Alternatively, the feedback amplifier topology provides wide bandwidth while reducing the gain of the circuit. Another important property of the negative feedback is the suppression of the nonlinearity. However, in feedback circuits the stability may suffer if the loop gain is too high which the phase margin reaches -180° or the phase margin is so much that the feedback becomes positive. Therefore, compensation techniques are required to eliminate the instability problem. In the noise canceling technique reported in [21], 5 inductors are used and the noise figure is 4.5−5.1 dB from 1.2−11.9 GHz with 20 mW power consumption, which makes it unattractive for low cost, low power applications. In [22], several narrowband amplifiers with different resonance frequencies are cascaded. Therefore, the resulting multistage
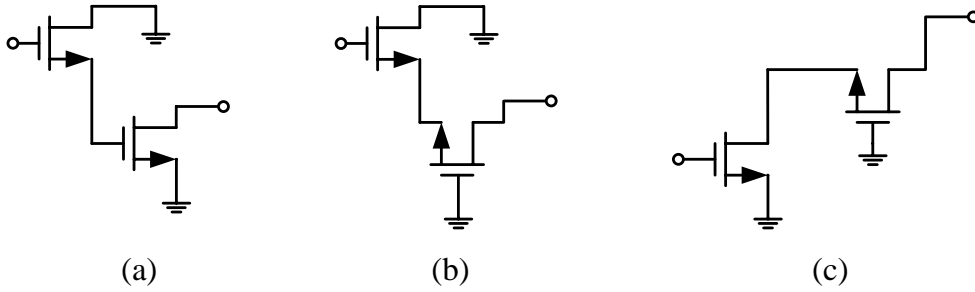
Figure 3.1: Wideband two-stage amplifiers, (a) A source follower driving a common-source amplifier, (b) A source follower driving a common-gate amplifier, (c) A common-source amplifier drives a common-gate amplifier.

amplifier provides a broadband response. This circuit required 8 inductors in a differential architecture and since many stages are cascaded it is prone to poor linearity and stability problems.

It is well known that the amplifier frequency response suffers from Miller feedback capacitance C_μ and a severe gain-bandwidth trade-off is required. However, the two-stage amplifiers shown in Fig. 3.1 suffer less from the Miller effect. In Fig. 3.1(a), a source follower derives a common-source amplifier, thus lowering the source resistance seen by the Miller capacitor. In Fig. 3.1(b), a source follower drives a common-gate amplifier, rising the input impedance of a basic common-gate amplifier without drastically altering the gain. This topology is also recognized as a differential amplifier driven by a single-ended input.

The Third amplifier, shown in Fig. 3.1(c), is a cascade of a common-source and common-gate amplifier, which is widely known as cascode topology. This amplifier is simple and elegant as it provides both voltage and current gain. Since the devices can be stacked, the DC current is shared by the two stages, resulting in low-power amplifier block. These schematics are the basic idea on the broadband amplifier design, now lets move on to a more detailed version of the design. In the amplifier shown in Fig. 3.2, the voltage gain across the Miller capacitor can be made as small as desired by sizing
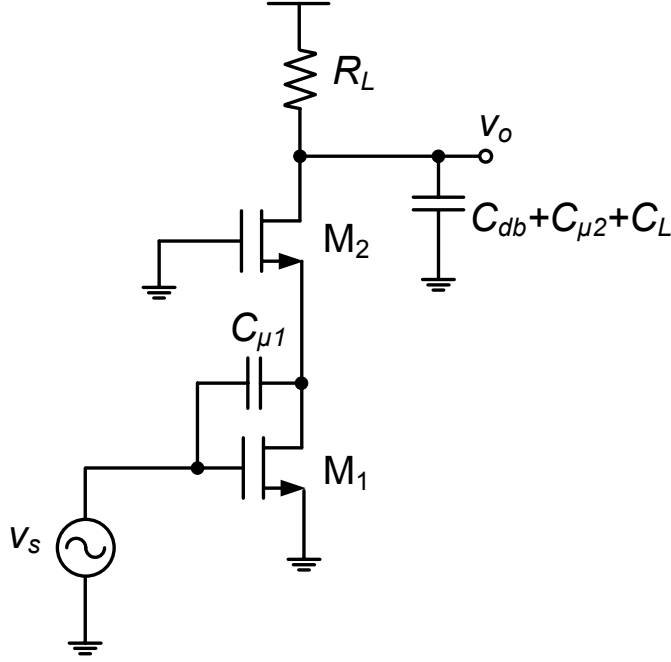
Figure 3.2: A resistive load cascode amplifier does not suffer from Miller effect.

the cascode transistor at the cost of loading amplifier with a non-dominant pole. In a well-balanced design, the dominant pole is due to the output of the amplifier

$$\omega_{-3dB} = \frac{1}{R_L C_o} \qquad \text{(Eq. 3.1)}$$

where $C_o = C_{\mu2} + C_{db} + C_L$. This capacitance is independent of the gain of the amplifier since the gate terminal of M_2 is fixed at AC potential. The cascode boosts the gain of the amplifier by allowing a larger load resistance ($g_m r_o^2$) for a given bandwidth. The gain-bandwidth product of the amplifier is then bounded by

$$A_v \times \omega_{-3dB} = \frac{g_m}{C_{\mu2} + C_{db} + C_L} \approx \frac{g_m}{C_L} \qquad \text{(Eq. 3.2)}$$

In theory, this amplifier has a gain-bandwidth product approaching a significant fraction of the ω_T of the device.

There are few problems with this amplifier. First, in terms of the gain, we have to pay with headroom since a larger load resistance R_L consumes larger DC headroom. This

may lead to unreasonably high supply voltage. In most applications, we do not have control over the supply due to the intrinsic breakdown in a transistor. Higher f_T device also have lower breakdown voltage, leading to a natural limit to the gain of the amplifier. For example, 130 nm CMOS technology may limit the supply to 1.3 V. In analog circuit the voltage headroom is usually solved by active load. Thus the upper limit of the gain is set by maximum current or power consumption. In addition, active load has several drawbacks. First it further limits the output swing of the amplifier since operation into triode region should be avoided for both the load and the cascode transconductance device. Furthermore, the non-linearity of the load degrades the linearity of the amplifier, leading to excess distortion.

3.1.1 Tuned Amplifiers

The RLC loaded amplifier shown in Fig. 3.3(a) solves several of the headroom problems of the Fig. 3.2. In Fig. 3.3(a), a single transconductance device drives a shunt RLC load, which results in

$$A_{v,max} = -g_m Z(j\omega) = \frac{-g_m}{Y(j\omega)} \qquad \text{(Eq. 3.3)}$$

In order to maximize the gain, we have to employ high-Q inductors in the load and omit the resistor load R_L. Assuming the Q-factor is dominated by the inductor, the peak gain is

$$A_{v,\text{max}} \approx -g_m \left(R_{LP} \right) = -g_m Q_L.\omega L \qquad \text{(Eq. 3.4)}$$

where R_{LP} is the equivalent parallel resistance of the inductor L. The gain is maximized at a fixed bias current and frequency is increased by maximizing the $Q_L \times L$ product. So, in theory, there is no limit to the voltage gain of the amplifier as long as the quality
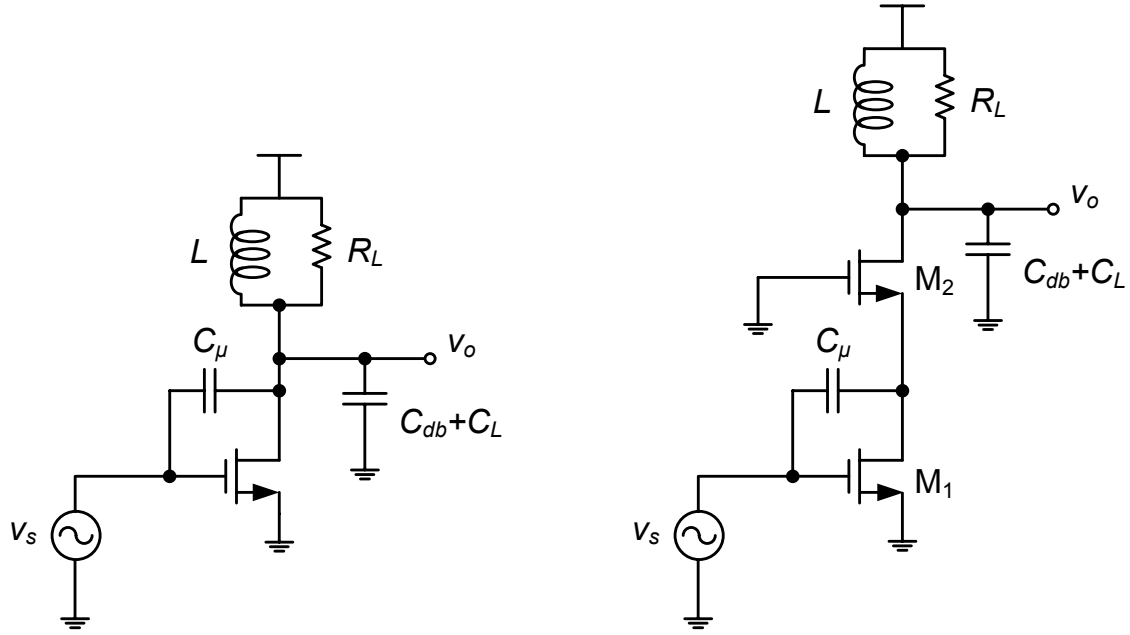
Figure 3.3: (a) A single stage LC tuned amplifier, (b) A cascode LC tuned amplifier.

factor Q_L can increase. Note, that the parasitic capacitances of the circuit are resonated by the shunt inductor. In other word, L is chosen such that

$$LC_{eff}\omega^2 = 1 \qquad \text{(Eq. 3.5)}$$

where $C_{eff} = C_{db} + (1 - |A_v^{-1}|)C_\mu + C_L$. The ability of this circuit to tune out the parasitic capacitance is the major advantage of the tuned amplifier. The other important advantage of this circuit is that there is practically no DC voltage drop across the inductor, allowing very low-supply voltage operation. Another less obvious advantage is the improved voltage swing at the output of the amplifier. Usually the voltage swing is limited by the supply voltage and $V_{DS,sat}$ of the amplifier. In this case though, the voltage can swing above the supply, since the DC voltage drop across the inductor is zero. Beside the advantage of boosting output impedance and maximizing the Q of the load, cascode device in Fig. 3.3(b) solves the stability issue of the circuit.

It is interesting to note that the bandwidth of the amplifier is still determined by the RC time constant at the load. The bandwidth is given by
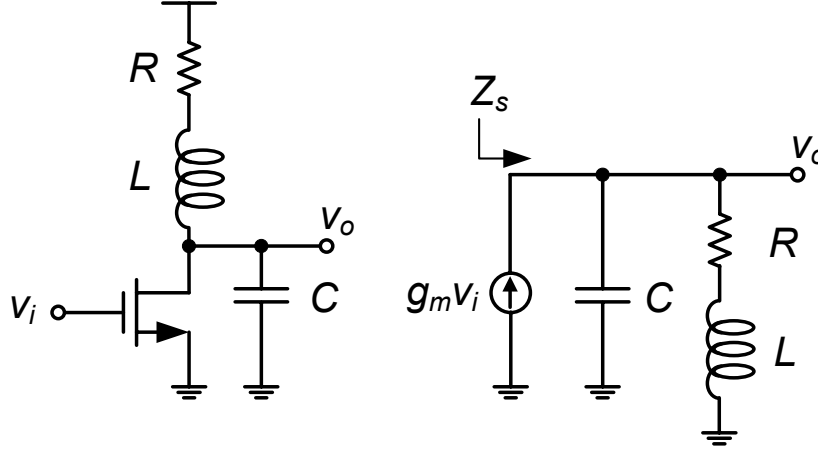
Figure 3.4: (a) A common-source amplifier with a shunt-peaking load, (b) Equivalent circuit for the shunt-peaking amplifier.

$$BW = \frac{\omega_0}{Q} = \frac{\omega_0}{\omega_0 RC} = \frac{1}{RC} \qquad \text{(Eq. 3.6)}$$

The ultimate sacrifice for the high-frequency operation in a tuned amplifier is that the amplifier is narrowband with zero DC gain. In fact, the larger is the Q-factor of the tank, the higher is the gain and the lower the bandwidth. To get some of the bandwidth back it requires other techniques, such as shunt peaking [23] and distributed amplifiers [24].

3.1.2 Shunt and Series Peaking

As shown in Fig. 3.4(a), in the simplest from, a load consisting of a resistor and an inductor in series lead to a zero in the transfer function. This can be used to cancel the pole of the transfer function and within a band of frequencies create a flat-frequency response. With reference to Fig. 3.4(b), one can get

$$Z(s) = (sL + R) \parallel \frac{1}{sC} = \frac{R\left(1 + s\frac{1}{R}\right)}{1 + sRC + s^2 LC} \qquad \text{(Eq. 3.7)}$$

This equation can be written in normalized form with m as the ratio of two time constant

$$m = \frac{RC}{L/R} \qquad \text{(Eq. 3.8)}$$

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letting $\tau = L/R$ we have

$$Z(s) = \frac{R(1 + s\tau)}{1 + s\tau m + s^2\tau^2 m} \qquad \text{(Eq. 3.9)}$$

and by solving the above quadratic equation [25], the following equality is achieved

$$\frac{\omega}{\omega_1} = \sqrt{\left(1 + m - \frac{m^2}{2}\right) + \left(1 + m - \frac{m^2}{2}\right)^2 + m^2} \qquad \text{(Eq. 3.10)}$$

The maximum bandwidth obtainable occurs for $m = \sqrt{2}$ or a bandwidth boost of 85% [23], [25]. This comes at the expense of 20% peaking. A good compromise value occurs for $m = 2$, which leads to only 3% peaking and a bandwidth of 82%. Finally, in a broadband application where a linear phase or flat delay response is desired, the optimum value of $m \approx 3.1$ is the choice to get 57% bandwidth enhancement. Although bandwidth is improved but peaking still is high.

Another example to obtain a wideband response is to use series peaking technique as shown in Fig. 3.5 [2]. Compared to a common-source (CS) LNA, a common-gate
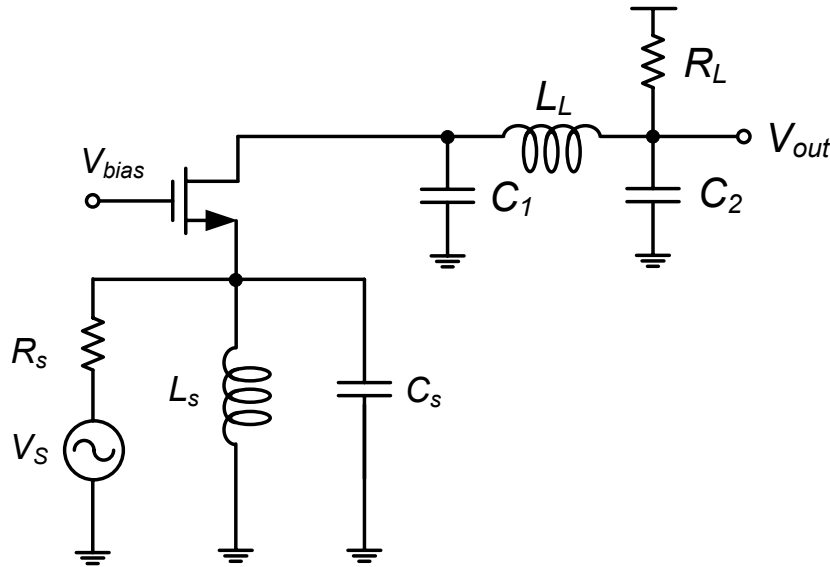
Figure 3.5: Series peaking in a common-gate low noise amplifier with stagger compensation [2].

(CG) LNA offers design simplicity, low power, and good linearity. In the common-gate LNA, the input match condition ($g_m = 1/R_s$) keeps the size of the transistor small so the gate-source and gate-drain capacitances also remain small. As the value of R_s is fixed (50 Ω), R_L is necessarily large for high gain product. Because of high R_L, together with the total load capacitance C_2, sets a bandwidth constraint, which required a technique for bandwidth extension. Thus, a low-Q series-peaked inductor is utilized at the output for a broadband response. The capacitor C_s is tuned out by a source inductor L_s at the resonant frequency ω_s. L_s and C_s form a shunt parallel resonant network with $Q = \omega_s C_s R_s / 2$ [2]. A low Q shunt network for the input suggests a possible broadband impedance match. The fundamental difference between the input matching networks is that the CS-LNA uses series resonant while the CG-LNA uses parallel resonant. By proper sizing the source inductor L_s and the input transistor (W/L), ω_s is optimized to meet the necessary specifications over the entire band, $3.1-10.6$ GHz.

3.1.3 Wideband Input Matching and Reactive Series Feedback

Since the input matching circuit can affect performance of the LNA, so it is important to design a proper matching network in order to cover a wide range of frequency. Wideband impedance matching was first introduced by Bode [26] and Fano [27] to enhance the bandwidth of the antenna. Fano's method is a general solution to enhance the bandwidth of the narrowband circuits. Therefore, it is possible to extend the bandwidth of the narrowband LNA.

Consider the second-order low-pass ladder filter as two port network in Fig. 3.6. Under the resonance condition, the input impedance of the network is real and equals to R. Therefore, the values of L and C are calculated as

$$L = \frac{R}{\omega_0}$$
$$C = \frac{1}{\omega_0 R} \qquad \text{(Eq. 3.11)}$$

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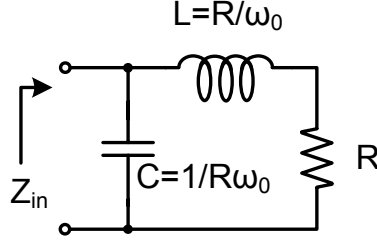
Figure 3.6: Second-order low-pass ladder filter.
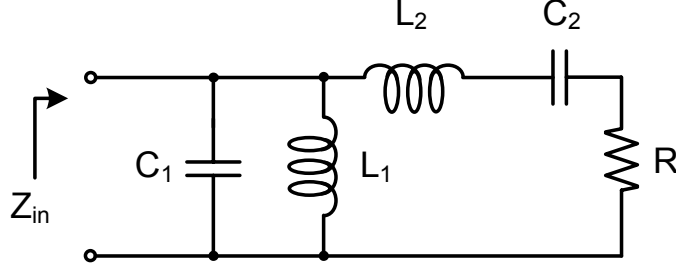
Figure 3.7: Fourth-order bandpass ladder filter.

Using the low-pass to bandpass transformation, the series inductor transformed to series LC, and shunt capacitor transforms to parallel LC network. Transforming the second-order filter in Fig. 3.6, results in a fourth-order filter, shown as shown in Fig. 3.7. The new value of the capacitors and resistors are determined as

$$L_1 = (\omega_2 - \omega_1)/C\omega_0^2 \approx \frac{R}{\omega_1} \qquad \text{(Eq. 3.12)}$$

$$C_1 = C/(\omega_2 - \omega_1) \approx \frac{1}{R\omega_2} \qquad \text{(Eq. 3.13)}$$

$$L_2 = L/(\omega_2 - \omega_1) \approx \frac{R}{\omega_2} \qquad \text{(Eq. 3.14)}$$

$$C_2 = (\omega_2 - \omega_1)/L\omega_0^2 \approx \frac{1}{R\omega_1} \qquad \text{(Eq. 3.15)}$$

where ω_1, ω_2, and ω_0 are the low band, high band, and resonance frequency of the series and parallel devices, respectively. Therefore, the resulted bandpass network can be used as a wideband matching network, to design a wideband LNA.

Input matching network often must convert a predominantly imaginary load impedance to a real value. Consider the circuit shown in Fig. 3.8(a). At moderate frequencies the
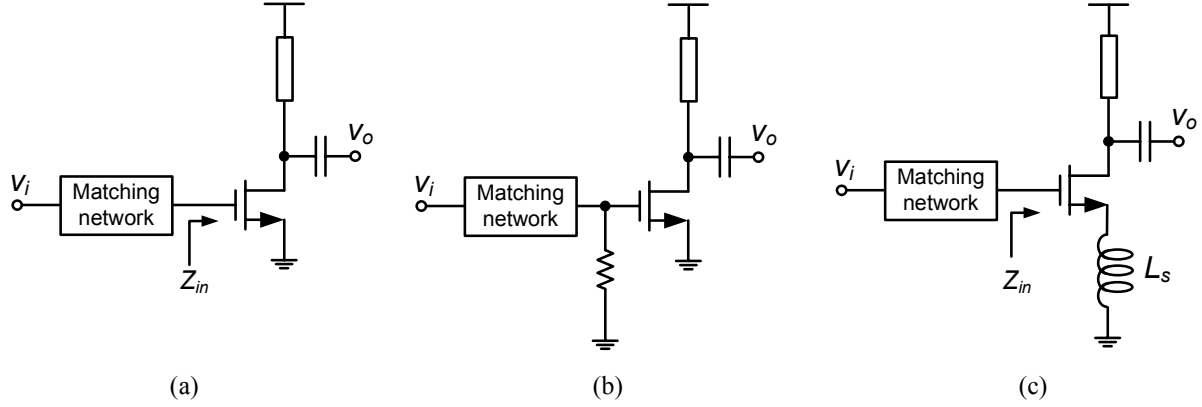
Figure 3.8: (a) Matching network is used to achieve real value, (b) A simple solution is to simply terminate the matching network with a physical resistor, (c) A more elegant solution uses a feedback synthesized resistor input match.

input is dominated by C_{gs}. We need to transform the input capacitance to a real load resistance. Any real MOS amplifier has a real component, which contributes to the input impedance. If the transistor layout has ample fingers to minimize the physical polysilicon gate resistance, the remaining gate-induced channel resistance is given by $1/5g_m$ [23]. Thus the Q-factor of the input of the MOS transistor is given by

$$Q_{gate} \approx \frac{5g_m}{\omega C_{gs}} = 5\frac{\omega_T}{\omega} \qquad \text{(Eq. 3.16)}$$

At moderate frequencies $\omega \ll \omega_T$, this is a high-Q input impedance. If we resonate out this capacitor (C_{gs}) with a shunt inductor, the resulting shunt resistance $Q^2 R_i$ is too large to match to the low-source resistance. On the other hand, if we use a series inductor, the input resistance is simply the equivalent series resistance of the inductor R_i, too small to match. One explicit way is to add resistor to the gate, as shown in Fig. 3.8(b), but this method will add noise to the circuit. A more elegant solution is to add an inductor to the source of the amplifier, shown in Fig. 3.8(c). The action of this feedback produces a term which in resonance becomes purely real as

$$\Re(Z_{in}) = R_{in} = \frac{g_m L_s}{C_{gs}} = \omega_T L_s \qquad \text{(Eq. 3.17)}$$

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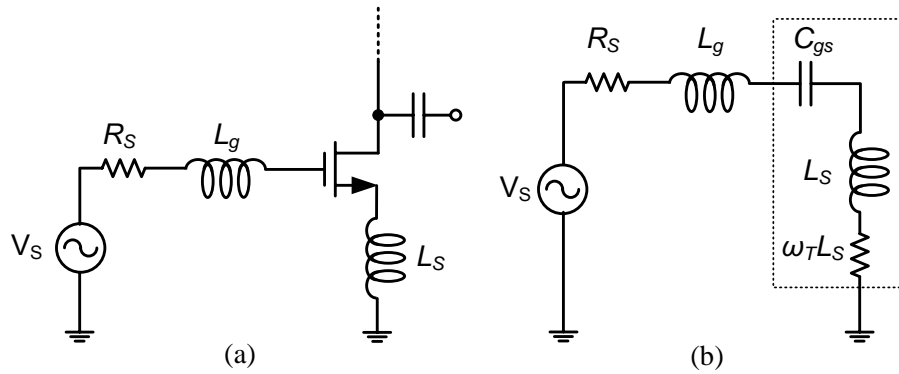
Figure 3.9: (a) The complete input-matching requires a gate inductor L_g to resonate with the capacitor C_{gs}. (b) the equivalent circuit for the input match is a series RLC circuit.

By controlling the value of the L_s, we can control the input impedance. We can also vary the ω_T of the device by placing a capacitor in the shunt with C_{gs}.

It is interesting to observe that the source impedance in effect drives a series RLC circuit, shown in Fig. 3.9(a) with equivalent circuit in Fig. 3.9(b). The inductively degenerated transistor in Fig. 3.9(b) follows the same concept in Fig. 3.7. The bandwidth of the matching stage of the inductively degenerated amplifier is set by the Q-factor of the input. Since the source impedance is fixed, there is little freedom in controlling the Q-factor of the input stage. But many applications require larger bandwidth. For example an ultra-wideband (UWB) amplifier needs a $3-8$ GHz band. Therefore, this input matching is not suitable for a wideband input matching, and a filter with higher order is needed.

3.1.4 Shunt-Shunt Feedback

Consider a simplified resistive-feedback amplifier, as shown in Fig. 3.10(a). A simple single stage amplifier is designed with shunt-shunt feedback resistor, R_F. The equivalent small-signal model of the transimpedance amplifier is shown in Fig. 3.10(b), where g_m represents the transconductance of the transistor. Using the samll-signal model in Fig.

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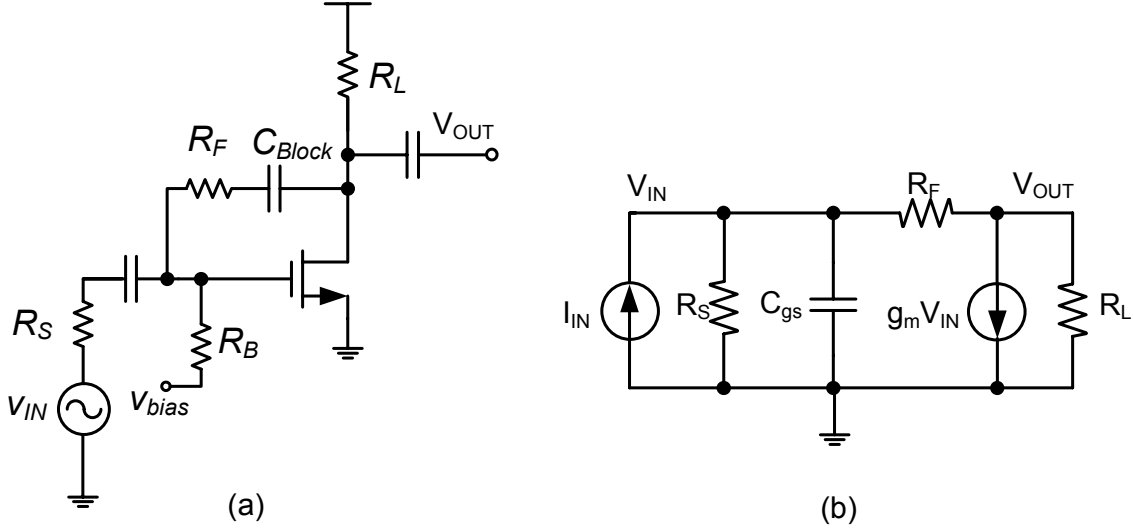
Figure 3.10: (a) Simplified schematic, and, (b) small-signal model of a shunt-shunt feedback amplifier.

3.10(b), the voltage gain of the amplifier can be derived as [28]

$$Av = \frac{V_{out}}{V_{IN}} = -\left(g_m - \frac{1}{R_F}\right)(R_L \parallel R_F) \tag{Eq. 3.18}$$

Shunt-shunt feedback reduces the input impedance of the amplifier by a factor of $(1 + af)$ and the input impedance of the amplifier is

$$R_{in} = \frac{R_S \parallel R_F}{1 + af} \tag{Eq. 3.19}$$

$$a = -(R_S \parallel R_F)\, g_m\, (R_L \parallel R_F) \tag{Eq. 3.20}$$

$$f = -\frac{1}{R_F} \tag{Eq. 3.21}$$

where a is the open-loop transimpedance gain and f is the feedback factor. For the input impedance matching, R_{in} should be equal to $R_S/2$, where in this case af is just below 1, which also ensures the stability condition. In order to achieve low noise figure in this architecture, high open-loop gain is required together with good input matching. The open-loop bandwidth also has to be high to achieve high linearity at high frequencies. The noise figure contribution of each noise source to the total output noise is calculated

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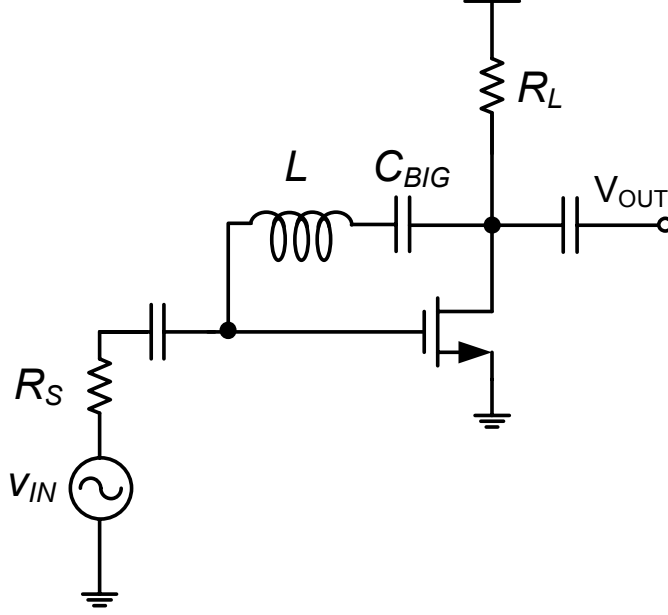
Figure 3.11: LC shunt-shunt feedback technique.

as [28]

$$NF \approx 1 + \frac{\gamma g_m}{R_S g_m} + \frac{1}{R_S R_L g_m^2} + \frac{4R_S}{R_F} \left(\frac{-1}{1 + \frac{R_S + R_F}{(1 + g_m R_S) R_L}} \right)^2 \qquad \text{(Eq. 3.22)}$$

where γg_m is the noise excess factor of the transistor. The calculation of (Eq. 3.22) shows that a large feedback resistor R_F reduces the noise figure contribution. A high R_F requires a high open-loop gain for input matching, which leads to high power consumption. Although, resistive feedback amplifier can achieve high gain and reasonably low noise figure, circuit techniques are required to improve the power consumption.

Another alternative approach to implement the shunt-shunt feedback is to use LC network instead of RC network. This technique uses an inductor L to resonate out the gate-drain capacitor C_{gd} of the transistor to improve the reverse signal flow (coupling) from output to the input port. A sever drawback with this architecture is the size of the inductor and capacitor used for the feedback path. Normally, the value of the inductor should be very high to be able to resonate out the parasitic capacitor C_{gd}. Furthermore,

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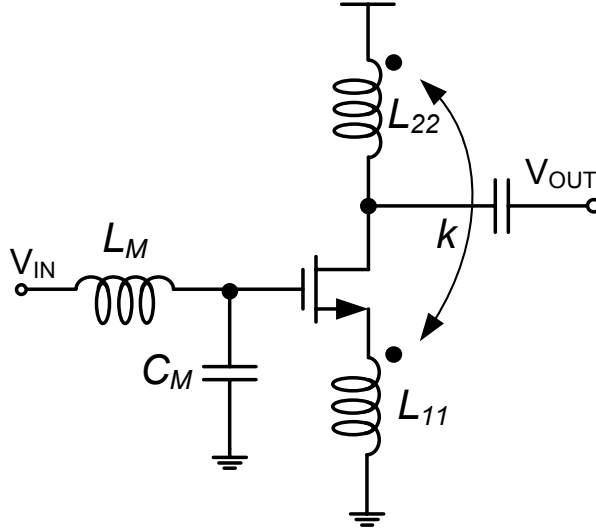
Figure 3.12: transformer-feedback technique [3].

a big value of C_{BIG} is required, which loads the drain and gate terminals of the transistor. This would reduce the forward gain through the transistor transconductance.

In [3], a transformer-feedback technique is proposed, which introduces magnetic coupling between drain and source inductors of a common-source transistor, as shown in Fig. 3.12. In this technique, a portion of the output signal is fed back through transformer, which effectively cancels the coupling from output to the input via Miller capacitor C_{gd} capacitor. The magnetic coupling between the input and output using transformer adds negative feedback. An increase in drain current causes the ac voltage across the secondary L_{22} to increase, and simultaneously increases the voltage across the primary L_{11} in opposite direction, which is due to the wiring direction of the transformer. This event causes V_{gs} to decrease, which is a negative feedback. The transformer-feedback can be can be used as a wideband technique, which the bandwidth is restricted by the bandwidth of the transformer. For a given LNA design, the transformer turns ratio n is often constrained by linearity, gain, and noise specifications. In this design, the coupling coefficient k is the extra degree of freedom that can be adjusted to obtain desired bandwidth of the LNA. The architecture in Fig. 3.12 can be implemented differentially to reduce the effect of
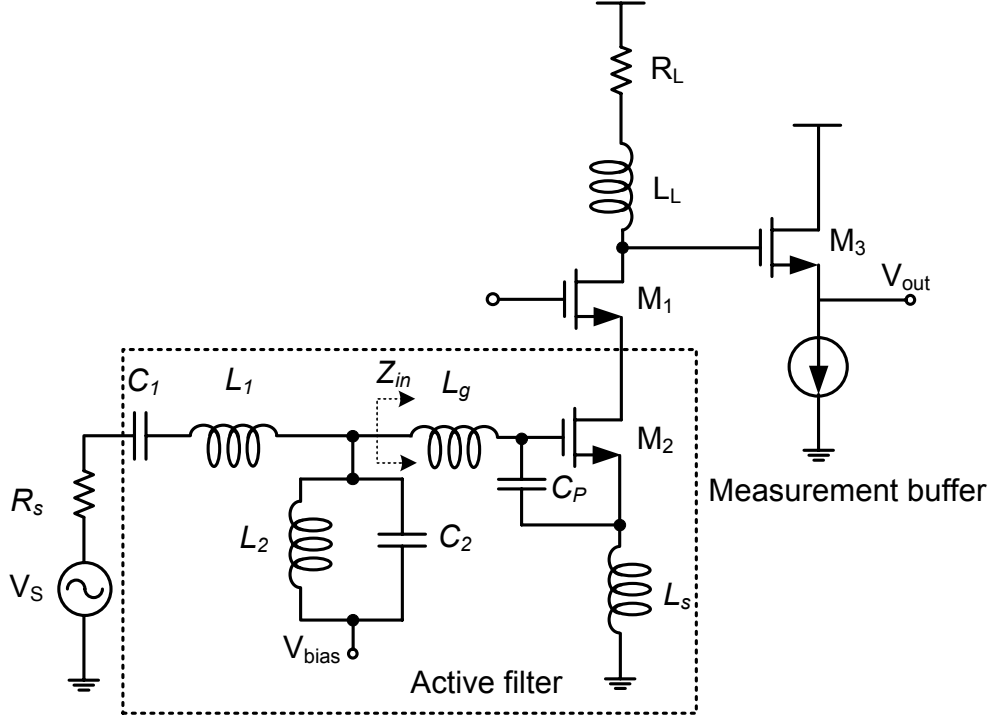
Figure 3.13: An ultra-wideband amplifier using Chebyshev active filter [4].

ground path parasitics and to increase common-mode rejection. Therefore the primary and secondary inductances are implemented as a differential transformer with magnetic coupling M. The input matching network is performed using L_M and C_M network, which L_M is implemented off-chip.

A broadband amplifier is shown in Fig. 3.13, which employs a three-section Chebyshev active filter at input. The series RLC network formed by the transconductance stage forms a third section of the filter, which R is $\omega_T L_S$ series resistance in the source of transistor, shown before in 3.9(b). The bandwidth of the matching stage of the inductively degenerated amplifier in Fig. 3.13 is very depended on the Q factor of the input Chebyshev filter. The input impedance of the MOS transistor with inductive degeneration is achieved as [4]

$$Z_{in}(s) = \frac{1}{s\left(C_{gs} + C_p\right)} + s\left(L_s + L_g\right) + \omega_T L_s \qquad \text{(Eq. 3.23)}$$

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where $\omega_T = g_m/(C_{gs} + C_p) = g_m/C_t$. This network is embedded in the Chebyshev structure to form the input matching network. The parallel resonance occurs between L_s and C_{gs}. The second series resonance, on the other hand, occurs between L_g and the equivalent capacitance resulting from the parallel combination of L_s and C_{gd} at frequencies higher than the parallel resonance.

From noise analysis perspective, the noise contribution of the input network is due to the limited quality factor Q of the integrated inductors. The noise optimization relays on achieving the highest Q for a given inductance value. The need for high Q inductor to reduce the noise figure account as a drawback for the design. The noise contribution of the transistor M_1 relies on the choice of its width for a given current bias. An minimum noise figure can be achieved once L_s and C_t resonate, and consequently a low noise figure over the entire amplifier bandwidth is obtained.

The voltage gain of the amplifier can be found by $R_s/W(s)$, where W_s is the Chebyshev filter transfer function. The transfer function of the Chebyshev filter is unity in-band and tends to zero out-of-band. So the impedance looking into the amplifier is R_s in-band, and it is very high out-of-band. The overall gain is [4]

$$\frac{V_{out}}{V_{in}} = -\frac{g_m W(s)}{s C_t R_s} \cdot \frac{R_L \left(1 + \frac{s L_L}{R_L}\right)}{1 + s R_L C_{out} + s^2 L_L C_{out}}. \qquad \text{(Eq. 3.24)}$$

where R_L is the total resistance, L_L is the load inductance, and C_{out} is the total output parasitic capacitance at the drain of M_2. The shunt-peaking load is compensating the gain roll off, which in (Eq. 3.24) is set by L_L. The presence of parasitic capacitor C_{out} introduces spurious, which should be kept out-of-band.

The results observed from this design benefits from the use of a ladder-filter input matching network. This LNA achieves wide bandwidth and input matching from $3-10$ GHz [4]. However, this wideband LNA needs too many components, specifically high Q inductors, to form the Chebyshev filter at the input. This drawback adds to the area and the cost of the design.

Chapter 4

Proposed Wideband Low-Noise Amplifier

One of the major challenges in wideband communications systems is the design of a wideband low-noise amplifier. As the first active component in the receiver chain, the LNA should offer sufficient gain and low noise to keep the overall receiver noise figure as low as possible. In most applications, it is desirable to obtain wideband on-chip input matching to a 50 Ω antenna/filter, good linearity, and low power consumption. In addition, gain-flatness over the entire frequency range of interest is necessary to meet the design specifications. These properties are the cornerstones of the wideband LNA design which affect the total broadband communication system characteristics.

This section introduces a T-coil network to achieve wideband input matching and wideband output response. In this technique the parasitic capacitors of the transistors and inherent mutual inductance of the inductors are taken as a part of the design [20]. In this design 3 inductors are used which 2 of inductors are center-tap inductor, to implement a single-ended LNA.

4.1 CIRCUIT DESIGN: THEORY AND PRACTICE

In [4], a Chebyshev type bandpass filter is used at the input of a common-source amplifier in order to provide good matching over a wide bandwidth. These kind of filters neces-
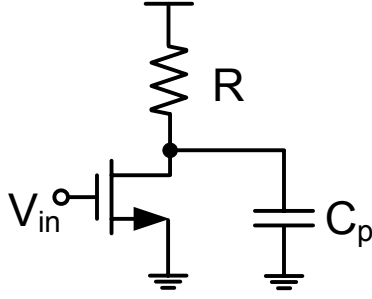
Figure 4.1: Common-source amplifier with output parasitic capacitance C_p

sitate the use of many components which occupy a large area and reduce the circuits integration level. Furthermore, the loss associated with the components deteriorates the noise figure of the circuit. Therefore, techniques to alleviate these issues without degrading performance is required.

In general, when the LNA circuit is cascaded to the next stage, the interstage parasitic reactance attenuates the desired bandwidth of the LNA. For example, in Fig. 4.1 parasitic gate-source capacitance C_p of a mixer or buffer, reduces the circuit performances as it shunts with the output load R of the common-source amplifier. A dominant pole due to the parasitic C_p is created at frequency of $1/RC_p$ which reduces the bandwidth. One way to compensate C_p is to insert an inductor in series with R at the output of Fig. 4.1 to resonate out C_p. However, the existence of resistor R will require extra voltage headroom, which limits the allowable bias current. In the discussions below, different peaking techniques are introduced to improve the bandwidth. Shown in Fig. 4.2(a), a series inductor L across R and C is used to create a series peaking in the frequency response. The series inductor creates a second-order RLC resonant circuit with a resonance frequency of $\omega_0 = 1/\sqrt{LC}$. In this circuit transfer function is not changed by exchanging R and C since L is in series with C in both cases. The transfer function of the series inductive peaking circuit is

$$H_1(s) = \frac{R}{s^2 LC + sRC + 1} = \frac{1}{mR^2C^2} \cdot \frac{R}{s^2 + s/mRC + 1/mR^2C^2}. \qquad \text{(Eq. 4.1)}$$

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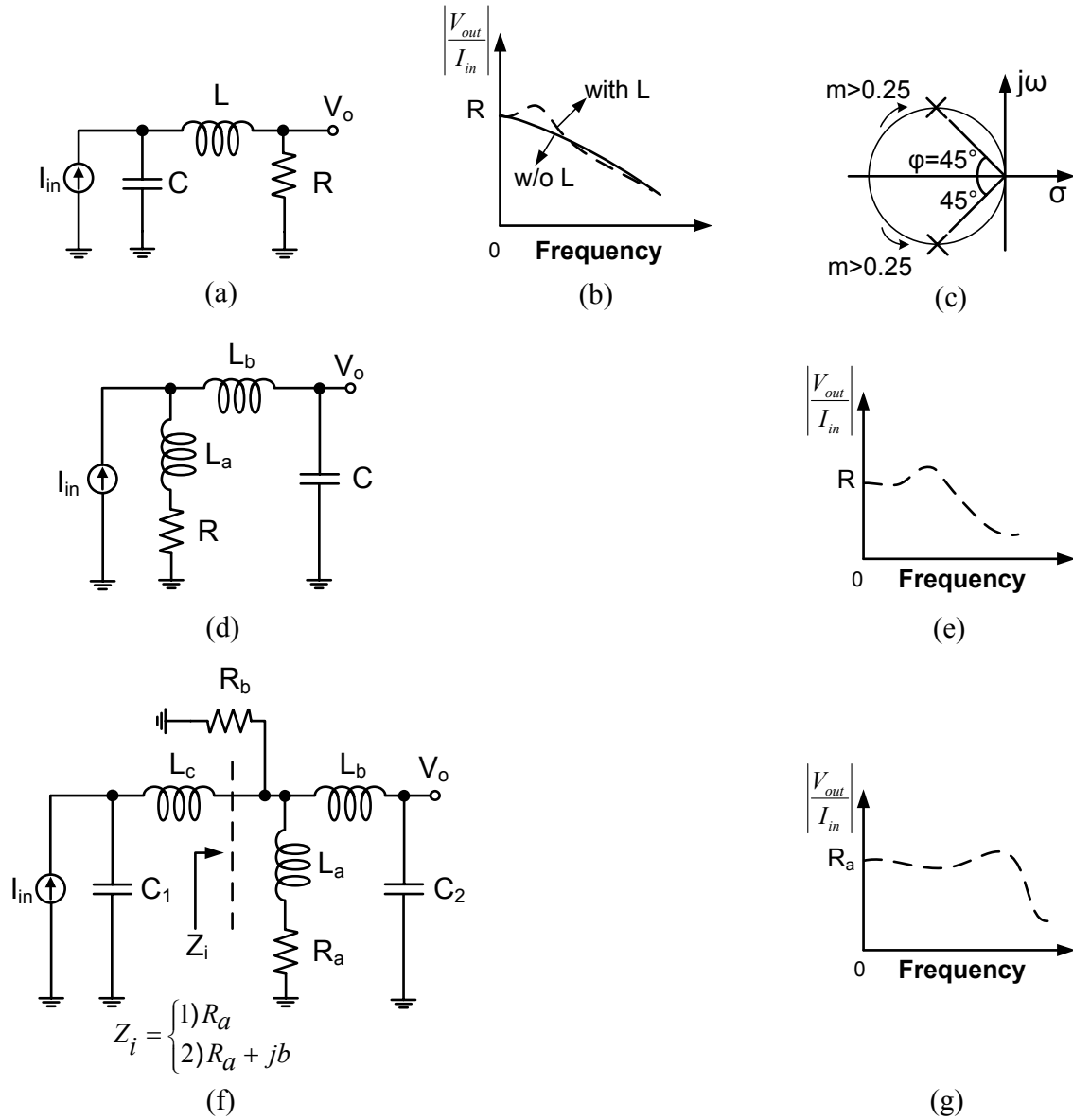
Figure 4.2: (a) Series inductive peaking circuit, (b) frequency response of the circuit (a) with and without L, (c) complex poles location for maximum gain-flatness response, (d) shunt-series inductive peaking circuit, (e) frequency response of the shunt-series peaking circuit, (f) series-shunt-series peaking including a T-coil peaking network, (g) series-shunt-series peaking frequency response.

where $L = mR^2C$, m is a dimensionless parameter that defines the poles location and determines the overdamped response of the filter. From (Eq. 4.1), the complex conjugate

poles are

$$s_{1,2} = -\frac{1}{2mRC} \pm j\sqrt{\frac{1}{mR^2C^2} - \frac{1}{4m^2R^2C^2}} = \frac{1}{2mRC}\left(-1 \pm j\sqrt{4m-1}\right). \qquad \text{(Eq. 4.2)}$$

From the frequency response shown in Fig. 4.2(b), the circuit including the series peaking inductor improves the bandwidth compare to the circuit without L. For this circuit with $m = 0.25$ poles are equal to $s_1 = s_2 = -2/RC$ near to the critically damped response. As the value of m increases ($m > 0.25$) poles become complex conjugate and travel along the real axis towards the $j\omega$ axis, Fig. 4.2(c). If we equate the standard 2nd-order Butterworth poles with (Eq. 4.2), the components values are calculated and maximum gain-flatness response is satisfied. As shown in Fig. 4.2(c), poles angle (φ) should be equal to 45° from origin to get the maximum gain-flatness response [29].

The circuit in Fig. 4.2(a) with two reactance components represents one resonance frequency. The circuits with more than two reactance components have more than one resonance mode. A multi-resonance circuit can be utilized to cover a wider range of frequency than a single resonance circuit. For this reason, the resonance frequencies should be chosen properly to optimize the bandwidth of interest.

Now consider the circuit shown in Fig. 4.2(d). An inductor L_a in series with R adds a shunt peaking to the series peaking L_b, results in a shunt-series peaking circuit which improve the bandwidth. The frequency response of this circuit is shown in Fig. 4.2(e). The transfer function of the shunt-series peaking network is determined as

$$H_2(s) = \frac{V_o}{I_{in}} = \frac{sL_a + R}{s^2 C\left(L_a + L_b\right) + sCR + 1} \qquad \text{(Eq. 4.3)}$$

$$= \frac{1}{C\left(L_a + L_b\right)} \cdot \frac{L_a\left(s + R/L_a\right)}{s^2 + sR/(L_a + L_b) + 1/C(L_a + L_b)}.$$

where from denominator, the complex poles are

$$s_{1,2} = \frac{-R}{2(L_a + L_b)} \pm j\sqrt{\frac{1}{(L_a + L_b)\,C} - \left(\frac{R}{2(L_a + L_b)}\right)^2}. \qquad \text{(Eq. 4.4)}$$

The inductor L_a in series with R adds a real zero $-R/L_a$ to the numerator of the transfer function in (Eq. 4.3). The addition of a zero improves the bandwidth but also peaks the response. To reduce the peaking issue in the frequency response of Fig. 4.2(e), the components values are equated to the standard 2nd-order polynomial normalized Butterworth system. For this reason, let us normalize the transfer function $H_2(s)$ by putting $R = 1$ and $C = 1$ and then

$$L_a = m_1 R^2 C L_b = m_2 R^2 C, \quad m_2 < m_1 \qquad \text{(Eq. 4.5)}$$

where L_a and L_b are selected to get the maximum gain flatness. Note that in this work we are trying to keep an agreement between the bandwidth and the gain flatness.

Combining the circuits in Fig. 4.2(a) and Fig. 4.2(d), a series-shunt-series circuit which involves a T-coil network (L_{a-c}) is resulted in Fig. 4.2(f). The parasitic capacitors C_1 and C_2 are separated by the T-coil network (L_{a-c}). The transfer function of this circuit is the product of the transfer function in (Eq. 4.1) and (Eq. 4.3). For simplicity of the analysis, R_b is neglected (as $R_b \gg R_a$) and two valid cases are assumed. The first case is when the input impedance $Z_i = R_a$, and the second case is when $Z_i = R_a + jb$. For the first case it can be seen intuitively that at low frequencies the inductors short the input to R_a while the capacitors are open. For higher frequencies Z_i contains the imaginary part jb due to the existence of the passive components. So the transfer function for the case 1 and 2 are consecutively as follow

case1:

$$H_1(s) = \frac{R_a/m_1 R_a^2 C_1^2}{s^2 + s/m_1 R_a C_1 + 1/m_1 R_a^2 C_1} \times \frac{m_1 (s + 1/m_1 R_a C_1)/C_2(m_1 + m_2)}{s^2 + s/R_a C_2(m_1 + m_2) + 1/R_a^2 C_2^2(m_1 + m_2)}. \qquad \text{(Eq. 4.6)}$$

case2:

$$H'_1(s) = \frac{(R_a + jb)/m_1 (R_a + jb)^2 C_1^2}{s^2 + (s + 1/C_2 (R_a + jb))/(R_a + jb)(m_1 + m_2)}$$
$$\times \frac{m_1 (s + 1/m_1 R_a C_1)/C_2 (m_1 + m_2)}{s^2 + (s + 1/C_2 (R_a + jb))/C_2 (R_a + jb)(m_1 + m_2)}. \qquad \text{(Eq. 4.7)}$$

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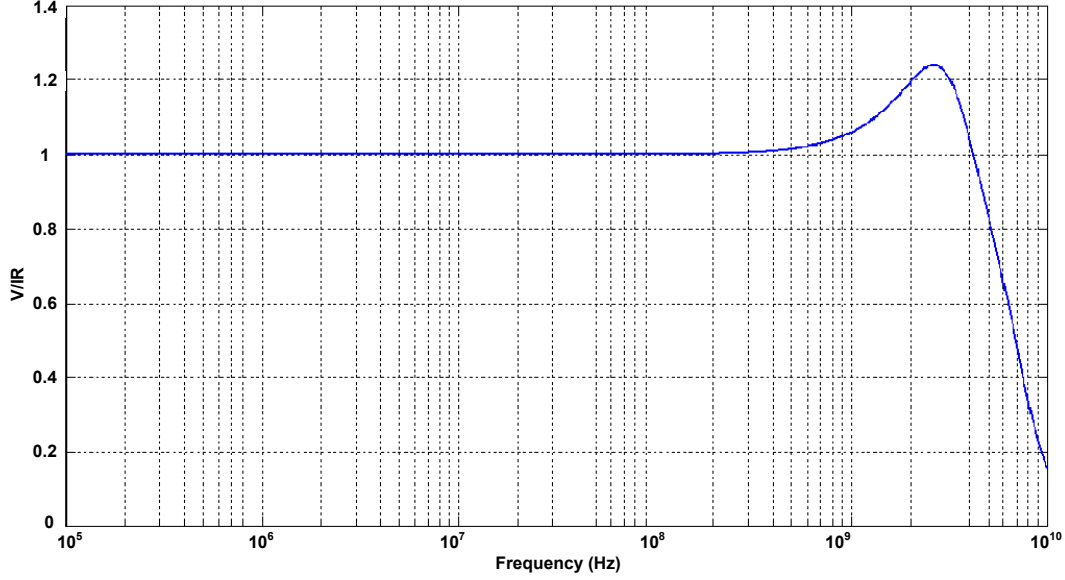
Figure 4.3: Transfer function of the equation (Eq. 4.6), plotted in MATLAB.

The denominator of (Eq. 4.6), includes four poles given by

$$s_{1,2} = \frac{1}{2R_aC_1m_1}\left(-1 \pm j\sqrt{4m_1 - 1}\right). \qquad \text{(Eq. 4.8)}$$

and

$$s_{3,4} = \frac{1}{2R_aC_2(m_1 + m_2)}\left(-1 \pm j\sqrt{4(m_1 + m_2) - 1}\right). \qquad \text{(Eq. 4.9)}$$

In (Eq. 4.6), two left hand complex poles extend the bandwidth much further compared to the poles in (Eq. 4.3), because the circuit in Fig. 4.2(f) represents more than one resonance mode. Assuming $C_2 > C_1$ so poles $s_{1,2}$ are located at higher frequency than poles $s_{3,4}$. Fig. 4.2(g) illustrates the frequency response improvement of the circuit in Fig. 4.2(f). If we replace R_a in (Eq. 4.8) and (Eq. 4.9) by $R_a + jb$, the poles of (Eq. 4.7) are obtained. A similar circuit to Fig. 4.2(f) is presented in [2] which the transfer function of the circuit is normalized to find the relation between the components for maximum bandwidth. The circuit shown in Fig. 4.2(f) is analyzed based on the simple inductors without having any mutual coupling. In our analysis of the Fig. 4.2(f), 3

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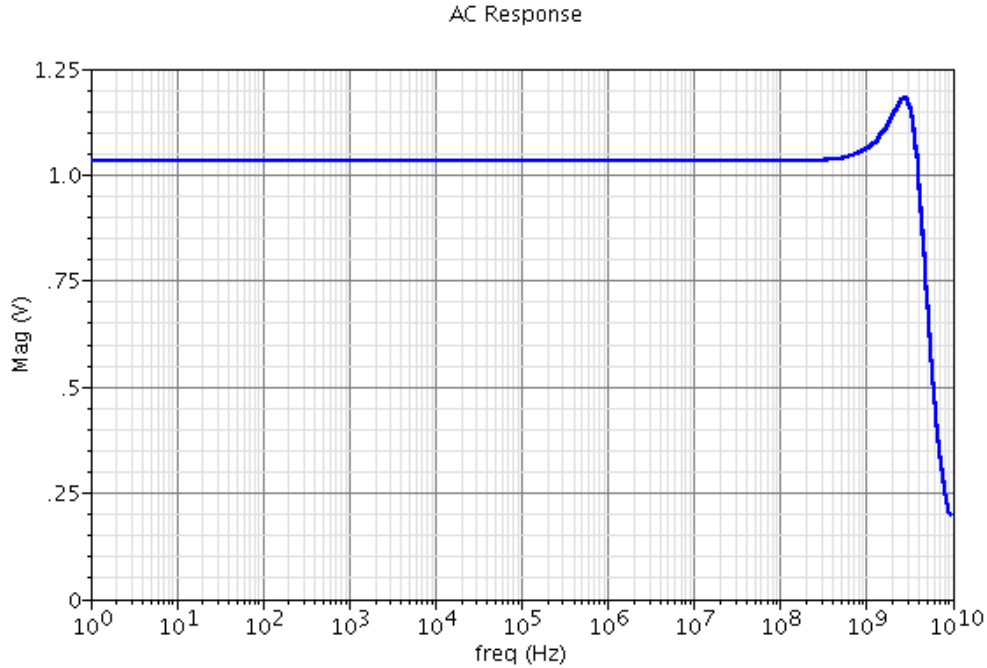
Figure 4.4: Transfer function of the peaking network (Fig. 4.2(f)) using Cadence simulator.

inductors are used while L_b is modeled as the mutual coupling between the inductors L_a and L_c. The series-shunt-series network can be isolated as long as the mutual coupling is modeled properly as an inductor. Since the mutual coupling is modeled as an inductor, the circuit can be further simplified. The final transfer function of Fig. 4.2(f) is a fourth-order equation. The transfer function of the circuit is separated into two paths. The transfer function of Fig. 4.2(f) is plotted in MATLAB (Fig. 4.3) and compared with the simulation of the network in the Cadence simulator (Fig. 4.4) to prove the validity of the calculations. The similarity between these two plots confirms that the transfer function equation of 4.2(f) is correct.

4.2 WIDEBAND AMPLIFIER DESIGN

In this section the series-shunt-series circuit in Fig. 4.2(f) is applied to a common-source amplifier to realize a wideband LNA design.

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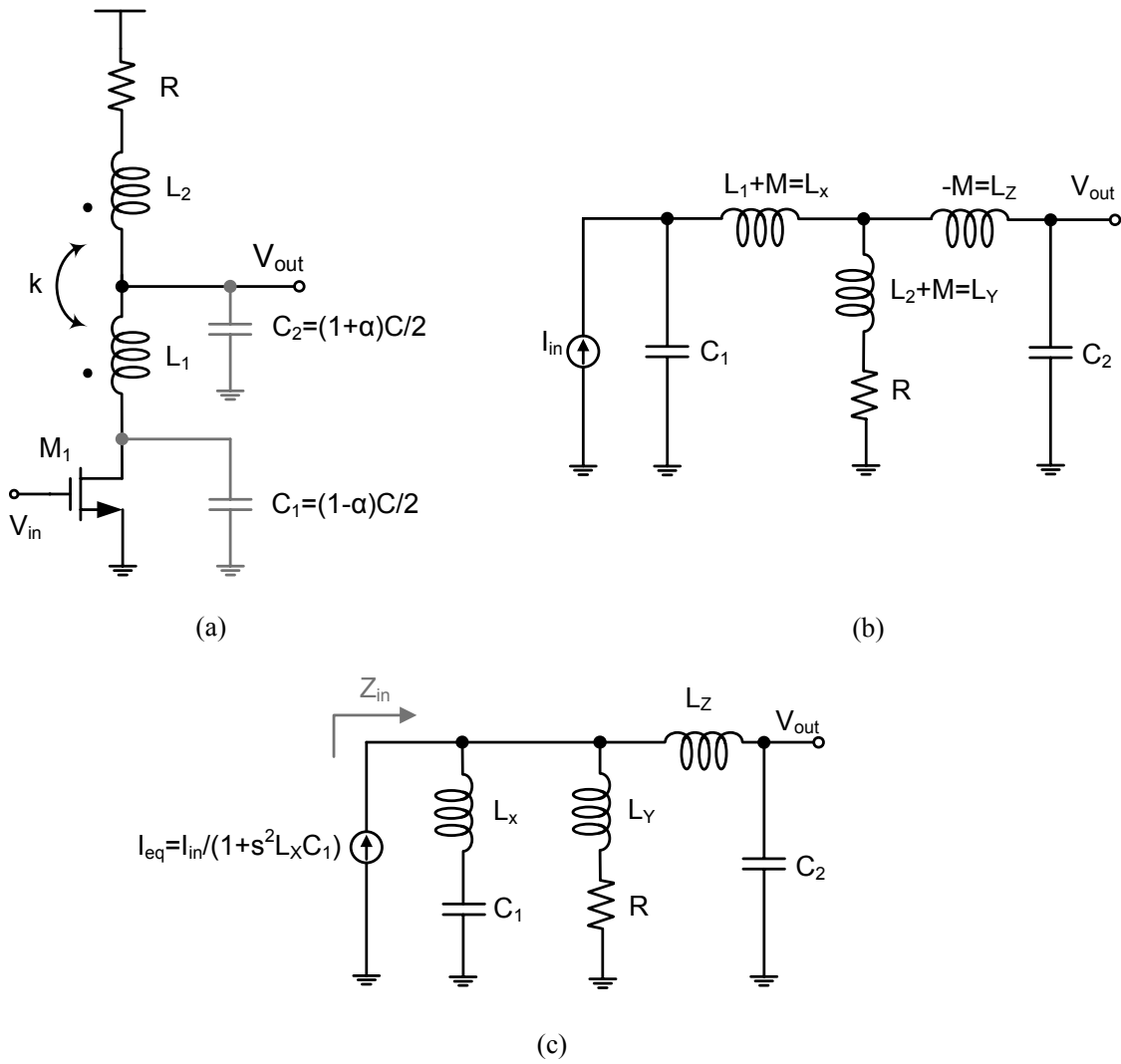
Figure 4.5: (a) Common-source amplifier with symmetric T-coil peaking network, (b) and (c) Simplified small-signal equivalent circuit of the T-coil peaking.

4.2.1 Output Peaking Network

The use of 3 inductors in Fig. 4.2(f) leads to difficulties in the layout. Fortunately, this issue can be resolved through implementation of a center-tap (CT) inductor. The circuit shown in Fig. 4.5(a) is a common-source amplifier incorporating the CT inductor with a magnetic coupling coefficient k between L_1 and L_2 to form the T-coil peaking network at the output network. The basic functionality of this T-coil network is similar to the

circuit in Fig. 4.2(f) that was explained above. The CT inductor is employed to save die area and reduce the loss associated with the inductors. The CT inductor with the negative mutual coupling $(-M)$ leads to greater improvements compare to the circuit in Fig. 4.2(f).

Since only one CT inductor is used in Fig. 4.5(a), less parasitic components are introduced to the circuit. The equivalent small-signal model of the output peaking network is shown in Fig. 4.5(b). Since $C_2 > C_1$ we assume that $C_2 = (1+\alpha)C/2$ and $C_1 = (1-\alpha)C/2$, where $0 < \alpha < 1$. The CT inductor in this network has a symmetrical structure, hence $L_1 = L_2 = L$, $k = M/L$ and from here $L_X = L_Y = L(k+1)$ and $L_Z = -kL$. The mutual coupling between L_1 and L_2 as an extra term can be exploited to modify the bandwidth extension. For an on-chip CT inductor/transformer the k-factor is dependent to the number of layers and the stray of the capacitors between layer to layer. The k-factor is extracted from the inductor model given by the foundry. The k-factor and mutual coupling inductance can be extracted from the impedance and admittance parameters:

$$M = \sqrt{\left(Y_{11}^{-1} - Z_{11}\right) \frac{Z_{22}}{\omega^2}}. \tag{Eq. 4.10}$$

$$k\left(L_1, L_2\right) = \sqrt{\frac{\left(Y_{11}^{-1} - Z_{11}\right) Z_{22}}{\operatorname{Im}\left(Z_{11}\right) \operatorname{Im}\left(Z_{22}\right)}}. \tag{Eq. 4.11}$$

where ω represents the resonance frequency of the CT inductor/transformer. In order to optimize the required gain-flatness over the entire bandwidth, k-factor should be determined precisely. For this reason, the relationship between group-delay and the k-factor of the T-coil network (Fig. 4.5(a)) is simulated in Fig. 4.6. In this simulation the loss of the inductors are included into the circuit model to get more accurate results. As the k-factor increases, flatter group delay over wider bandwidth is resulted. In addition, the total attenuation of the symmetric T-coil network at different frequencies versus k-factor
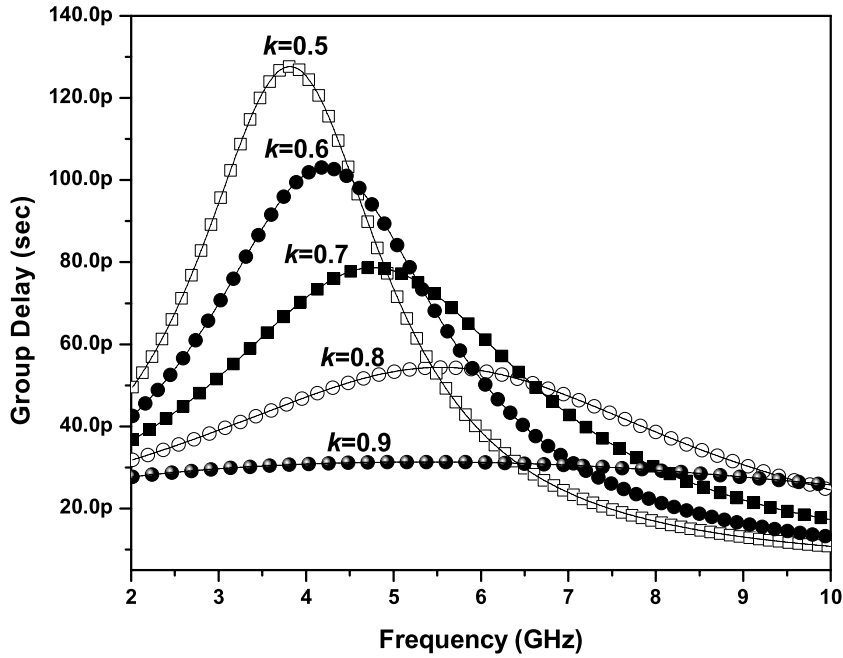
Figure 4.6: Group delay response of the T-coil network.

is plotted in Fig. 4.7. As the frequency increases, the attenuation of the T-coil network increases simultaneously. Therefore, a higher k-factor is required to reduce the attenuation specially at high frequencies. However, the design of a CT inductor to present a very high k-factor is not easy. The reason is that the k-factor is limited by the parasitic capacitances and resistances of the inductor. To eliminate the nonideal characteristic of the inductor, stacked top metal layers are implemented while the center-to-center distance of the turn-to-turn winding should be reduced [30]. More importantly, if the parasitic capacitances of the output CT inductor become significant, more parasitic capacitances are added to C_1, which makes C_1 comparable with C_2. This reduces the desirable bandwidth and makes the bandwidth extension technique inefficient. It is shown in the subsequent section that by increasing C_2/C_1 ratio the bandwidth is further improved. Fig. 4.8 plots the attenuation of the output T-coil network versus frequency for $k=$ 0.5 and 0.9, respectively. The attenuation is more gradual for $k=0.9$ and its deviation from 3 to 8 GHz is about 1.8 dB which is flatter compared to the attenuation of $k=$ 0.5. Now, in order

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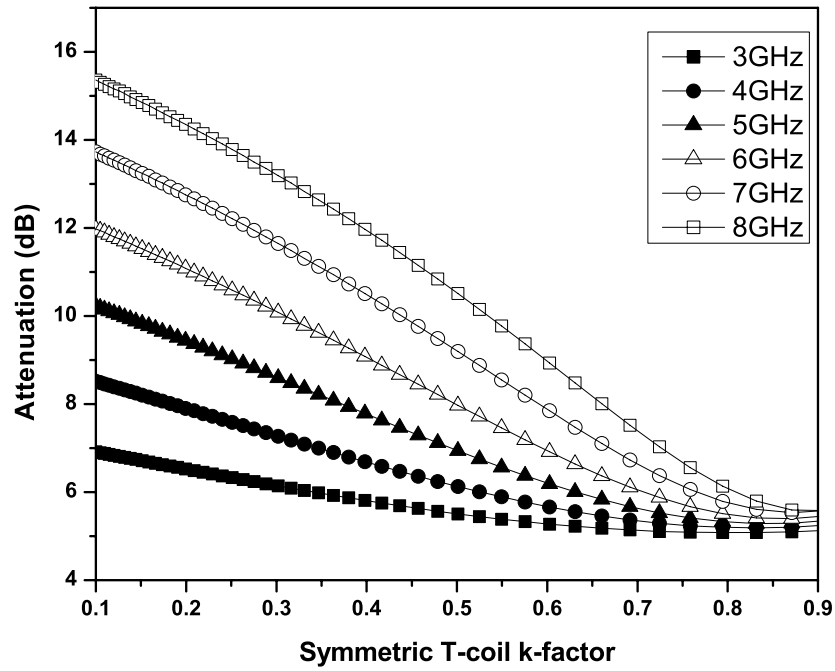
Figure 4.7: Amplitude response of the T-coil network vs. $k-$factor at different frequencies.
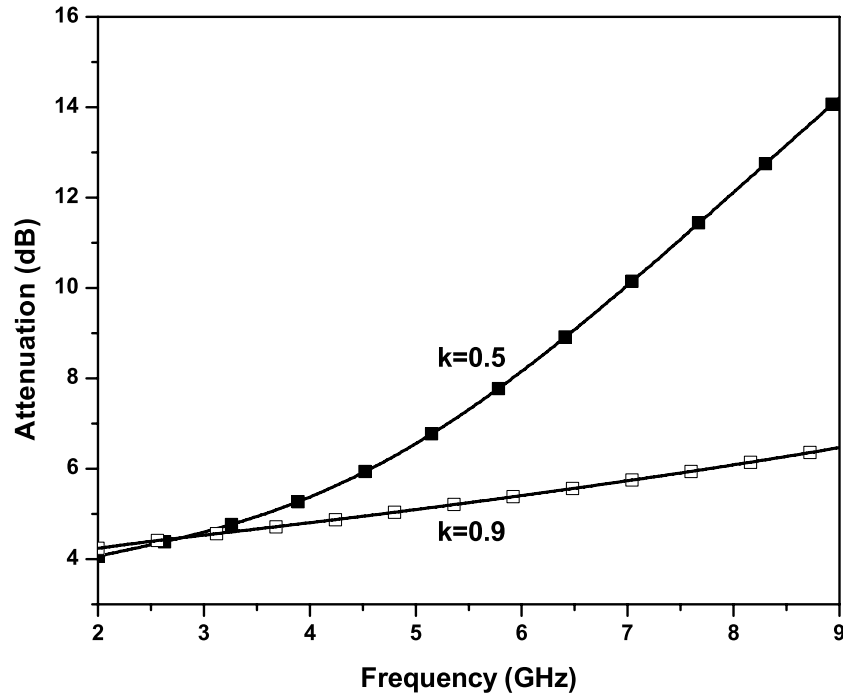
Figure 4.8: Amplitude response of the T-coil network vs. frequency.

to prove the feasibility of the technique explained above, the T-coil peaking network is implemented in a cascode amplifier. Fig. 4.9 shows the complete single-ended cascode LNA with the CT inductor at the input and the output of this circuit. An extra peaking inductor L_L is added into the output peaking network as a part of the load, to prevent the gain roll-off and to improve the gain-flatness. A resistor R at the output load in series with L_L reduces the quality factor of this inductor which extends the bandwidth of the LNA. However, the existence of R causes some drawbacks like peaking in the gain response and additional noise. In order to reduce the peaking in the gain response, a resistive-feedback path is connected across nodes "A" and "B". In Fig. 4.10 the frequency response of the wideband LNA with/without the feedback path is simulated. Clearly, the peaking issues are minimized due to the feedback path effect. That is, R_F moves the complex conjugate poles away from $j\omega$ axis to get $\varphi = 45^o$. Therefore, proper selection of R_F value is critical to minimize the peaking in the frequency response. If the series parasitic resistance of the output inductors are high enough (low Q inductors), R can be removed from the output peaking circuit.

4.2.2   Input Matching Network

Shown in Fig. 4.11 is the equivalent circuit model of the LNA input matching network. The input matching network is implemented using T-coil network, similar to the output peaking network. This technique helps to minimize the number of inductors at the input stage. The input impedance of this circuit is expressed as

$$Z_{IN} = (sL_X + r_X) + \left[sL_Z + \left(\frac{R_F}{1 - A_v} \right) \right] \parallel \left[sL_Y + r_Y + \frac{1}{s(C_{gs} + C_\mu)} \right]. \quad \text{(Eq. 4.12)}$$

where A_v is the open loop voltage of the amplifier, r_X, r_Y are the loss associated with L_X, L_Y, respectively and C_μ is the Miller capacitor. The real part of (Eq. 4.12) is defined as $R_s = \Re(Z_{IN})$ where $\Re(Z_{IN})$ is directly dependant to R_F. Regardless of the loss associated
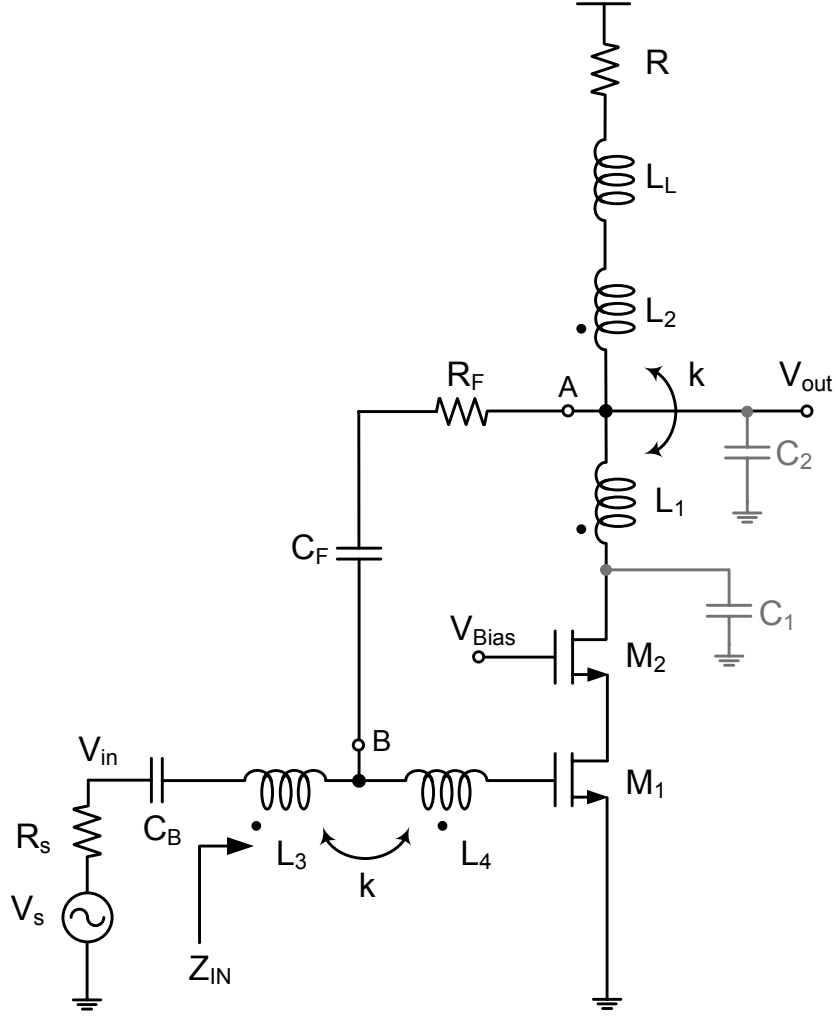
Figure 4.9: Wideband LNA using symmetrical center-tap inductor (biasing circuitry not shown).

with the inductors, the input resistance of the LNA is approximated by $R_{in}=R_F/(1-Av)$, which introduces a low input impedance and reduces the effect of input dominant pole

$$s_{in} = \frac{1}{R_{in}\left(C_B + C_{gs} + C_\mu\right)} = \frac{|Av|}{R_F\left(C_B + C_{gs} + C_\mu\right)}. \qquad \text{(Eq. 4.13)}$$

where $R_{in} \approx R_F/|Av|$ if $Av >> 1$. The input matching network is implemented as bandpass filter. The tuning condition of the filter is dependant to the proper value of the components. For instance, the right selection of the blocking capacitor C_B is very important because a large value of C_B adds to the overall parasitic capacitance at the
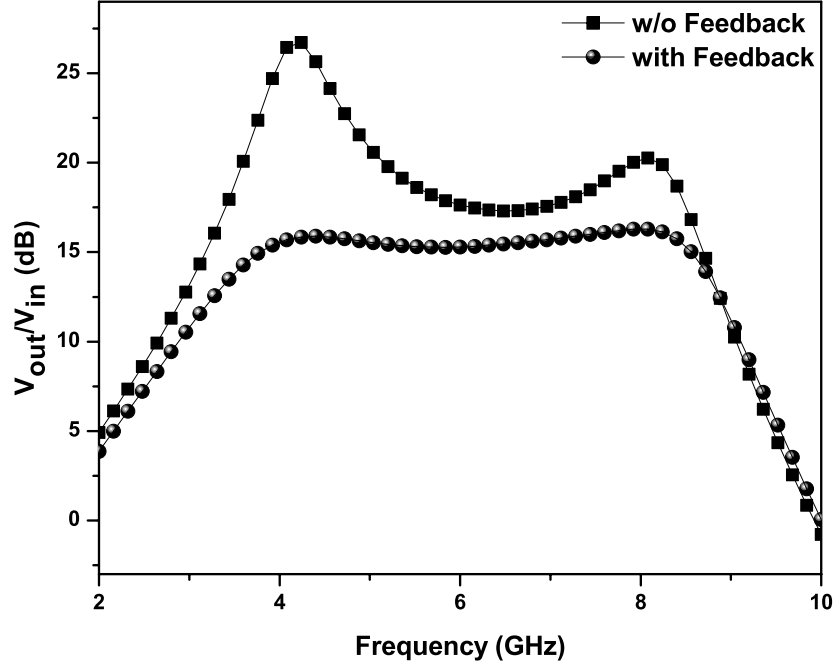
Figure 4.10: Simulated frequency response of the LNA, in here $R = 0$. The wideband LNA with/without feedback path is simulated for comparison, the 3 dB bandwidth is adjusted later.

input, affecting the overall bandwidth of the circuit. A small value on the other hand, has significant AC impedance that leads to the gain reduction.

The quality factor (Q) of the input network is given by

$$Q_T = \frac{1/\omega_0\left((C_{gs} + C_\mu)\,||C_B\right)}{\left[R_s + r_X + r_Y + \frac{\omega_0^2(L(k+1))^2}{R_P}\right]}.$$ (Eq. 4.14)

where resistor $R_P = (R_F/(1 - A_v))\left(1 + Q_{L_Z}^2\right)$ is the parallel equivalent resistance of the inductor L_Z, and ω_0 corresponds to the resonance frequency of the network as

$$\omega_0 = \frac{1}{\sqrt{\left((C_{gs} + C_\mu)\,||C_B\right)\left[L_X + (L_{Z'}||L_Y)\right]}}.$$ (Eq. 4.15)

As k-factor of the input CT inductor increases, the attenuation reduces and the input network bandwidth increases. By tuning R_P in (Eq. 4.14), Q_T of the input network would be tuned and desired input matching can be obtained. Note that the tradeoff

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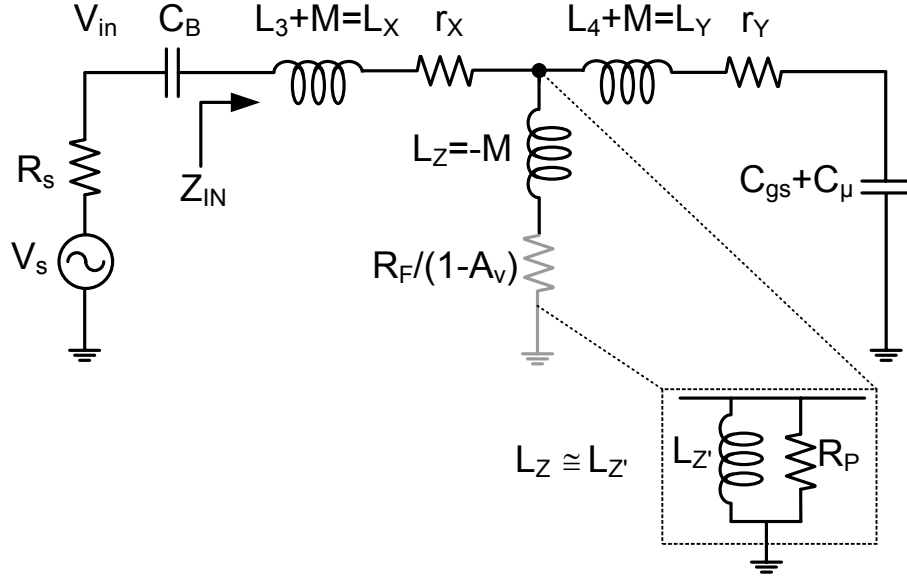
Figure 4.11: Input impedance equivalent network of the LNA.

between the input matching and the noise figure should be considered when the value of k-factor is selected. From (Eq. 4.15), it is seen that the parasitic $C_{gs} + C_\mu$ can be tuned out with proper selection of the components values.

4.2.3 Noise Analysis

There are many factors which may directly affect the NF of the proposed LNA design. The input impedance matching network, feedback resistor, biasing circuitry and drain current noise of the MOS device M_1, are the major contributors. In saturation, the drain current noise is mainly due to the drain current and weakly is dependant to drain voltage [31]. The output load resistance and the output buffer, which generally assumed to have insignificant noise contribution, also add to the NF. The parasitic components of the input CT inductor which reduce Q_T of the matching network and channel length effect of the transistor M_1 are inevitable issues, which need careful design strategies to overcome. Since the noise contribution of the cascode transistor M_2 is negligible, its noise effect is neglected [32].

The equivalent small signal noise model of the wideband LNA is shown in Fig. 4.12. Since the mutual coupling M between two halves of the inductors is noiseless, the effect
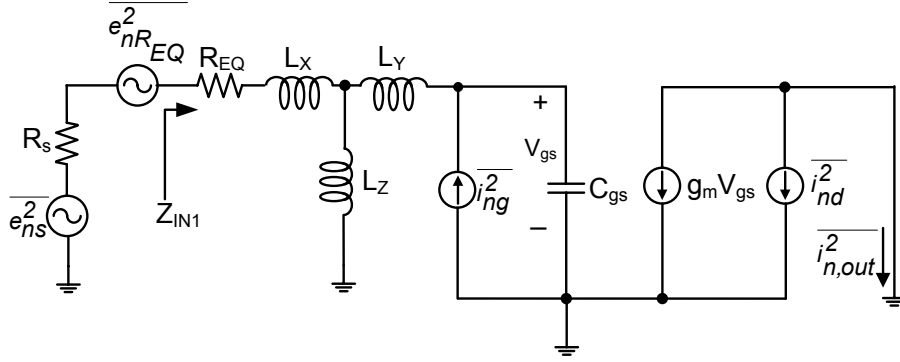
Figure 4.12: Simplified small-signal model of Fig. 4.5(a), noise contribution of M_2 is ignored.

of $L_Z = -M$ is neglected in the NF calculations. By solving the small-signal model for $Z_{IN1} = R_s$ at resonance and following the noise calculation method explained in [23], we get

$$F = \frac{R}{R_s}\left(1 + \frac{R}{R_s}\frac{\omega_0^2 R_s g_m \gamma}{\omega_{T_0}^2 \alpha}\chi\right). \qquad (\text{Eq. 4.16})$$

where,

$$\chi = \frac{\delta\alpha^2}{5\gamma}\left[1 + Q_T^2\right] + 1 - 2\left|c\right|\sqrt{\frac{\delta\alpha^2}{5\gamma}}. \qquad (\text{Eq. 4.17})$$

$$R = R_s + R_{EQ}, \ \ \alpha = \frac{g_m}{g_{d0}}, \ \ \omega_{T_0} = \frac{g_m}{C_{gs} + C_\mu}. \qquad (\text{Eq. 4.18})$$

$$R_{EQ} = R_g + r_X + r_Y + \frac{(L_X\omega_0)^2}{R_F/1 - A_v}. \qquad (\text{Eq. 4.19})$$

where $\delta \approx 1.33 - 4$, $\gamma \approx 0.67 - 1.33$ are excess noise parameters, $c \approx j0.4$ [32], and g_{d0} is the channel conductance at $V_{DS} = 0$. For the noise analysis, parasitic resistances of L_X, L_Y, and gate resistance of the transistor M_1 are lumped into R_{EQ}. In order to determine the NF contribution due to R_F, the open loop gain A_v is assumed to be consistent across the bandwidth. An increase in R_F reduces noise linearly. However,

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an increase in R_F pushes the input dominant pole in (Eq. 4.13) to a lower frequency. The NF can be lowered by choosing the right value of R_F which alters Q_T in (Eq. 4.17). Given in (Eq. 4.18), ω_{T0} increases as the transconductance increases and consequently improves the NF. Any extra physical input resistance r_g adds an additional term of r_g/R_s to (Eq. 4.16). Since only one CT inductor is employed at the input of the LNA, less loss is contributed to the NF.

4.2.4   Design Sensitivity to Process Variations

Due to the frequency and process dependency of the components, variations in the design specifications are expected. In this part susceptibility of the LNA to these variations and its effect on the performances is briefly evaluated. For instance, mismatch between the components in the input matching network, frequency dependency of the components, modeling inaccuracy and manufacturing variations as technology scales, are the important parameters which increases the design sensitivity. In this wideband LNA, the gain, NF, and linearity specifications are constrained to be met with minimum power consumption. A key parameter that degrades the NF of the amplifier is the noise resistance R_n which is investigated in [33]. Clearly, by reducing R_n the NF improves to some extent. In Fig. 4.13 variation of the measured R_n versus frequency is plotted. The bias current constraint is kept to less than 3.5 mA. Since the width (W) of the device is inversely proportional to R_n [33], proper selection of W results in an optimum value of R_n that reduces the variation of the noise figure (ΔNF). However, the device size cannot be made arbitrarily larger to make R_n smaller because the parasitic C_{gs} increases as W increases. As shown, the variation of normalized R_n in this design is less than 0.8 Ω over a wide range of frequency at three different DC currents. It is noted that the variations of R_n is almost constant over the wide range of frequency. As a conclusion, since the variations of R_n are the same for 3 different currents, we cannot improve the NF necessarily from this point of view in this design.
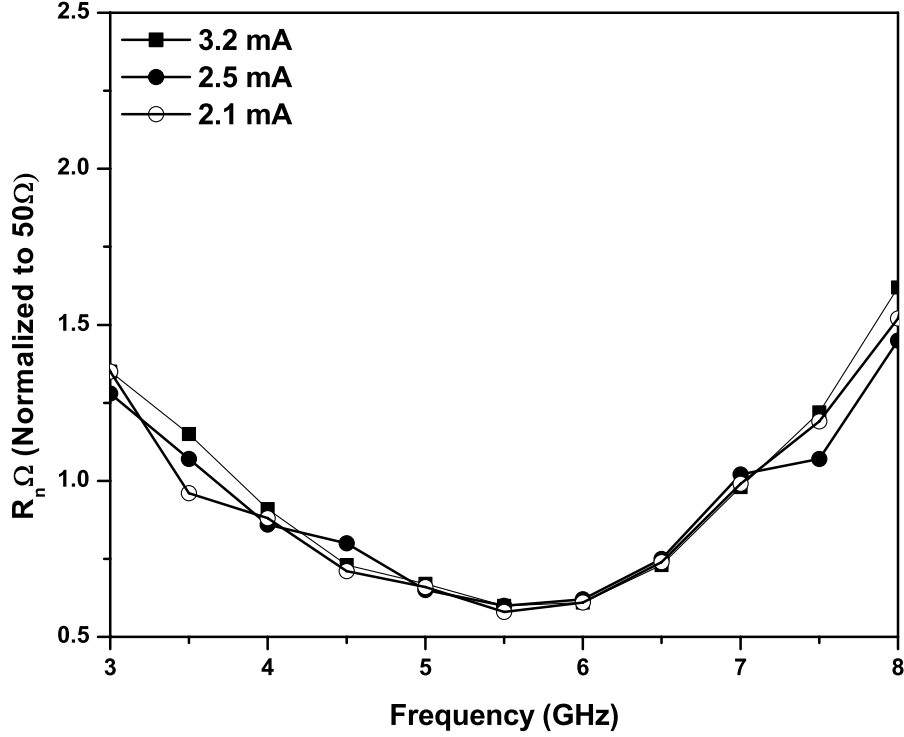
Figure 4.13: Variations of normalized R_n with three different currents vs. frequency.

The mismatch between the components degrade the gain and high frequency performances of the LNA. The focus in here is mainly on the sensitivity of the gain and noise figure to the parameters variations. Basically, with a higher voltage gain, a better NF performance can be resulted. On the other hand, this LNA is designed to be used with a mixer, and high gain LNA reduces the linearity of the whole design (LNA+Mixer). Therefore, LNA should meet the tradeoff between all the design characteristics. To gain more insights, we would calculate the voltage gain of the LNA. To derive the voltage gain of the amplifier, notice that R, L_L, which are in series with L_2, and the parasitic C_1 are neglected and $L_1 = L_2 = L$. The overall gain is

$$\frac{v_{out}}{v_s} = \frac{-g_m}{sC_{gs}\left(R_s + Z_{IN}\right)} \cdot \frac{\left(R_F \parallel sL\right)}{s^2 L_Z C_2 + sC_2\left(R_F \parallel sL\right) + 1}. \tag{Eq. 4.20}$$

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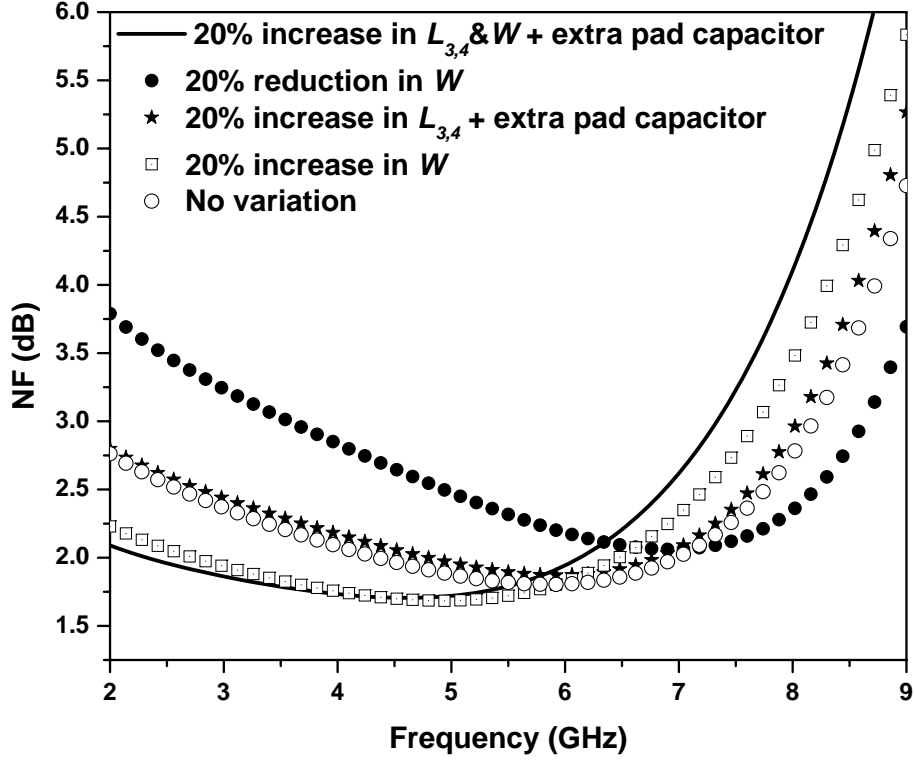
Figure 4.14: Device variations effect on the noise figure performance.

where $v_s = i_s R_s - v_{in}$ and assuming $i_{d1} \approx i_{d2}$, then the output current i_{d1} is equal to $v_s . g_m / s C_{gs} (R_s + Z_{IN})$. Equation (Eq. 4.20) shows that the gain rolls-off if C_{gs} is large. The impact of C_{gs} is reduced with higher f_T or reduction of the mismatch between the input matching components to guarantee that C_{gs} is resonated out over the frequency of interest. Moreover, the output capacitor C_2 causes reduction in the voltage gain. The reduction in the voltage gain would increase the NF. These parameters should be considered to keep the agreement between the gain and NF performances.

Fig. 4.14 is plotted to show the sensitivity of the NF to 20% devices variations at 3.2 mA current consumption. As shown in the solid line plot, the worst case in the NF degradation is when W of the transistor M_1 and $L_{3,4}$ are increased (20%) and an extra pad capacitor is added to the circuit. This plot shows that the NF has a better performance at the frequencies lower than 5.5 GHz compared to the case when no variation is applied.

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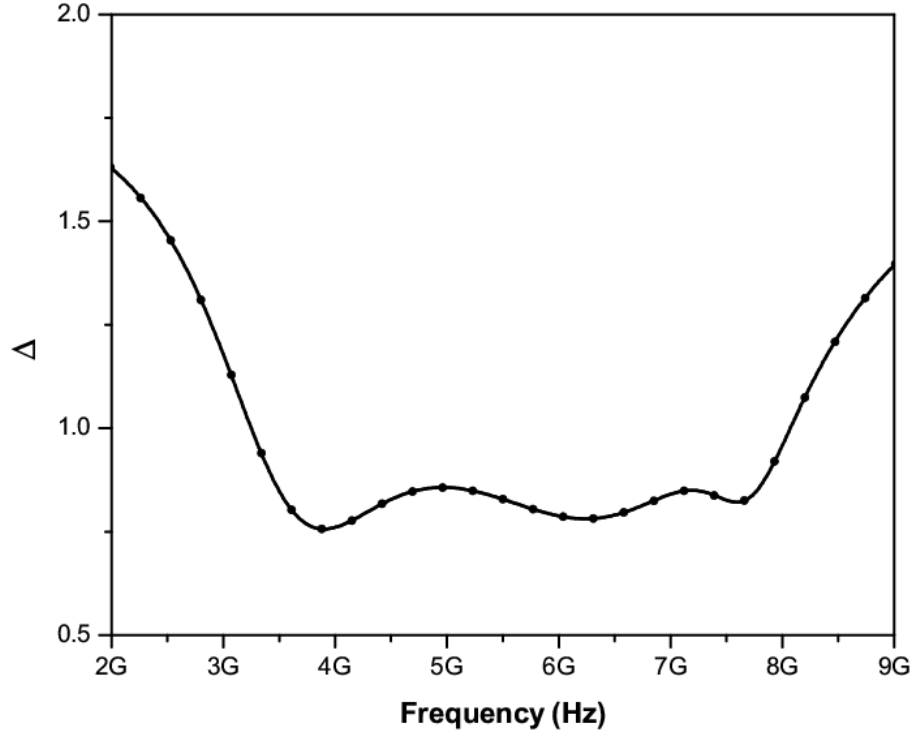
Figure 4.15: Simulation stability of the wideband LNA, Δ.

This difference is due to the higher current from the larger device size. It should be noted that the frequency at which the minimum sensitivity to process variations in NF is observed (about 5.75 GHz from Fig. 4.14), is very close to the frequency at which the minimum value of R_n occurs (5.5 GHz in Fig. 4.13). However, the NF degrades at frequencies higher than 5.8 GHz due to the reduction in the gain and Q-factor of the inductors. The deterioration of the noise figure at higher frequencies is partially due to the gate resistance noise and gate induced noise (both are $\propto f^2$) [32].

4.3   Experimental Results

In order to examine the stability condition of the LNA, the stability simulation is carried out as below in Fig. 4.15 and Fig. 4.16. As these simulations shows, both stability conditions $\Delta < 1$ and $K_f > 1$ are met.
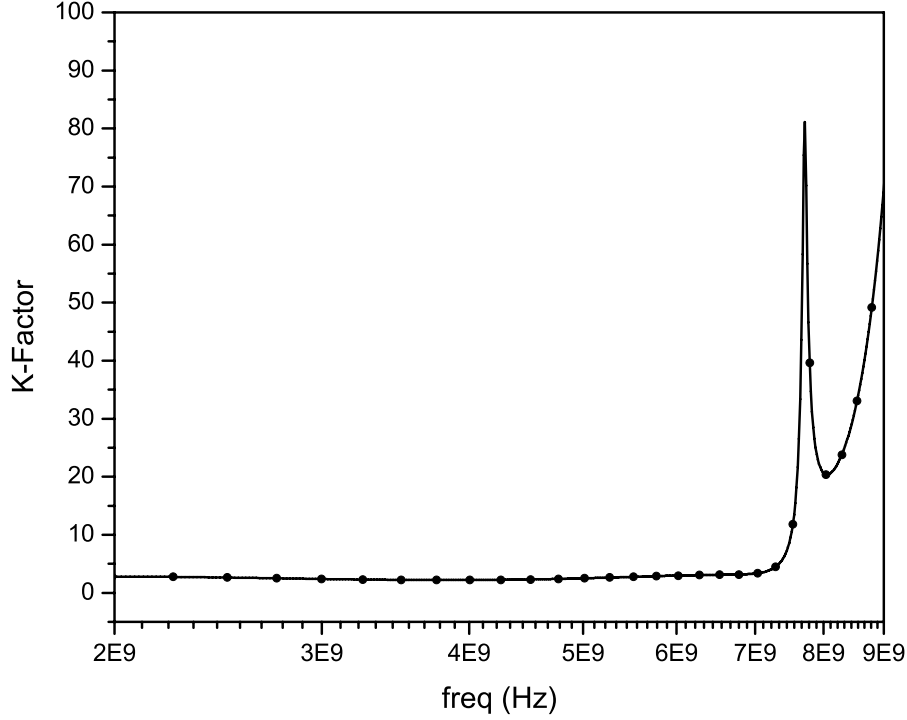
Figure 4.16: Simulation stability of the wideband LNA, K_f.

From the discussion above, a wideband LNA with the bandwidth of $3.168-7.920$ GHz is designed for the multiband OFDM standard. The components values are listed in Table 4.1. The size of M_1 is selected properly to get low current consumption. From simulation, this wideband LNA provides a maximum gain of 20 dB with maximum NF of 2.9 dB under 2.2 mA current consumption. Since the sum of series parasitic resistances of the output inductors $L_L + L_{1,2}$ is high enough, which is about 55 Ω at 7 GHz, R in Fig. 4.9 was removed from the final design. This enables the transistors to have enough voltage headroom with the optimum device size which efficiently reduces the current consumption of the LNA. In addition, it improves the gain and the NF without extra current consumption.

By the size of the transistor M_1, the parasitic C_{gs} can be found out. From the blocking capacitor C_B of 1 to 2 pF, the value of the input CT inductor is determined to get the desirable input matching. On the other hand, the size of M_2 determines the parasitic

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Table 4.1: Component values of the LNA

$(W/L)_{M_1}$	$(W/L)_{M_2}$	$L_{1,2}^*$	$L_{3,4}^*$	L_L	R_F
120/0.18	40/0.18	9 nH	2.92 nH	1.31 nH	1.14 $k\Omega$

* $L_{1,2}$ and $L_{3,4}$ are the center-tap inductor.
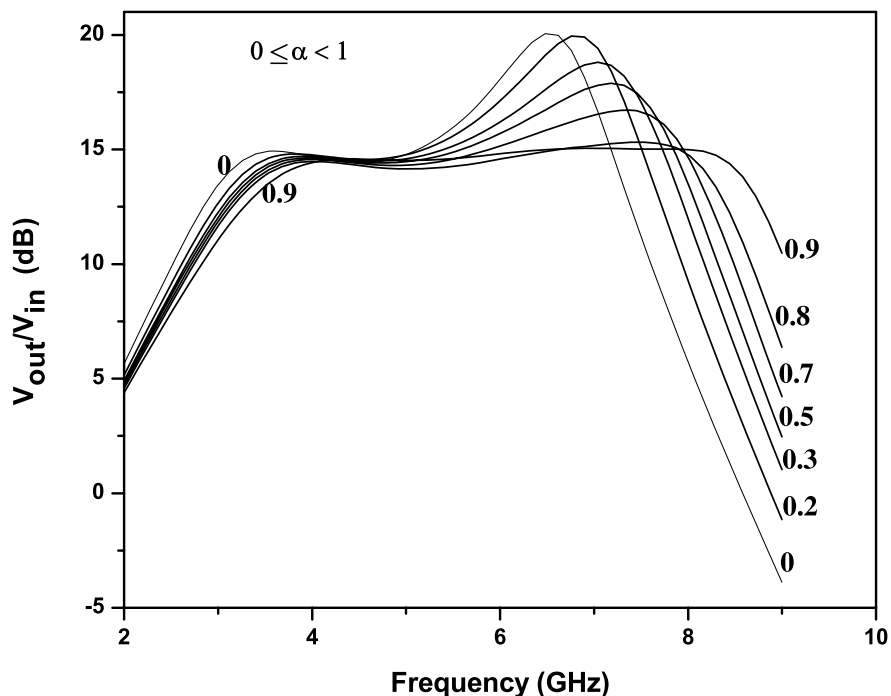
Figure 4.17: Contour plots of α variation (variation of the next stage parasitic capacitance) and its effect on the gain peaking vs. frequency.

capacitance C_1 at the output network. The output response of Fig. 4.9 is simulated in Fig. 4.17 to show the different loading (C_2) effects. As α increases, $C_1=(1-\alpha)C/2$ reduces and $C_2 = (1+\alpha)C/2$ increases. As shown in Fig. 4.17, with a reduction in C_1 and an increase in C_2, the output T-coil network exhibits larger bandwidth with smaller peaking especially when C_2 dominates (α =0.9). So the size of M_2 is selected to be much smaller than the size of M_1, to decrease the parasitic C_1 and to reduce the peaking in the response at high frequencies. Since this wideband LNA will be interfaced with a mixer in the UWB design, the input capacitance of the I/Q downconversion mixer should be taken into account as it determines the gain-flatness of the LNA. In this design, a current reuse
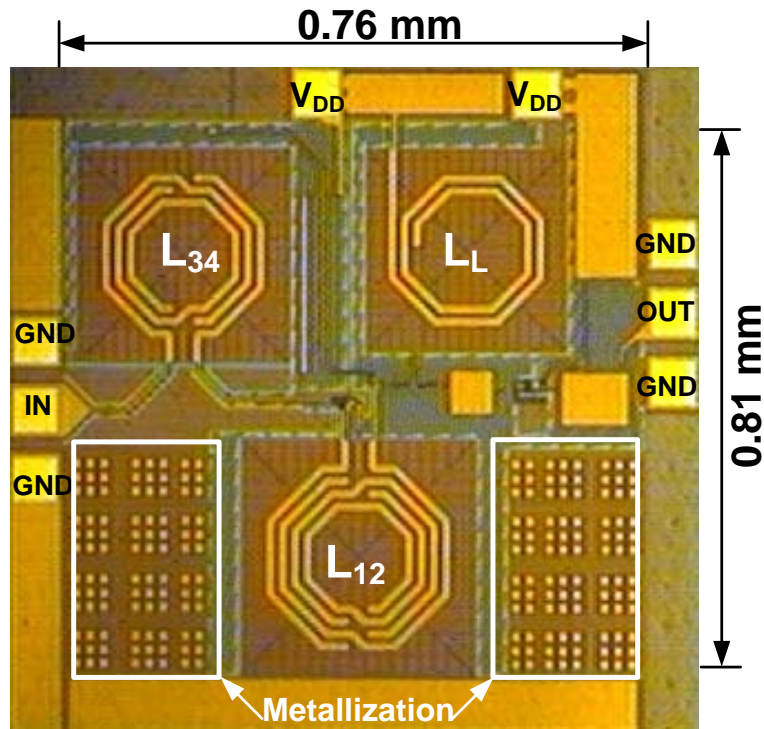
Figure 4.18: Die micrograph of the wideband LNA.

buffer is implemented to obtain 50 Ω output matching for the measurement purposes. The loading effect of the buffer is determined to be about the same as the mixer loading effect on the LNA stage. The prototype of the wideband LNA is fabricated in a six-metal 0.18 μm CMOS technology. The die micrograph is shown in Fig. 4.18. The total die area including the output buffer is 0.76×0.81 mm^2. The inductors are mounted on the pattern ground shield structure for better efficiency [34]. The empty spaces are covered with metal-filling to reduce the process variations effects. The transistors M_1 and M_2 are divided into six units to reduce the gate parasitic resistance. The simulated and measured results of the S-parameters are plotted in Fig. 4.19 and Fig. 4.20, respectively. The measured gain has a maximum peak of 16.4 dB from 3.19 to 3.8 GHz frequency. The gain-flatness of 2.1 dB from 4 to 7.6 GHz frequency is obtained with 2.16 mA current consumption. The gain rolls-off by 3.5 dB from 7.6 to 8 GHz frequency. This drift can be corrected by adjusting the inductors in the subsequent silicon iteration. The measured

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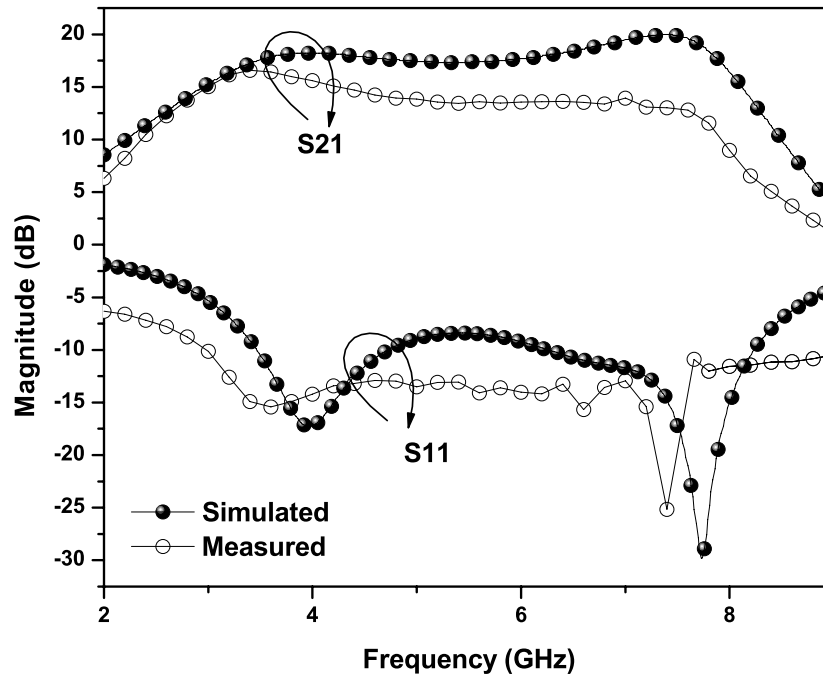
Figure 4.19: Gain and input reflection coefficient of the LNA vs. frequency.
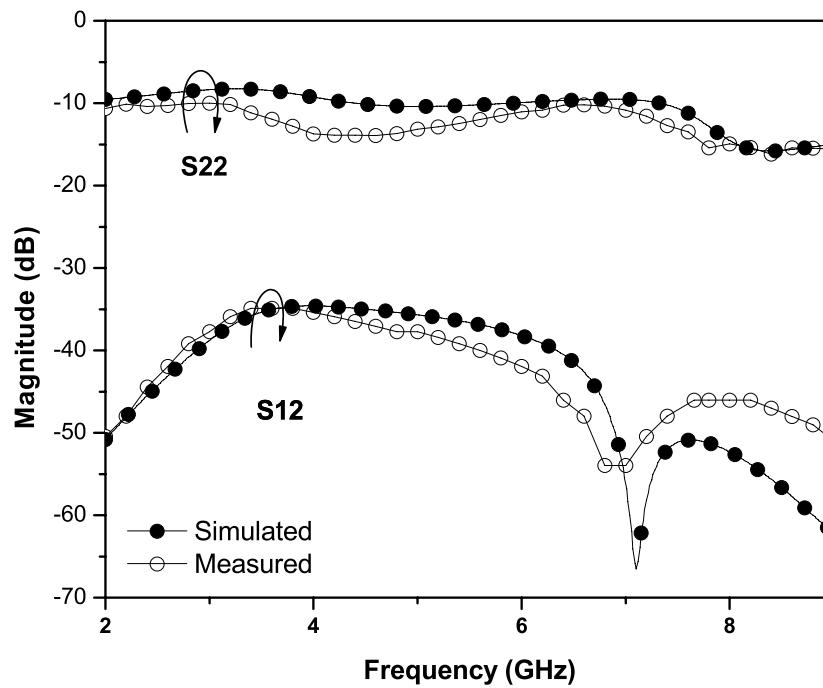
Figure 4.20: Measured and simulated S_{22} and S_{12} of the LNA vs. frequency.
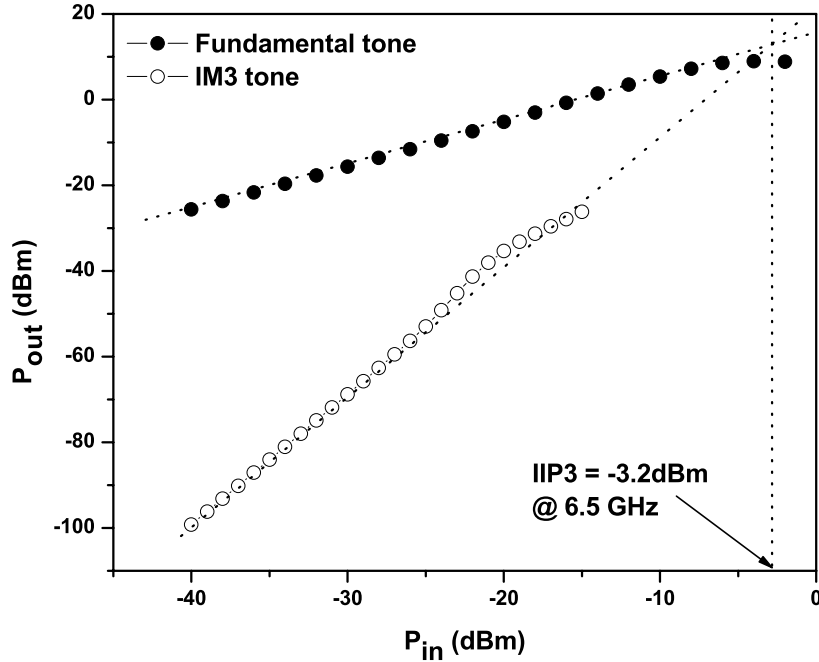
Figure 4.21: Simulated IIP3 at 6.5 GHz.

input reflection coefficient is well below -10 dB for the entire operating frequencies. As explained before, the output matching of the LNA is set by a current reuse buffer just for the test purposes. The comparison between the measured and simulated S_{22} and S_{12} is plotted in Fig. 4.20.

The third order input intercept point (IIP3) is simulated versus different frequencies. Fig. 4.21 plots an IIP3 of -3.2 dBm at 6.5 GHz frequency. Two-tone test is used to simulate the IIP3 with 1 MHz frequency space between the tones.

The simulated and measured NF over the bandwidth is shown in Fig. 4.22. Several dies were measured and mean value of the NF is plotted. The difference between the measured and simulated NF is owed to the process variations as explained before. A minimum NF of 2.7 dB is measured at 2.8 GHz and the NF at 3 GHz is 2.9 dB. The maximum NF is 4.66 dB at 7 GHz and it falls to 3.8 dB at 8 GHz frequency. Fig. 4.23 depicts the measured quality factors of the input and the output inductors. The Q-factor of the input inductor effects the NF directly. The measured Q-factors are $8 < Q_{L_L} < 11.8$,

Table 4.2: Wideband LNA performance summary and comparison

Reference	Technology	BW GHz	S11 dB	Gain$_{max}$ dB	NF dB	IIP3 dB	Power mW	Area mm^2	FOM
This Work	**0.18 μm CMOS**	**3−8**	**<-10**	**16.4**	**2.9−4.66**	**-2.2 to -4.3**	**3.9**	**0.62**	**4.4 to 8.9**
[4] STD	0.18 μm CMOS	2.3−9.2	<-9.9	9.3	4−8	-6.7[†]	9	1.1	0.3 to 1.5
[4] TW	0.18 μm CMOS	2.4−9.5	<-9.4	10.4	4.2−8	-8.8[†]	9	1.1	0.49 to 1.6
[21]	0.18 μm CMOS	3.1−10.6	<-11	9.7	4.5−5.1	-6.2	20	0.59	0.5 to 0.6
[2] LNA2	0.18 μm CMOS	1.3−12.3	<-9	8.2	4.6−5.5	7.6-9.1	4.5	1	2.69 to 3.64
[35]	0.18 μm SiGe	3−10	<-10	21	2.5−4.2	<-1[‡]	30	1.8	1.6 to 3.4
[36]	0.18 μm CMOS	0.4−10	<-10	12.4	4.4−6.5	-6	12	0.42	1 to 1.99
[37]	0.18 μm CMOS	2.8−7.2	−	19.1	<3.8	-1[§]	32	1.63	0.88
[38]	0.13 μm CMOS	1.5−8.1	<-9	11.7	3.6−6	11.7 to 14.1	2.62 @1.3V	0.58	3.25 to 7.5
[39]	0.18 μm SiGe/CMOS	0.1−11	<-12	8	2.9	-3.55	21.6	0.76	1.3
[40]	65 nm CMOS	0.2−5.2	−	15.6	<3.5	>0	14 @1.2V	0.009	1.7
[41]	0.18 μm CMOS	0.048−1.2	-9	14[×]	3[◊]	3[◊]	15.8 @2.2V	0.37	1.84
[42]	0.13 μm CMOS	0.8−2.1	-8.5	14.5	2.6	+16	17.4 @1.5V	0.0992	0.48
[43]	0.13 μm CMOS	3.1−10.6	<-9.9	16.5	2.07−2.93	-5.1 − -8.5[◦]	9 @1.2V	0.87	5.78 to 9.1

* at 3−8 GHz. † at 6 GHz. ‡ at 5.4 GHz, 5.6 GHz. $^◦$ at 4−8 GHz. § at 6 GHz. $^×$ power gain. $^◊$ at maximum gain.

8.8< $Q_{L_{1,2}}$ <10.7, and 11.5< $Q_{L_{3,4}}$ <13.9 for 3−8 GHz frequency. A high Q inductor

at the input is chosen for better NF, and lower Q inductors at the output were used

for the gain-bandwidth tradeoff. Table 4.2 indicates the performance comparisons of

the proposed wideband LNA with prior works. A figure-of-merit (FOM) is used here to
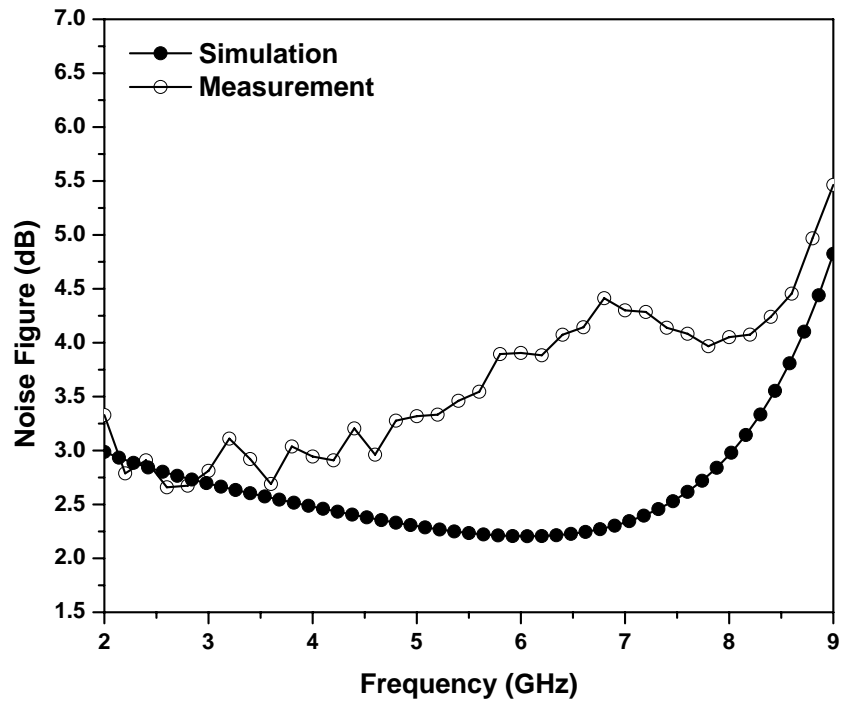
Figure 4.22: Simulated and measured noise figure of the wideband LNA.
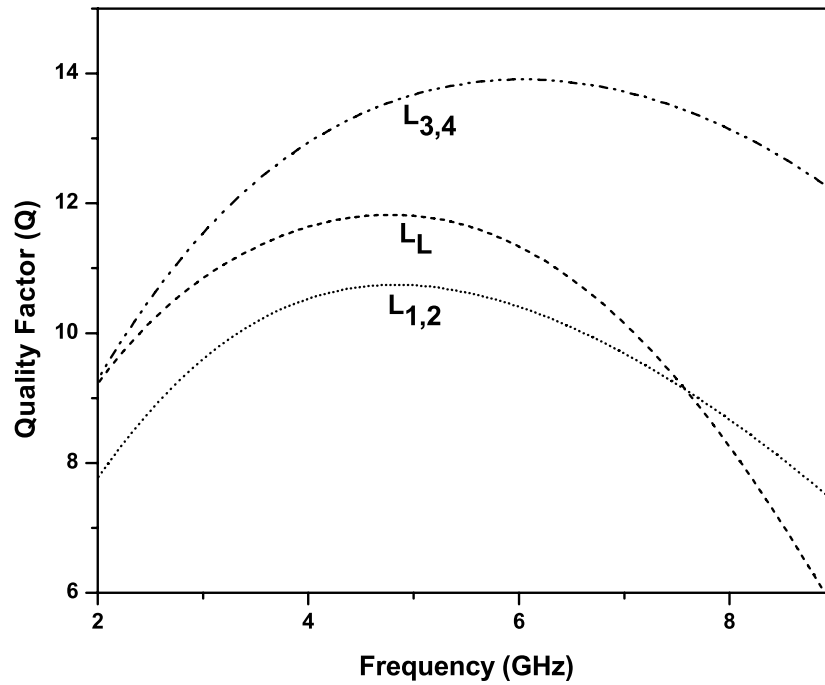
Figure 4.23: Measured quality factor of the inductors.

compare the performance of different LNAs with similar functionality. The *FOM* in here evaluates the gain, -3 dB bandwidth, excess noise factor and power consumption of the LNA which is defined as

$$FOM = \frac{|S_{21}|\, BW_{GHz}}{(F-1)\, P_{mW}}.$$ (Eq. 4.21)

Based on the *FOM* calculated in Table. 4.2, the proposed wideband LNA shows comparable performances to the other designs.

As a summary, a technique to attain the wide bandwidth LNA is presented using 0.18 μm CMOS technology. The introduced technique tunes-out the parasitic capacitances of the transistors over a wide bandwidth. The relations of the components to the standard form of the Butterworth filter are calculated to get the desired gain-flatness. The number of inductors are minimized to reduce the loss associated with them. Using this technique, a single stage wideband LNA is obtained with a low power consumption.

Chapter 5

Introduction to Mixer Architecture

Mixers can be implemented using any nonlinear device such as diode, FET and bipolar transistors. Mixer design can be classified in two passive and active structure. In the passive architecture, we wish to minimize the conversion loss, because low conversion loss generally guarantees low-noise operation. In microwave FET mixers, high gain is relatively easy to obtain, but it does not automatically insure that other aspects of performance will be good. Indeed, high mixer gain is often undesirable in receivers because it tends to increase the distortion of the entire receiver. Therefore, in most receiver applications, an active mixer is designed not to achieve the maximum possible gain, but to achieve a low noise figure and modest gain.

5.1 Active Mixer

The CMOS active mixer (frequency multipliers) has many advantages over the passive type mixers. The active mixers can have broad bandwidth and provides conversion gain. The most well-known active mixer architecture is current commutating mixer shown in Fig. 5.1. This topology was introduced for the first time by Barrie Gilbert [44] in bipolar technology. Although other types of mixers have been proposed, most FET mixers structure have the LO and RF applied to the gate and source and IF is filtered from the drain. The time-varying transconductance is the dominant contributor to frequency
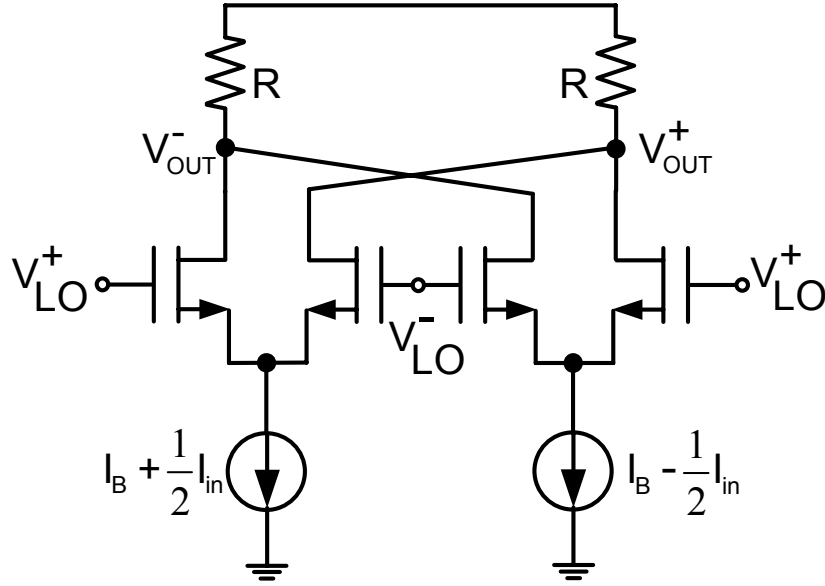
Figure 5.1: Current commutating active mixer.

conversion. In such mixers the effect of gate-to-drain capacitance, gate-to-source capacitance and drain-to-source resistance are often harmful and must be minimized. Since the time-varying transconductance is the primary contributor to mixing, it is important to maximize the range of the FET's transconductance variation. To maximize the transconductance variation, the FET must be biased close to its threshold voltage, V_t, and must remain in its saturation region throughout the LO period. Full saturation can be achieved by ensuring that the drain voltage $V_d(t)$ under LO pumping remains at its dc value, V_{dd}. This condition is achieved by short circuiting the drain at the fundamental LO frequency and all LO harmonics. If the drain is effectively shorted, the LO current, which may have a fairly high peak value, can not cause any drain-to-source voltage variation. In this case the LO voltage across the gate-to-drain capacitance is minimal, so feedback is minimal and mixer is stable.

If the drain is not effectively shorted, the drain voltage varies with LO excitation. Then, the voltage is likely to drop, at the current peaks. If the voltage dips enough that the FET drops into its linear region, the peak transconductance also decreases, so the

(a) Unbalanced mixer   (b) Double-balanced mixer
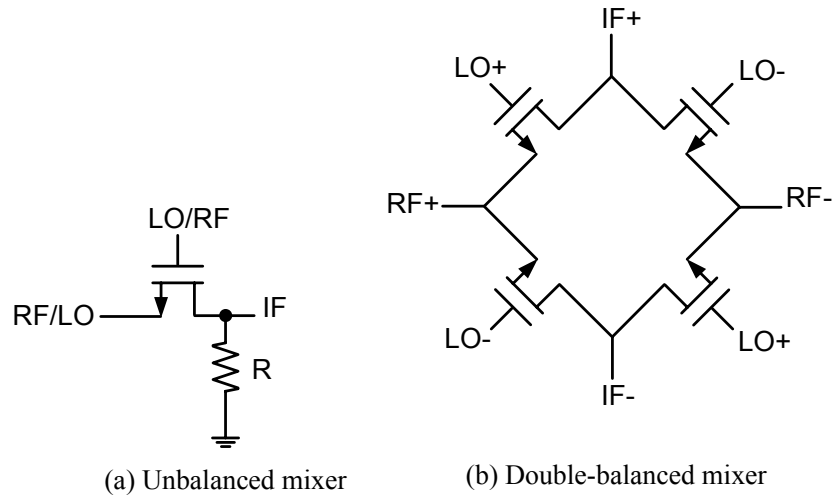
Figure 5.2: Passive mixer structures.

fundamental-frequency component of the transconductance is not maximized. Similarly, the peak drain-to-source conductance increases, increasing the average output conductance, creating an additional loss mechanism. It is always best to bias the FET at the same drain voltage it would require when used in an amplifier. A well-designed mixer is usually insensitive to small changes in dc drain voltage, but may be moderately sensitive to dc gate voltage.

5.2 Passive Mixer

The main advantage of the passive mixer is that it does not dissipate static power. More importantly, passive mixers have very low distortion, low $1/f$ noise, and no shot noise. Since the high frequency noise is entirely thermal, the noise figure depends on the conversion loss. In Fig. 5.2 two examples of the FET passive mixers are shown. Since there is no current flowing thorough the switches, passive mixer tends to present a good linearity. Although, the switch resistance is non-linear but still their linearity performance is better than an active mixer. Passive mixers are divided into voltage-mode passive mixer [5], [45], Fig. 5.3, and current-mode passive mixer, Fig. 5.4. In the
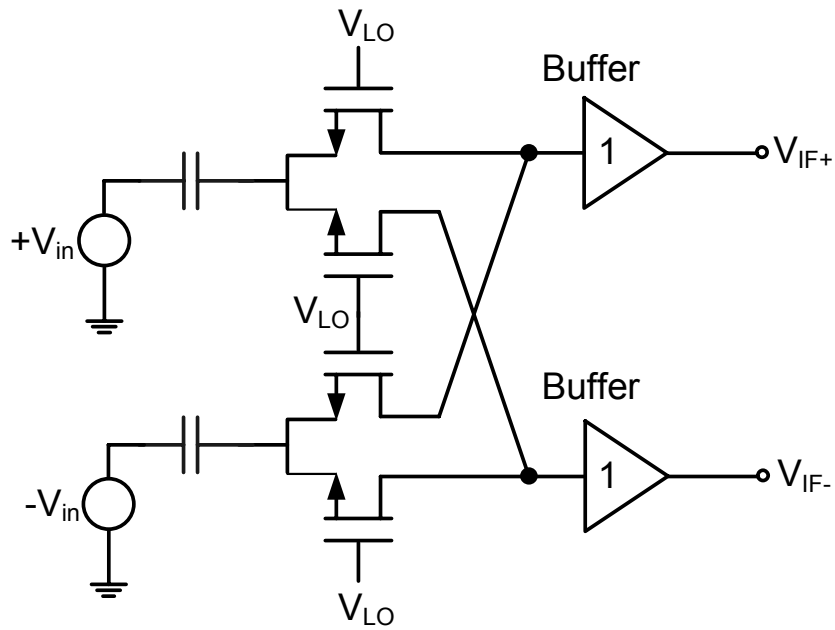
Figure 5.3: Double balanced voltage-mode passive mixer [5].
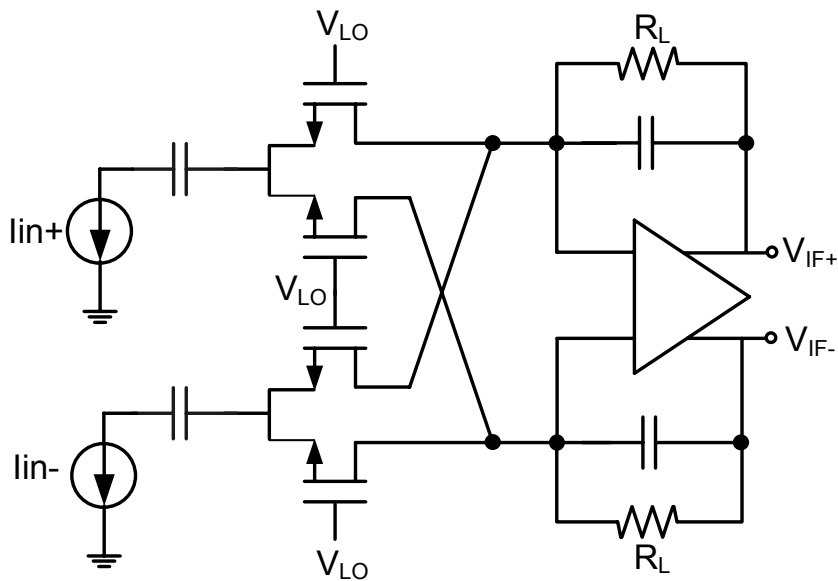
Figure 5.4: Double balanced current-mode passive mixer.

voltage-mode passive mixer, voltage is commutated using voltage switch. In the voltage-mode passive mixer there is a substantial voltage swing across the switches, whereas the current-driven passive mixer loaded with a transimpedance stage, have negligible signal

swing across the switches, with further results in better linearity [46], [47]. In voltage-commutating passive mixer a buffer is needed before the switching transistors to derive the switch resistance and also the input resistance of the stage following the mixer core. In contrast to the active mixer, in the current- and voltage-mode passive mixer, all the MOSFET switches are always in triode region. For this reason, this architecture is called passive.

In Fig. 5.3, the RF transconductor transforms the RF output voltage of the LNA to a current. The conversion gain of this architecture assuming ideal LO square wave switching, is expressed as

$$CG = \frac{2}{\pi} g_m R_L \qquad \text{(Eq. 5.1)}$$

where g_m is the transconductance of RF stage in current-driver stage, R_L is the feedback resistor of the transimpedance amplifier. In practice, the real gain will be smaller due to the parasitic components at the common source of the switches of the mixer and the output of the transconductance stage that shunts a part of the RF signal to ground. Therefore, it is important to care the device sizing, layout of the switching stage, and device matching in the transconductance stage.

From linearity point of view, the IIP3 of the active mixer at high frequency can be improved by increasing the DC bias current [48]. However, the passive mixer does not consume any significant static power. Although the switches are non-linear, yet passive mixer poses better linearity compared to the active mixer. The current-mode passive mixer has lower signal swing across the switches compared to the voltage-mode passive mixer, which increases the linearity performance of the current-mode passive mixer. The reason can be sought in difference between loading stage in these two architectures.

Low frequency noise of the switches in the mixer design is a critical issue in many front-end receiver architectures, which can corrupt the output performance of the whole system.

The flicker noise of the passive current-mode mixer is dominant by the transimpedance amplifier (TIA) stage. Any mismatch between devices in TIA adds to the total flicker noise of the mixer. Furthermore, the input parasitic capacitance of the mixer stage plays an important role in the noise contribution. A method to reduce the parasitic capacitance of the switches, is to reduce the device width. However, the ON-resistance of the device increases. If device width reduces, the value of the ON-resistance becomes comparable to the output impedance of the driving stage, which reduces the gain and increases the noise contribution. On the other hand, this parasitic capacitance is much smaller in an active mixer, if the switches remain in the saturation region during the whole LO period.

5.3 Non-idealities of the Mixer

5.3.1 Intermodulation Distortion

In short-channel CMOS transistors, the main source of distortion comes from the nonlinear behavior of the transconductance. Assuming the output transconductance is linear and the cross modulation between the transconductances is negligible. Then the ac current in a MOS transistor can be modeled as

$$i_{ds}\left(v_{gs}, v_{ds}\right) = g_m v_{gs} + g_d v_{ds} + g_{m2} v_{gs}^2 + g_{m3} v_{gs}^3 + ... \qquad \text{(Eq. 5.2)}$$

where g_d is output-conductance nonlinearity. The second-order transconductance g_{m2} equals to 0 A/V at $v_{gs} = 0$ and then increases before reaching a maximum value at a small overdrive voltage $(V_{gs} - V_t)$. Further increase in V_{gs} results in decreasing g_{m2}. As a result, g_{m3}, which is obtained by differentiating g_{m2} with respect to V_{gs}, decreases to zero at a very small overdrive voltage, i.e., when the transistor is operating in the moderate inversion region. Therefore, if the transistor is biased at this operating point, which is known as "sweep spot" [49], third-order harmonic distortion would tend to zero, which would result in infinite third-order output intercept point (OIP3), shown in Fig. 5.5.
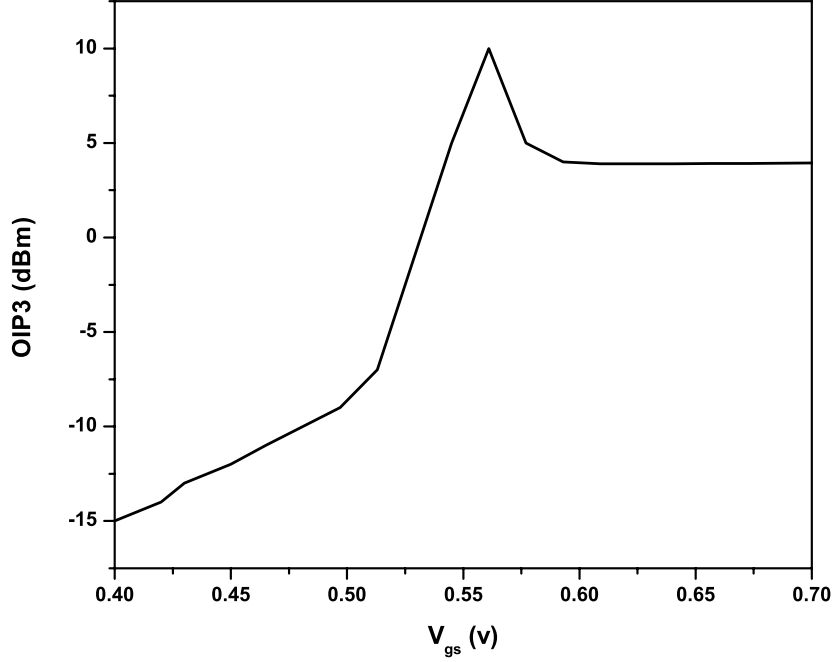
Figure 5.5: IIP3 versus V_{gs} for a single transistor.

Referring to the Fig. 5.2(a), when switching transistor is "on" it may be modeled as shown in Fig. 5.6. The transistor operates in the triode region and is replaced by a nonlinear resistor R_{on}. This is the primary source of intermodulation distortion. Note that arrow on the resistor symbol for R_{on} indicates the nonlinearity, not the time varying resistor. The capacitors C_{gs} and C_{gd} are not included, as their impact on distortion is small. The gate overlap capacitors are combined together and represented as C_g. In the low-frequency the distortion is mainly determined by the R_{on} of the transistor and distortion due to the parasitic capacitors C_{sb} and C_{db} is quite small. If we assume that LO is not switching, the mixer in Fig. 5.2(a) is represented as nonlinear time invariant (NLTI) system. Therefore, to derive distortion associated with R_{on}, we can use the equation for an MOS transistor biased in the triode region as

$$I_d = k \left(V_{gs} - V_t\right) V_{ds} - \frac{k}{2} V_{ds}^2 \qquad \text{(Eq. 5.3)}$$

where $k = \mu C_{ox} \left(W/L_{eff}\right)$, and V_t is the threshold voltage. From (Eq. 5.3), we can see

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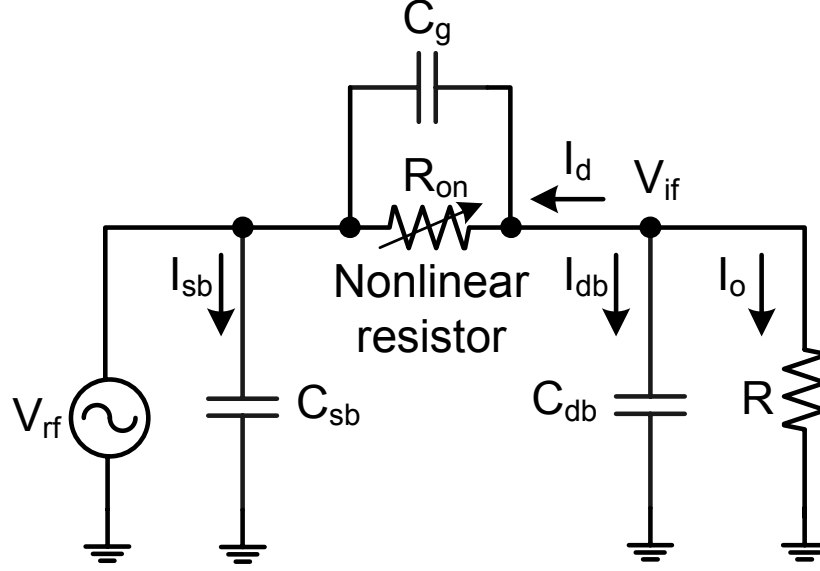
Figure 5.6: Distortion model for the unbalanced switching mixer in Fig. 5.2(a).

that I_d depends on V_{ds}^2, and this gives rise to distortion. Applying the Taylor series expansion, the third-order distortion is found as [50]

$$IM_3 = \frac{3}{8}\frac{1}{k(V_{GS} - V_t)^3 R}A_{if}^2 \qquad \text{(Eq. 5.4)}$$

This expression predicts distortion in the switch for inputs with small signal levels and low frequency. Since the large signal is presented, (Eq. 5.4) does not predict the distortion in mixing operation, however, it illustrate design strategies for low distortion whether or not there is a large signal presented. The most important point from (Eq. 5.4), is to apply large enough gate bias (or large LO drive for mixing operation). Because IM_3 reduces with cube of the gate to source bias voltage. Another important design strategy is to use large W/L ratios. The distortion at low frequency would improve, however, at high frequency the junction capacitors dominate the distortion.

For high frequency, to simplify the calculations, lets assume that the nonlinear capacitor C_{db} at the drain in Fig. 5.6 is replaced with a linear capacitor C, whose value is
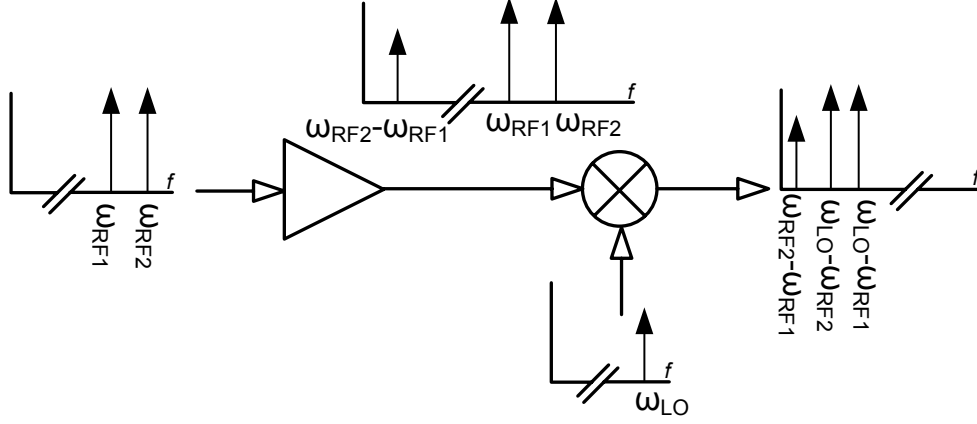
Figure 5.7: Nonlinearity in the RF.

taken to be the value of C_{db} when $V_{db} = 0$, and also assume that

$$IM_3 = \frac{3}{8} \frac{1}{k(V_{GS} - V_t)^3 R} A_{rf}^2$$

$$R \gg R_{on}$$

$$\frac{1}{j\omega_{rf}C} \gg R_{on} \quad \text{or} \quad \frac{1}{2\pi R_{on}C} \gg f_{rf}$$

(Eq. 5.5)

Applying these assumptions to the model in Fig. 5.6, an expression for IM_3 at high frequency due to interferers can be found as [50]

$$IM3 = IM_3 \left|_{low-frequency} \sqrt{1 + \left(\frac{RC\omega_{rf}}{3}\right)^2}\right.$$

(Eq. 5.6)

Now, we consider the case when V_{lo} is switching. In the low frequency case when V_{lo} is an ideal square wave, which means it has zero rise and fall time, the input voltage is multiplied by the Fourier representation of the LO square wave.

5.3.2 Second-Order Intermodulation Distortion

When two tones at ω_{RF1} and ω_{RF2} are presented at the RF input of the mixer, Fig. 5.7, the sum and difference of these two frequencies can be generated as a result of offsets in
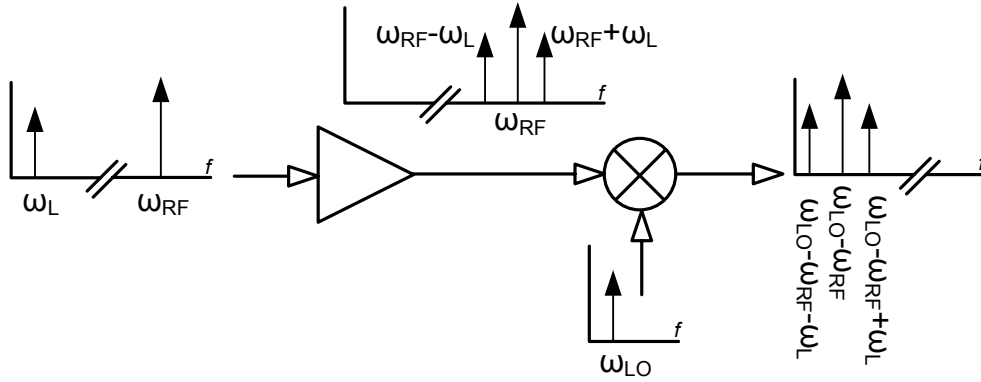
Figure 5.8: RF and low-frequency intermodulation.

the RF input stage. Therefore, in the presence of offset in transistors, the offset frequency $\omega_{RF1} - \omega_{RF2}$ can leak through following stage and fall in the output band.

A mechanisms which causes the second-order intermodulation (IM_2) distortion is known as RF-LO and LO-RF coupling which is due to the parasitic coupling of the RF/LO frequency into LO/RF port [6], [51]. Lets first consider only offset from RF input. A low-frequency signal at frequency ω_L at the RF input will mix with the RF signal at frequency ω_{RF} in the presence of second-order distortion and will create second RF tones at $\omega_{RF} - \omega_L$ and $\omega_{RF} + \omega_L$. Both RF tones will mix with the local oscillator signal, generating the desired signal at $\omega_{LO} - \omega_{RF}$ and the interferences at $\omega_{LO} - \omega_{RF} \pm \omega_L$, as shown in Fig. 5.8. As a result, the unwanted signal will mix down to the baseband and corrupts the baseband signal.

Leakage from LO port to the RF input creates intermodulation as shown in Fig. 5.9. The leaked LO signal on the RF port, is mixed with the LO signal, causing both the IF signal and a dc component appearing at the output. This will degrade the performance of the zero-IF receiver.

The other mechanism is due to the second-order nonlinearities in the active devices of the transconductor [52]. The low frequency intermodulation current at the output of the transconductor leaks to the output of the mixer without frequency conversion due to the
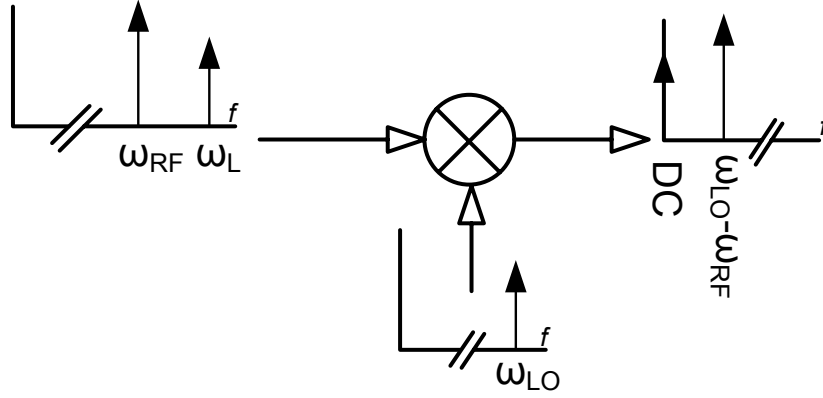
Figure 5.9: LO oscillator self-mixing. LO leakage to the RF port.

a duty-cycle distortion of the LO. This effect can be alleviated using a double-balanced topology if we assume that the devices in double-balanced structure are matched. Furthermore, the leakage due to the mismatch between the devices in the current switching stage is not easy to cancel. Furthermore, the second-order intermodulation products are generated due to the nonlinearity of the switching stage. The mismatch between two active devices contribute to the nonlinearity at low frequency. At high frequency on the other hand, the parasitic capacitance at common source of the RF input differential pair, increases the second-order intermodulation product. The parasitic capacitance introduces a limit to get a high second-order input intercept point (IIP2).

Considering a single balanced mixer in Fig. 5.10, and assuming a square-wave voltage applied at the switching pair, then the differential output current is equal to $(I + g_m V_{in})$ for one half period and $-(I + g_m V_{in})$ for the other half period. If the LO pulse has an exact 50% duty-cycle and assuming no mismatch between M_1 and M_2, there would be no second-order term generated at the mixer output. Otherwise, if we consider the non-ideal case, the second-order intermodulation current at the output, neglecting the
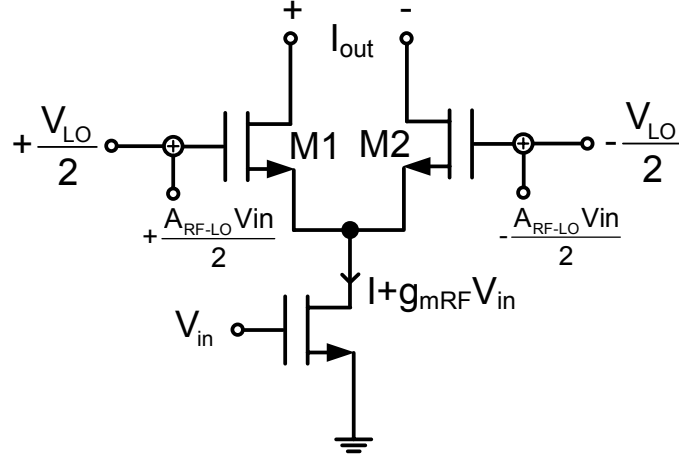
Figure 5.10: Self-mixing model in Single balanced mixer [6].

high frequency components, is obtained by [6]

$$I_{IM2,out} = \frac{g_{mRF}A_{RF-LO}}{V_L}V_{bk}^2 \times sw(t)$$

$$V_{bk} = A\left(\cos\omega_1 t + \cos\omega_2 t\right)$$

$$I_{IM2,out} = \frac{2g_{mRF}A_{RF-LO}}{\pi V_{pk}}A^2$$

$$\times \left[1 + \cos(\omega_1 - \omega_2)t + \frac{1}{2}\cos 2(\omega_{LO} - \omega_1)t\right.$$

$$\left. + \frac{1}{2}\cos 2(\omega_{LO} - \omega_2)t + \cos(2\omega_{LO} - \omega_1 - \omega_2)t + \cdots\right] \qquad \text{(Eq. 5.7)}$$

where $sw(t)$ is a square-wave function representing the LO waveform and V_{bk} is the blocker signal represented by a double sideband suppressed carrier (DSB-SC). The square-wave function toggles between 0 and 1 with a duty cycle equal to $2T_{sw}/T_{LO} = 2V_L/(\pi V_{pk})$. From equation above, it is clear that the second term causes the intermodulation distortion, and the other spectral components can be easily filtered out. This equality shows that if there is a blocker at high frequency between LO frequency and received signal, both the received and intermodulation product would be available at IF.

From second-order input intercept point definition, the relation of the IIP2 to the LO

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amplitude and port-to-port coupling can be found as [6]

$$IIP2\,(dBm) = 20\log\left(\frac{2}{A_{RF-LO}}\right) + V_{pk}\,(dBm)\,. \qquad \text{(Eq. 5.8)}$$

In order to increase the IIP2, the RF-to-LO coupling should be reduced and LO amplitude has to be increased. The coupling of the RF signal to the LO port of the mixer can create IM_2 through modulating the resistance of the switches. In the direct conversion architecture, since the local oscillator is at the same frequency as the RF carrier, the potential exists for LO leakage to either mixer input or the antenna where radiation may occur. The unintentionally transmitted LO signal may reflect back from an object nearby and be "re-received" consequently causing the self-mixing problem.

The IM_2 of the input transconductance stage in the presence of the switch mismatch, can be harmful as well. The IM_2 created by transconductance stage can be up-converted around LO frequency in presence of mismatch by the RF stage and then down-convert to the baseband by the switching stage. Therefore, if a low-frequency signal is presented at the RF input, any available offset in the switching stage will allow this low-frequency signal to fed through to the mixer output.

Similar to Eq. 5.2, considering the transfer characteristics of a nonlinear amplification circuit expressed by Taylor series expansion as [53]

$$v_{out}\,(t) = \alpha_1 v_{in}\,(t) + \alpha_2 v_{in}^2\,(t) + \alpha_3 v_{in}^3\,(t) + \cdots\,. \qquad \text{(Eq. 5.9)}$$

where α_1 is the small-signal voltage gain and α_2 and α_3 are the second- and third-order distortion coefficients, respectively. For distortion analysis, assuming the interfere signal at RF input as

$$v_{in}\,(t) = A_m m\,(t) \cos\left[(\omega_c - \omega_0)\,t + \varphi_m\,(t)\right] \qquad \text{(Eq. 5.10)}$$

where A_m is the peak signal amplitude, $m(t)$ is the modulating signal, ω_c is the carrier frequency, ω_0 is the phase offset from carrier frequency, and φ_m is the time-varying

phase signal. Now lets assume that our front-end design consists of a LNA followed by a quadrature mixer. In addition of the LNA gain, both LNA and mixer have non-zero second- and third-order distortion coefficients. Representing the gains, second- and third-order distortion coefficients of the LNA and mixer by G_{LNA}, G_{MIX}, α_{2LNA}, α_{3LNA}, α_{2MIX}, and α_{3MIX}, respectively.

Applying the signal in (Eq. 5.10) to the input of the LNA and find the output of the mixer by

$$v_{out-Mix}(t) = G_{LNA}G_{MIX}A_m m(t) \cos\left[\omega 0 + \varphi_m(t)\right]$$
$$+\frac{1}{2}\alpha_{2MIX}G_{LNA}^2 A_m^2 m^2(t)\left[1 + \cos\left(2\omega_0 t + 2\varphi_m(t)\right)\right]. \qquad \text{(Eq. 5.11)}$$

If ω_0 is much larger than channel bandwidth, the second term $0.5\alpha_{2MIX}G_{LNA}^2 A_m^2 m^2(t)$ generates in-band distortion. The first term and third term would be filtered-out by the low-pass filter following the mixer. In above, the second-order distortion nonlinearity was calculated in the absence of distortion.

5.4   Noise in the Mixer

Mixer noise, particularly flicker $(1/f)$ noise in CMOS mixers, can be troublesome when receiving narrowband wireless channels such as Global system for Mobile (GSM) communications. In [54], an extensive studies on the output noise of the active mixer, Fig. 5.11, due to the flicker noise of the FET is done. The flicker noise of the FET is directly proportional to the dc current which is commutated by the switching pair. Therefore, reducing the current flowing through the switching stage would reduce the flicker noise. This method can be implemented by injecting a part of the transconductance stage current into tail of the differential pair [54], Fig. 5.11. However, this method poses some drawbacks such as increase in white-noise level due to the additional current source plus

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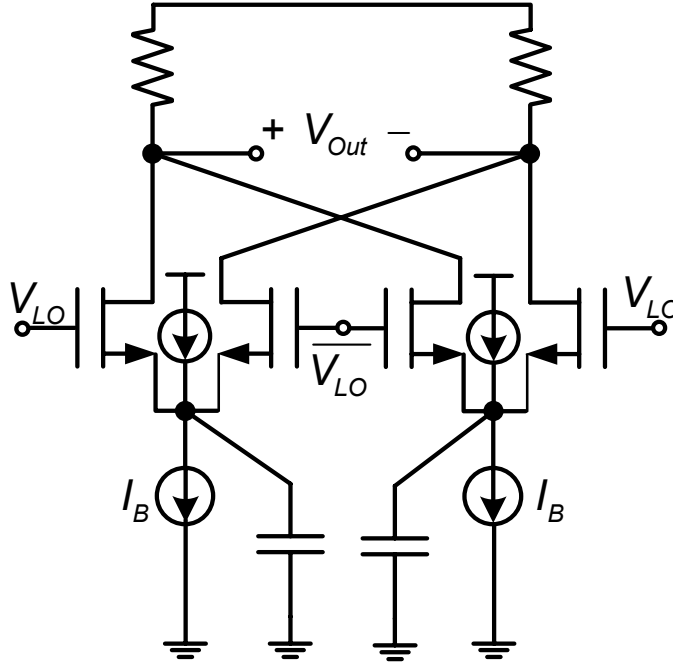
Figure 5.11: Noise reduction technique in an active mixer.

linearity degradation. Another issue rise from reduction of transconductance of the active differential FET switches, which their current is reduced.

On the other hand, a mixer without current commutating results in very low flicker noise at the output. Indeed, this mixer would only commutate the ac current. Since the mixer switches carry no current, they operate in the triode region and have to be driven with strong LO voltage. When, LO is high, the triode the triode FET switch directly connects the input transconductor to the output load through its ON resistance. Therefore, in order to minimize the effect of the stage following the mixer, a current buffer is used after mixer to isolate it from other stages, shown in Fig. 5.3. If voltage is desired at the output, a transresistance buffer should be designed.

In order to determine the noise of the passive mixer we have to take the output current buffer of the mixer into account. Consider a noise voltage at the frequency ω_m in the input node of the current output buffer, Fig 5.3. Due to the commutation of the switches, this noise voltage is up-converted to the RF side of the mixer and initiates RF

current at $\omega_{LO} \pm \omega_m$. These RF currents are then down-converted and become baseband noise current at ω_m. The baseband noise currents are superimposed onto the desired signal currents, pass into the current buffers, and appears at their output.

In an active mixer, however, the flicker noise of the FET switches appears at two different mechanism [54]; direct mechanism, which is due to the commutated currents, and indirect mechanism, which is because of the parasitic capacitance at the tail of the differential pair, shown in Fig. 5.11. In the direct mechanism, the flicker noise is represented as time-varying offset voltage of the gate associated with differential pair, having a constant rms value and a spectral density proportional to $1/f$. The offset voltage slowly modulates the commutation instant, which is located at the zero crossing of the LO waveform. This results in a train of noise pulses which add to the ideal square-wave commutation waveform, and then flicker noise appears at the output. The analysis and expressions in [54] is used for a mixer with narrowband frequency. Means that if there is an input RF signal at f_{in}, the flicker noise appears at DC and $2kf_{LO} \pm f_{in}$. So, in a direct conversion architecture where $f_{in} = f_{LO}$, if there a flicker noise at low frequency at current source of the transconductance stage, it would be up-converted to the LO frequency. However, if there is a blocker at $(2k-1)f_{LO} + f_{in}$, the dc commutating mechanism of the switches would transfer the flicker noise of the switches to the output [45].

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Chapter 6

Integrated Wideband Rreceiver Front-End

The UWB front-end can be designed either as direct conversion technique or double conversion technique. So far many designs have been introduced, which utilize the direct conversion receiver (DCR) architecture to implement the wideband receiver front-end [11], [55] and the problems with DCR (zero-IF) are well understood [56]. In the UWB receiver front-end a blocking signal can simply get down-converted with the desired RF band to the baseband frequency. This blocking signal appears as low-frequency second-order distortion, which is generated due to the non-ideality of the receiver stage such as device/load mismatch in the mixer stage and RF self-mixing. A low linear receiver front-end would be more susceptible to the intermodulation products. Apparently, this issue in a wideband receiver is one of the drawbacks, which can severely suppress the front-end performances.

In this paper unlike the conventional method, which employs the direct conversion technique, a half-RF architecture is used to alleviate the even-order distortion and LO leakage issues appeared in the DCR. This architecture, however, poses a number of drawbacks, which are described through the paper.

6.1 Theoretical Calculation of the Receiver Requirements

The receiver front-end is designed based on a double conversion technique, which the first stage results in a half-IF, and second stage is a direct-conversion zero IF architecture. The key specifications for the proposed architecture are noise figure, input second- and third-order intercept point (IIP2 and IIP3), which are derived below. The specifications are calculated from the required signal-to-noise ratio, and the contribution of reciprocal mixing interferences from other bands.

6.1.1 Noise Figure Requirements

The noise figure (NF) requirements of the receiver is calculated from input thermal noise (input noise of the receiver), noise due to the second-order nonlinearity products and noise due to front-end blocks in the receiver. It should be noted that noise from transmitter to the receiver part is ignored in this application since the receiver and the transmitter are not "ON" at the same time. The primary noise sources in the receiver front-end is mostly referred to the LNA and mixer. In addition, the loss associated with the preselect filter (1.1 dB) and TR (transmitter/receiver) switch (0.6 dB) are included in the NF calculation. For a system operating at 480 Mb/s at 2 m, with signal-to-noise ratio (SNR) of 6 dB and a thermal noise power ($P_{Nth} = 10\log(k.T.B.10^3)$) of -86.77 dBm, a NF equal to 6.2 dB is required, where k is Boltzman's constant, T is absolute temperature, and B is channel bandwidth (528 MHz). The strict sensitivity requirement of -73.2 dBm to -80.5 dBm is specified for information data rate of 480 Mb/s (at 2 m) to 110 Mb/s (at 10 m) [7].

6.1.2 Linearity Requirements

For the DCR system the undesirable harmonics can fall in the RF frequency and reduce the system performance. The presence of other systems such as IEEE 802.11b/g, which

operate at 2.4 GHz-2.58 GHz frequency with the output power up to +30 dBm, lead to more challenging adjacent channel blocker rejection. In addition, the in-band interferes from another UWB system should be considered to analyze the system linearity.

One source of the nonlinearity is second-order intermodulation IM2. From definitions, the IM2 products are created at; DC, $f_1 + f_2$ and $f_1 - f_2$. The relationship between the power level of IM2 at $f_1 - f_2$ (sensitivity P_{sens}), interfere power at the input (P_{BLCK}) and second-order intercept point (IIP2) is given as:

$$IIP2_{REQ}\,(dBm) = 2P_{BLCK} - P_{sens} + SNR - 6\,dB \qquad \text{(Eq. 6.1)}$$

where -6 dB represents the 25% IM2 products at $f_1 \pm f_2$ [57]. In the worst-case scenario where a WLAN system is placed at 0.2 m distance, an interferer can reach up to -3 dBm. If the minimum sensitivity of the UWB receiver with 480 Mb/s is -73.2 dBm with SNR = 6 dB, a maximum IIP2 of +67.2 dBm is required. Consequently, high IIP2 performance allows to have a high SNR contribution. Notice that the effect of pre-filtering is not taken into account. The required IIP2 can be lowered if the gain of the pre-filtering is considered. Assuming with an antenna filter, an interferer can be attenuated by +20 dB, which relaxes the required IIP_2 down to 27.2 dBm.

One way to reduce the IM2 nonlinearity of the proposed receiver front-end, is to implement fully differential circuitry to reduce the generated common-mode due to the mismatch between devices. However, a fully differential structure may not be always possible for a stage like LNA in the UWB systems, since it is hard to design a low-loss wideband balun for wideband differential input signal. Therefore, other techniques like single-to-differential (SD) conversion could be used to eliminate the lossy balun in front of the receiver.

For third-order intermodultaion (IM3), which are placed at $2f_1 \pm f_2$ and $2f_2 \pm f_1$, if

two-tones are equal, then the required IIP3 is calculated as

$$IIP3_{REQ}\,(dBm) = \frac{1}{2}\left(2P_{\text{int1}} + P_{\text{int2}} - (P_{sens} - SNR)\right)$$
$$= \frac{1}{2}\left(2P_{\text{int1}} + P_{\text{int2}} - P_{IM3} + Gain\,(dB)\right). \quad \text{(Eq. 6.2)}$$

where P_{int1} and P_{int2} are the received interference powers. If two interfere power levels of -41 dBm and -24 dBm are received from an ISM band and a WLAN system respectively, the required IIP3 with SNR $= 6$ dB would be -9.7 dBm, considering 110 Mb/s data rate.

Depending on the gain of the mixer, the linearity values could be even higher for different applications in the receiver front-end. The gain requirement of the front-end stage, is a trade-off between low-noise and linearity. For instance, the gain of the LNA should be high enough in order to get low NF but not too high to corrupt the linearity requirements. In fact, the gain of the receiver can be compensated by a baseband filter or a variable-gain-amplifier (VGA) stage.

6.2   UWB Front-End Architecture

The proposed receiver architecture is based on a dual-conversion heterodyne technique, which enables for high system integration level and low power applications. A simplified block diagram of the receiver front-end is shown in Fig. 6.1. A SD LNA circuit is designed to avoid the lossy and costly balun in front of the receiver. As shown, after the LNA a two-stage down-conversion mixer is designed to down-convert the wideband RF frequency to the baseband. As a result a $3.1-8$ GHz RF frequency is down converted to zero-IF at the baseband. The output buffers are integrated for the measurement purposes only. The differential output of the mixer is converted into a single I/Q, and drive an external 50 Ω load.
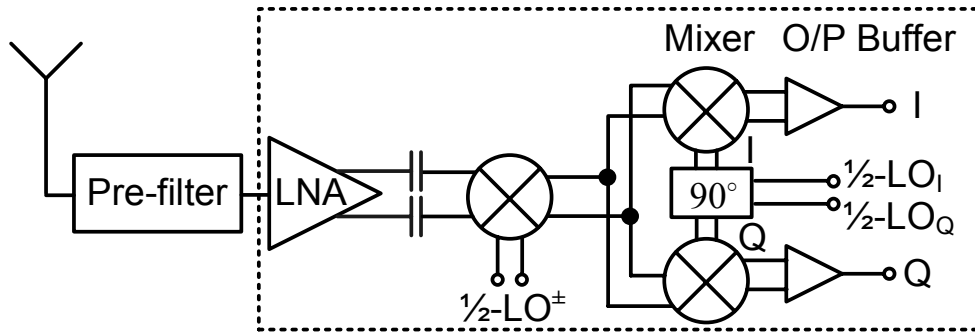
Figure 6.1: Simplified block diagram of the UWB front-end receiver
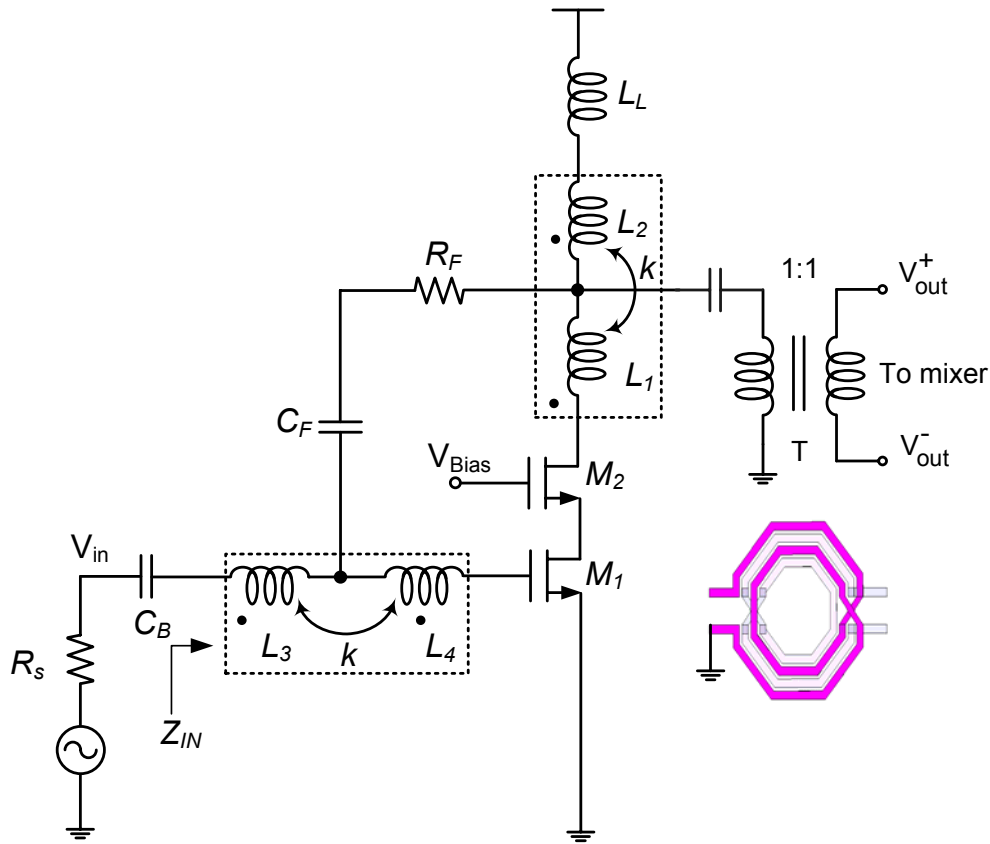
Figure 6.2: Simplified schematic of the UWB single-to-differential LNA (biasing is not shown).

6.2.1   SD LNA with on-chip transformer

In Fig. 6.2, a SD LNA using on-chip transformer is shown. The SD LNA is used with an output transformer load to provide differential output. The output transformer acts

as AC-coupling (high-pass filter), which attenuates the IM2 harmonics generated by the LNA at low frequency. Coupling capacitors were placed between LNA and mixer to remove any DC offsets from LNA. A very low current is consumed in this design, since only one stage is used to generate differential output. More details on the principle of the LNA can be found in [20]. The designed on-chip transformer, improves the integration level of the receiver, which prevent the use of off-chip lossy balun.

In comparison with microwave balun structure, which requires physical dimensions on the order of the signal wavelength, transformers have a relatively smaller size and wider bandwidth. Owing to the octagonal structure of the transformer, less loss is introduced. A symmetric winding style is implemented in the top metal layers to reduce the substrate capacitive loss. The appropriate number of turns $n = 1$ is chosen for two reasons; to provide high quality factor (Q) for better noise figure, and preventing the LNA performances degradation.

Due to the bandpass and AC-coupling properties of the transformer, the low frequency IM2 components of the LNA are attenuated strictly at the output of the transformer. Fig. 6.3(a) shows the transformer model used in this design. When two inductors are tightly coupled ($k \approx 1$), then it is useful to view the coupled inductors are a perfect transformer merged by parasitics. The transformer is modeled with series resistances R_1, R_2, parasitic capacitance of C_p, load capacitance C_L, M that represents the mutual coupling between two inductors L_1 and L_2, and I_{in}, which is the output current of the previous stage, in here LNA. Fig. 6.3(b) is the representation of the circuit in Fig. 6.3(a) with an ideal transformer. The series resistances R_1 and R_2 are represented as

$$R_1 = \frac{R_{p1}}{(1 + Q_1^2)}$$
$$R_2 = \frac{R_{p2}}{(1 + Q_2^2)} \qquad \text{(Eq. 6.3)}$$
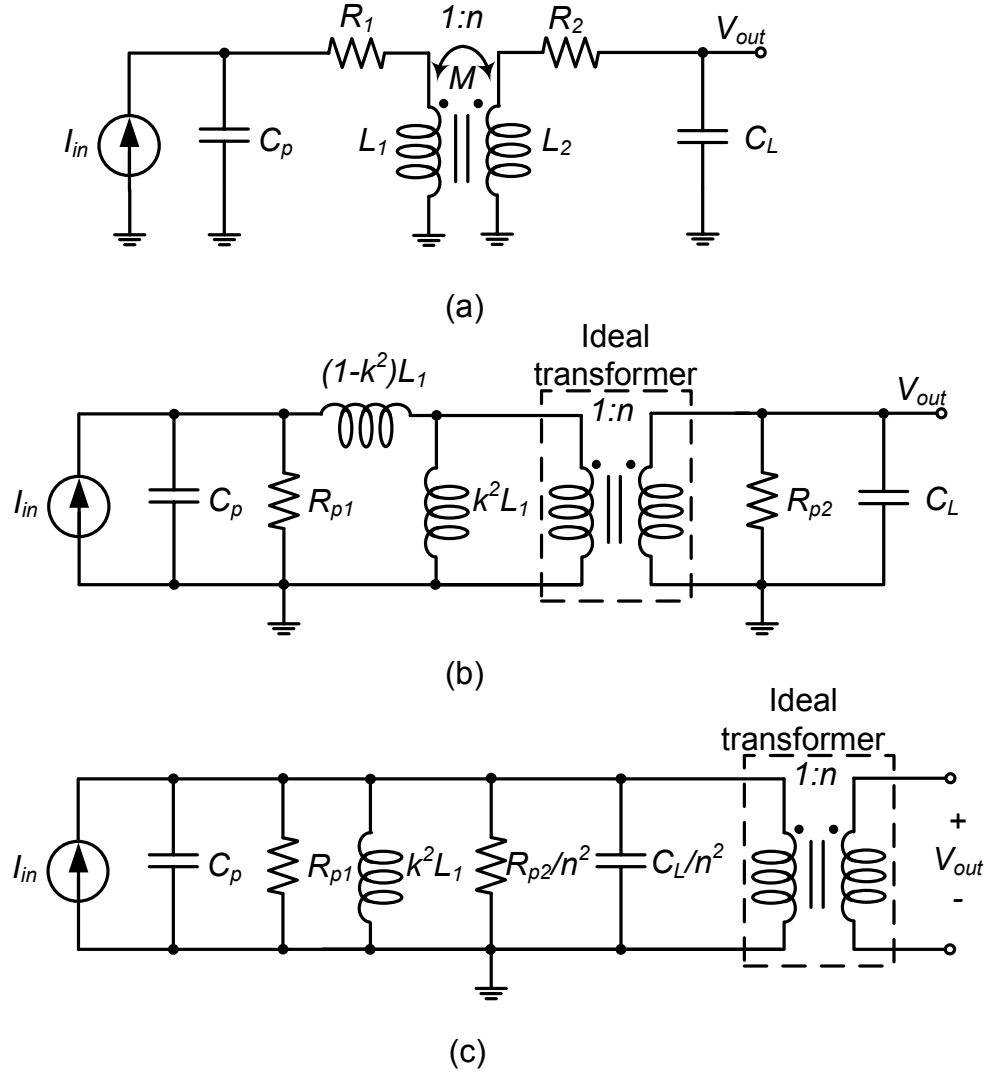
Figure 6.3: (a) Transformer Model. (b) Equivalent circuit model for coupled inductors. (c) Equivalent circuit of (b) with load network transferred to the input.

where Q_1 and Q_2 are the quality factors of the primary and secondary of L_1 and L_2. If we assume that k is very high and approximately equal to 1, then $(1 - k^2)L_1$ is negligible. Therefore, in resonance the voltage at secondary port is n^2 times of the voltage at input port and V_{out} is

$$V_{out} = I_{in} \left(R_{p1} \parallel \frac{R_{p2}}{n^2} \right) n^2 \qquad \text{(Eq. 6.4)}$$

As the number of turns increases, the area occupied by the transformer increases

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Table 6.1: Transformer characteristics

Parameter	Q_{p-max}	Q_{s-max}	L_p	L_s	$f_{res-max}$	k
(1-10 GHz)	8 @ 8 GHz	13 @ 8 GHz	0.58 nH	0.68 nH	14 GHz	$0.67-0.71$

too, which causes an increase in the substrate capacitance and turn-to-turn capacitive coupling. Therefore, the resonance frequency of the transformer reduces. However, more turns induces stronger magnetic coupling, i.e., larger k factor. From layout design point of view, reduction in spacing between secondary and primary layers, improves the magnetic coupling between L_1 and L_2, which leads to higher k factor. However, this space should not be kept as minimum as the technology limit. Because, as secondary and primary layers get closer and closer, the coupling capacitor in between increases, and consequently resonance frequency drops drastically. Therefore, the geometrical parameters of the transformer should be selected with trade-offs.

Form above, a wideband transformer is designed with characteristics indicated in Table 6.1. Fig. 6.4 shows the $S21$ measurement over a wide range of frequency. The transformer was measured separately from $1-10$ GHz, which shows a maximum primary Q of 8 and secondary Q of 13 at 8 GHz frequency.

6.2.2   Down-Conversion Mixer Architecture

In a CMOS down-conversion mixer DC offset and LO-RF feedthrough are the challenging issues and it can desensitize the mixer. Furthermore, in the DCR technique flicker noise $1/f$ is another issue, which appears at the output along with translated RF signal to the baseband frequency. The $1/f$ noise in the mixer distort the signal, and degrades both the noise figure of the receiver and SNR. The $1/f$ noise is partially originated from DC offset leakage due to the mismatch introduced by the switches. In the UWB systems, this issue is less disturbing than a narrowband system, since the baseband bandwidth is beyond $1/f$ noise corner. However, this does not mean that $1/f$ noise can
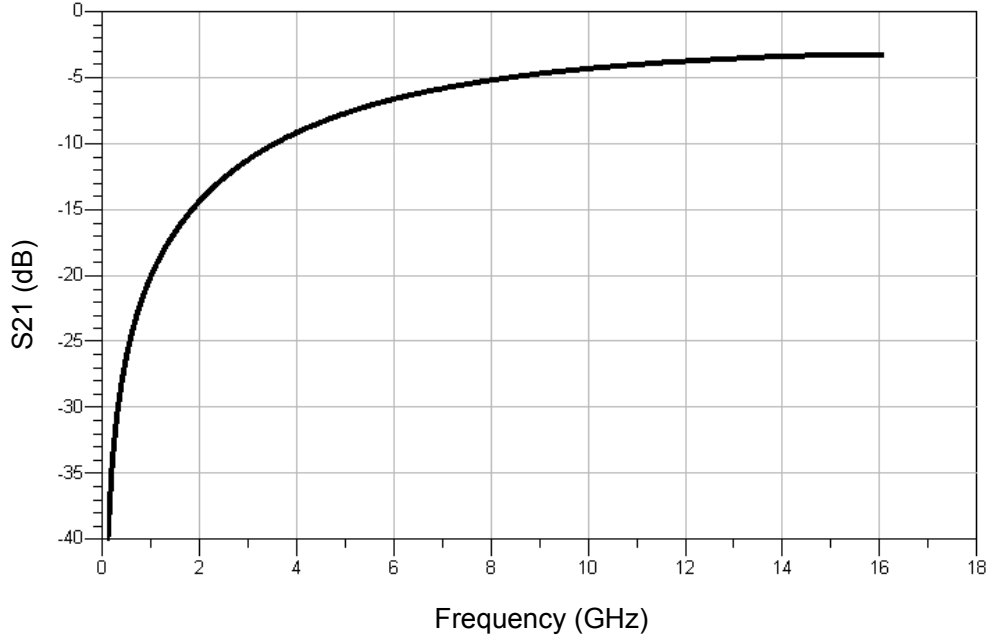
Figure 6.4: S21 measurement of the transformer over a wide frequency range.

be ignored in the design of the UWB systems. The flicker noise can degrade the low frequency part of the receiver's NF. Due to the small size of the MOS transistors, the flicker noise can reach up to few MHz. The flicker noise of the switches down-converts to the baseband and corrupts the IF frequency. In [58], it is discussed that if there is a blocker at $(2k - 1) f_{LO} + f_{RF}$ in a zero IF system, the switch flicker noise would transfer to the baseband output. In this paper, a two-stage down-conversion mixing architecture is introduced in, which $f_{LO} = f_{RF}/2$, is chosen as subharmonic of the RF frequency. The proposed down-conversion mixer is shown in Fig. 6.5(a), which the down-conversion is performed in two-stage with the same LO frequency for both mixers. The first row of transistors $M_1 - M_2$ are the RF transconductance stage, which drive the switching transistors $M_3 - M_6$. The size of the switches are selected to define the proper noise figure and conversion gain of the mixer. The first switching stage down-converts the RF frequency to an intermediate frequency, and the second stage is similar to a direct conversion technique. The second stage experiences the same issues as a conventional

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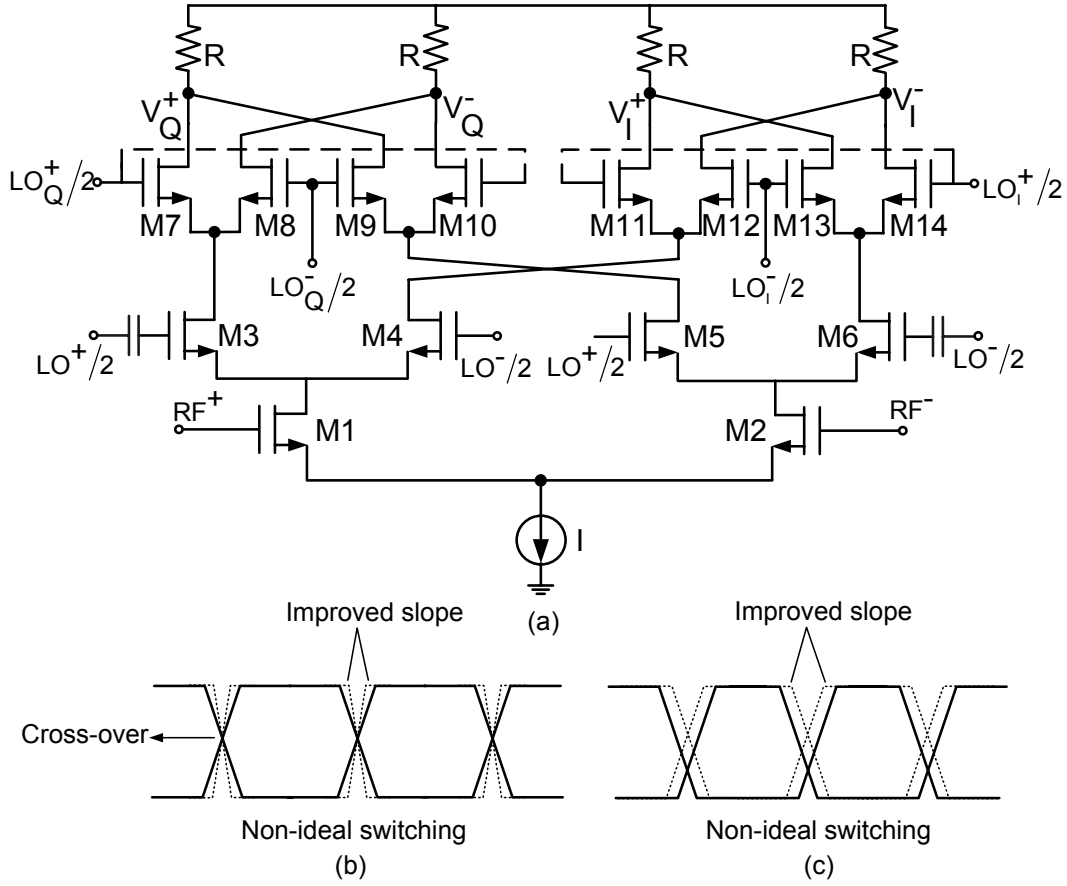
Figure 6.5: (a) Simplified schematic of the double-balanced down-conversion mixer, (b), (c) Non-ideal LO switching and slope improvement

direct conversion receiver does, such as flicker noise. However, having a LO waveform with a large $S \times T$ product, that is, low frequency LO with sharp transition will lower flicker noise of the switching stage, where S is the slope of the LO waveform at cross-over point, and T_{LO} is the LO period [54]. The 1/2-LO signal is applied to the gate of switching transistors stage to modulate the drain voltage of $M_1 - M_2$. The RF frequency is down-converted into 1/2-IF frequency at the drains of $M_3 - M_6$. Therefore, the switching action of $M_3 - M_6$ varies the drain-source voltage and transconductance (g_m) to provide frequency conversion gain. The down-converted signal is translated into the baseband frequency by another 1/2-LO down-conversion stage using $M_7 - M_{14}$ transistors.

The magnitude of the $1/f$ noise is dependent to the process used, size of the devices and topology of the design. Assuming the gate referred voltage of the switches as a slowly varying offset voltage associated with the switching pair. Due to the periodic behavior of LO frequency, ω_{LO}, the voltage offset varies slowly and modulate the gate-referred noise. This modulation results in train of noise pulses, which adds to the square-wave modulation waveform, and appears as flicker noise at the output. The flicker noise at the output of the mixer appears as two mechanisms [54]; zero-crossing modulation (direct mechanism) and induced current in the tail capacitance (C_P) (indirect mechanism). In a down-conversion mixer, the non-ideal properties of the switches causes non-ideal rise and fall time at the LO cross-over. As shown in Fig. 6.5(b), the LO slope at cross-over is reduced due to the imperfect characteristics of the switches and asymmetric layout routing. The idea in half-RF mixer design is that $1/f$ noise of the mixer is inversely proportional to $S \times T_{LO}$, where S is the slope of the LO waveform at cross-over point, and T_{LO} is the LO period [54]. So, since T_{LO} is large in this architecture, the $1/f$ noise contribution to the output is small.

From system design point of view, a mixer that operates at lower frequency has advantages compared to a direct conversion design. For the same architecture and technology, phase-noise performance of a voltage-controlled oscillator (VCO) at lower LO frequency is better than that of a higher LO frequency. For a VCO operating at higher frequency, larger transistor size is required to maintain the oscillation frequency (f_{osc}). At higher f_{osc}, parasitic resistances/capacitances of the transistors and asymmetric routing of the layout, severely affect on the tuning range of the VCO. For the same topology, considering the same phase noise performance, a VCO with higher f_{osc} consumes more power (P_{diss}) than a VCO with lower f_{osc}. In a VCO, which operates at lower frequency, the design of the output buffer is more relaxed. Consequently, a better figure-of-merit (FOM) can be achieved for a VCO operating at low frequency [59].

To investigate the mixer performance degradation due to the switching non-idealities, Fig. 6.5(b) plots non-ideal switching waveforms. As it is shown in solid line, the LO slope at cross-over is reduced due to the imperfect characteristics of the switches and asymmetric layout routing. One way to reduce the LO cross-over window is to increase the LO slope by increasing the LO-power, shown by dotted line in Fig. 6.5(b). A larger LO-power forces the zero-crossing with a greater slope, which reduces the contribution of the direct noise [54]. However, if the high LO voltage derived the FET switches into deep triode region, the nonlinearity of the mixer deteriorates due to the nonlinear resistance of the switches. A sharp square-wave signal can be generated using a frequency divider to redeem the noise. Another issue happens during the switching event, for instance when switch M_6 is ON at LO^+, and M_5 is supposed to be OFF at this period. However, the mismatch between two switches may cause M_5 to conduct for an interval time or vice versa. So ON-resistance R_{ON} of the switch M_5 drop the gate-source voltage of the transconductance stage, which drops the conversion gain reduces. As a result, during this time, flicker noise contribution increases.

As shown in Fig. 6.5(c), the non-ideal LO switching property due to the mismatch between threshold voltages of the switches (biasing voltage and device size mismatch) varies the duty cycle of the switches. Therefore, the ON-time of the transistor, derived with LO^+, can be longer than its OFF-time, which causes the other transistor, derived with LO^-, to have a shorter ON-time than OFF-time. Therefore, undesired signals is generated at the differential output, which can cause second-order intermodulation components (IM2). The ON and OFF times of the switches are determined by the bias voltage, and LO amplitude should be trimmed to reduce the undesired signals due to the mismatch. Beside the threshold voltage mismatch, the coupling from LO to RF port in the presence of the third-order nonlinearity of the transconductor generates IM2. Since the LO signal in direct conversion technique is at the same frequency as the RF carrier,

potentially LO can easily leak to the mixer input and result in time-varying dc offsets. Normally, the LO power is higher than RF power, therefore the LO to RF leakage is more significant than RF to LO leakage. However, in half-RF architecture the local oscillator does not operate at the same frequency of RF carrier. This would eliminate the LO leakage to the RF port. Although the second LO is at the same frequency as the first IF, the self-mixing is relatively constant and can be canceled using the same technique in [60]. Another advantage of this work is that the channel selection is realized with second LO (tunable), allowing the possibility of a programmable channel filtering.

In an architecture, which the down-conversion is performed in two-stage, the flicker noise of the first stage may upconvert to the second stage and then to the IF frequency. In order to improve the noise leakage from the first stage conversion to the output, the second stage is designed in double-balanced topology. By doing this, the LO-IF feedthrough would also improve. Although the flicker noise of the mixer can be improved using PMOS transistors owing to larger length, at the cost of bandwidth reduction.

Fig. 6.6, shows a flicker noise simulation comparison between two types of the mixer. The conventional direct-conversion mixer shows much higher corner frequency than the proposed mixer. Since the baseband bandwidth in this application is very wide compare to many other narrowband designs, the corner frequency is higher than other narrowband applications. In the UWB application, since the baseband bandwidth is much wider than narrowband bandwidth, it is not possible to increase the size of the devices indefinitely for better flicker noise, because the baseband bandwidth reduces due to the parasitic capacitances.

A disadvantage of the proposed architecture is that I/Q mismatch causes the image of the signal to lie nearby zero. However, since the intermediate frequency of the first down-conversion is high enough (1/2-RF), preselect filter at the antenna can suppress the image. Furthermore, the signal at zero frequency can be filtered-out by coupling
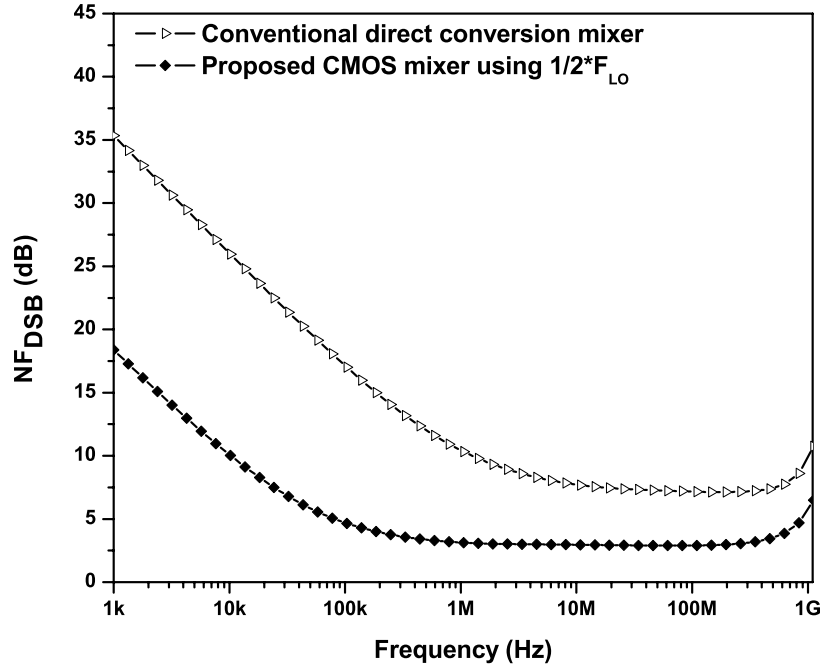
Figure 6.6: Flicker noise comparison between different types of the mixers.

capacitors before the mixer. So the design of image rejection filter cab be more relaxed in this architecture compared to other designs [61].

In the proposed mixer, the required linearity and gain are set by proper selection of the load. For high linearity, the output impedance should be lower than the output impedance desired for high gain. For this design, the load is selected for reasonable gain and high linearity. Although a current-mode load is more popular in low voltage design and provides high gain-conversion, but it is at the expense of higher mismatch. The mismatch in the current-mode load contribute more to the IM2 and DC offset, while resistive load has lower mismatch. Moreover, the parasitic capacitance of the current-mode output load create a low-pass filter with cut-off frequency of $1/R_{load}C_{load}$ at the output load, which reduces the IF bandwidth, where C_{load} is the parasitic capacitance of the current-mode switches. Hence, to improve the output bandwidth of the switching stage, the resistive output load is used instead of current-mode output load.
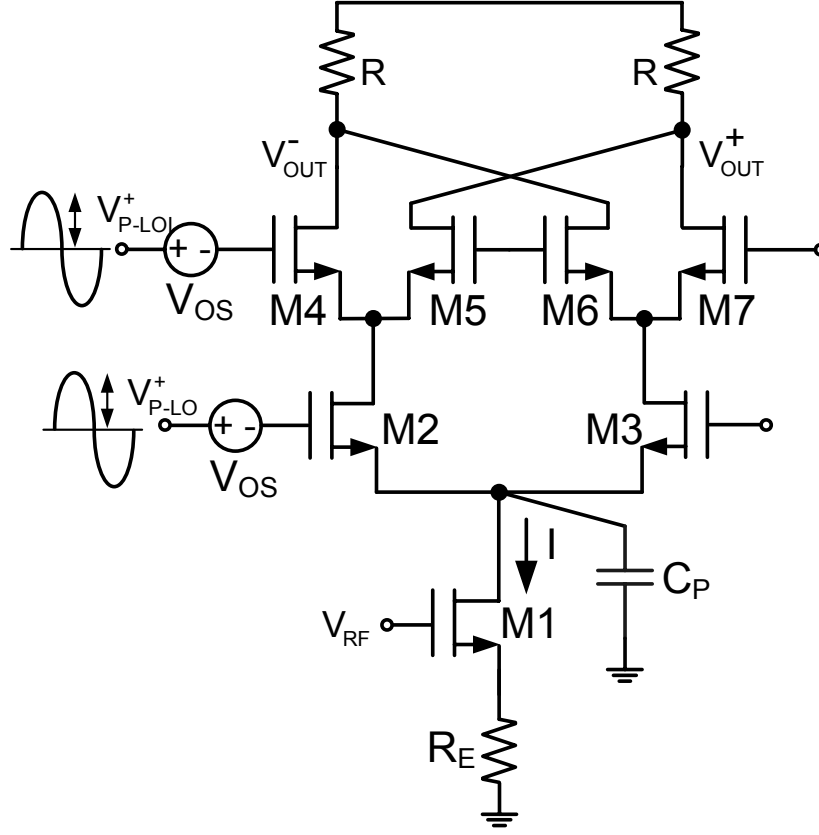
Figure 6.7: A single-balanced mixer with offset voltage at gate.

Optimization of the mixer requires to adjust the LO-power and dc bias. The level of the LO-power is important to ensure that mixer reaches its peak linearity or "sweet spot". To further investigate the linearity of the mixer, both nonlinearity of the transconductance and output conductance of a single transistor [62] are included in the drain-current in the Taylor-series expansion:

$$i_{ds}(v_{gs}, v_{ds}, v_{os}) = g_{m1}(v_{gs} + v_{os}) + g_{ds1}v_{ds}$$

$$+g_{m2}(v_{gs} + v_{os})^2 + g_{ds2}v_{ds}^2 + c_{m1}(v_{gs} + v_{os})v_{ds}$$

$$+g_{m3}(v_{gs} + v_{os})^3 + g_{ds3}v_{ds}^3 + c_{m2}(v_{gs} + v_{os})v_{ds}^2$$

$$+c_{m3}(v_{gs} + v_{os})^2 v_{ds} + ... \qquad \text{(Eq. 6.5)}$$

where c_{mx} describes cross-modulation term, v_{os} is the offset voltage source in series with

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the gate of the transistor, Fig. 6.7, g_{ds} is output conductance, and g_{mx} is the transconductance term. In (Eq. 6.5) the dependency of the i_{ds} with v_{gs}, v_{ds}, and v_{os} are shown, which by reducing the dependency on v_{ds} and v_{os} higher linearity is obtained. In order to achieve a high linearity, drain should be short-circuited at the unwanted mixing frequencies. Consequently the feedback path through c_{gd} is eliminated and undesired harmonics would not pass through c_{gd} to the gate. If v_{gs} of the switch increases, the FET device drops into the linear region, as v_{ds} keeps reducing. As a result, the transconductance reduces, which reduces the output conversion gain. Concurrently, g_{ds} increases, which causes the average output conductance to increase. The increase in the output conductance introduces more source of nonlinearity.

The threshold mismatch between two transistors laid out side by side, introduces offset voltage v_{os} in (Eq. 6.5). Therefore, IIP2 can be improved further by increasing the LO-power or reducing the offset voltage. However, the LO-RF isolation may be affected by increasing the LO-power. A careful layout design helps to reduce the offset voltage due to the mismatch between devices, and subsequently higher IIP2 is obtained. The IM2 products of the LNA is strictly attenuated by the transformer, which adds to the advantages.

If we assume that the LO-power is large enough, and mixing function is observed by commutation of the RF transconductance with LO square-wave $sq\,(\omega_{LO})$, ignoring the effect of R_E and up-converted terms, the output load current is derived as

$$I_{out} = g_{m1}V_{RF}\,(t)\,V_{LO}\,(t)$$

$$= (I_{DC} + g_{m1}\sin\omega_{RF}t) \times (V_{LO}(t) + \Delta_{offset})$$

$$= \frac{2}{\pi}g_{m1}V_{RF}\,(t)\,(\cos\,(2\omega_{LO} - \omega_{RF}))\,(I_{DC} + \Delta_{offset}) \qquad \text{(Eq. 6.6)}$$

$$V_{LO}(t) = \frac{4}{\pi}\sum_{n=1}^{\infty}\left(\frac{1}{n}\right)\cos\,(2n\omega_{LO}t). \qquad \text{(Eq. 6.7)}$$
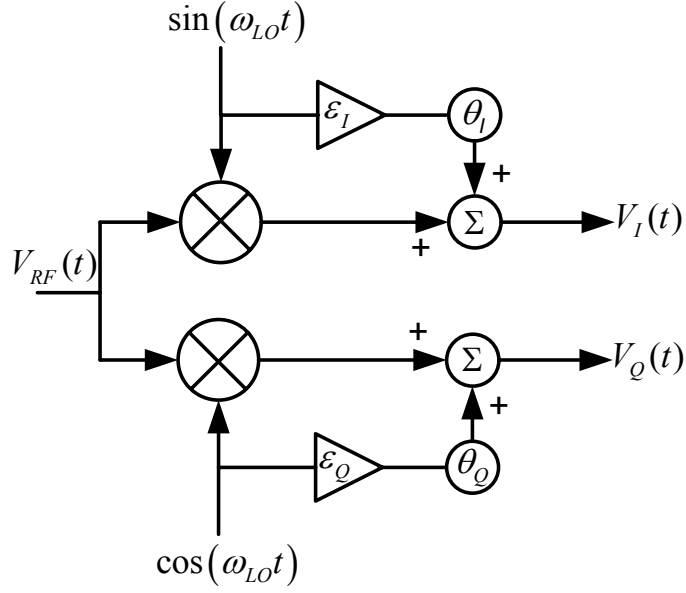
Figure 6.8: I/Q receiver model with I/Q imbalance.

where down-converted output frequency is shown as $2\omega_{LO} - \omega_{RF}$, I_{DC} is the DC current associated with RF components and Δ_{offset} is the DC offset due to the changes in duty cycle over 2π period $\left(= \frac{\Delta T}{2\pi}\right)$. From (Eq. 6.6), the overall voltage gain of the mixer is determined as

$$\text{Mixer Gain} = (2/\pi)\, g_{m1} \left(R \parallel R_{out,mixer}\right) \qquad \text{(Eq. 6.8)}$$

where R is determined by the load resistance and $R_{out,mixer}$ is the output impedance looking into drain of the switching stage when LO voltage is applied. The switching stage of the mixer is biased at $V_{GS} - V_t =$ 0.25 V to keep the switches in the saturation region, with total biasing current of 1.2 mA. Simulation shows that this bias voltage keeps an agreement between the linearity and noise figure as well. Further increase in biasing voltage may cause the output voltage to be clipped, which reduces the conversion gain.

6.2.2.1 I/Q mismatch

In practice, there are always mismatch in phase and amplitude between I and Q signals in the mixer, as modeled in Fig. 6.8. The I/Q imbalance is introduced by the local oscillator as amplitude mismatch ε and phase mismatch θ. According to the model,

$$V_Q(t) = V_{RF}(t).\cos(\omega_{LO}t) + \varepsilon_Q.\cos(\omega_{LO}t + \theta_Q). \qquad \text{(Eq. 6.9)}$$

$$V_I(t) = V_{RF}(t).\sin(\omega_{LO}t) + \varepsilon_I.\sin(\omega_{LO}t + \theta_I). \qquad \text{(Eq. 6.10)}$$

we can rewrite (Eq. 6.9) and (Eq. 6.10) as

$$V_Q(t) = A\cos(\omega_{LO}t + \alpha). \qquad \text{(Eq. 6.11)}$$

$$V_I(t) = B\sin(\omega_{LO}t + \beta). \qquad \text{(Eq. 6.12)}$$

where

$$A = \sqrt{(V_{RF}(t) + \varepsilon_Q\cos(\theta_Q))^2 + (\varepsilon_Q\sin(\theta_Q))^2}. \qquad \text{(Eq. 6.13)}$$

$$\alpha = \tan^{-1}\left(\frac{\varepsilon_Q\sin(\theta_Q)}{V_{RF}(t) + \varepsilon_Q\cos(\theta_Q)}\right). \qquad \text{(Eq. 6.14)}$$

and

$$B = \sqrt{(V_{RF}(t) + \varepsilon_I\cos(\theta_I))^2 + (\varepsilon_I\sin(\theta_I))^2}. \qquad \text{(Eq. 6.15)}$$

$$\beta = \tan^{-1}\left(-\frac{V_{RF}(t) + \varepsilon_I.\cos(\theta_I)}{\varepsilon_I.\sin(\theta_I)}\right). \qquad \text{(Eq. 6.16)}$$

It should be noted that $\varepsilon_I, \varepsilon_Q$ and θ_I, θ_Q in I and Q branches are independent and asymmetric respectively. The first parts in (Eq. 6.9) and (Eq. 6.10) denote the down-converted signal and second terms are the frequency components created by the amplitude and phase mismatch. In order to reduce the imbalance in phase and amplitude in two branches the following equalities should be satisfied, $V_Q(t) + V_I(t) = 0$, $A = B$ and

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$\alpha - \beta = \pi/2$. Reduction in mismatch would improve the performances especially second-order harmonic. Now, if we simplify (Eq. 6.5) and consider the second-order nonlinearity generated by the third-order nonlinearity

$$V_o(t) = \alpha v_{in}(t) + \alpha_3 v_{in}^3(t) \qquad \text{(Eq. 6.17)}$$

where α_a and α_3 are the small-signal voltage gain and third-order distortion coefficient. In order to find the second- and third-order intermodulation distortion due to the LO leakage, putting (Eq. 6.11) and (Eq. 6.12) in (Eq. 6.17), and let $V_X(t) = V_{RF}(t) \cos(\omega_{LO}t)$, the output voltage at Q side is give by

$$V_{out}(t) = \alpha_1 \left(V_X(t) + \varepsilon_Q \cos(\omega_{LO}t + \theta_Q) \right)$$
$$+ \alpha_3 (V_X(t) + \varepsilon_Q \cos(\omega_{LO}t + \theta_Q))^3$$
$$= \cdots + \left(\alpha_1 + 3\alpha_3 \varepsilon_Q^2/2 \right) V_X(t) + \cdots$$
$$+ 3\alpha_3 \varepsilon_Q \cos(\omega_{LO}t + \theta_Q) V_X^2(t) + \cdots. \qquad \text{(Eq. 6.18)}$$

The second term reveals the second-order nonlinearity intermodulation at the output of the mixer. Referring to [63], the input level at each frequency over the amplitude of the output components at second-order nonlinearities is

$$V_{IIP2} = \frac{\alpha_1 + 3\alpha_3 \varepsilon_Q^2/2}{3\alpha_3 \varepsilon_Q} \qquad \text{(Eq. 6.19)}$$

For the I side the same calculation is applied. The impact of the mismatch, which clearly affects the IIP2 should be considered.

Recalling from [63], the input referred voltage intercept point for third-order two tone-intermodulation is given by

$$V_{IIP3} = \sqrt{\frac{4\alpha_1}{\alpha_3}}. \qquad \text{(Eq. 6.20)}$$

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If we plug (Eq. 6.20) into (Eq. 6.19), the relationship between IIP2 and IIP3 is obtained as follows

$$V_{IIP2} = \frac{V_{IIP3}^2}{4} + \frac{\varepsilon_Q}{2} \simeq \frac{V_{IIP3}^2}{4\varepsilon_Q}. \qquad \text{(Eq. 6.21)}$$

where this approximation is valid for small values of ε_Q. This expression lead us to a conclusion that, IIP2 of the mixer in presence of LO leakage is directly proportional to IIP3. Therefore, an improvement in IIP3 reduces the second-order distortion, and improves IIP2, respectively. Another important point in (Eq. 6.21), is the reverse relation of the LO leakage to the IIP2. In this work, it is tried to use this concept to improve IIP2 and IIP3 without further circuit implementation. Although, much delicate circuit implementations are needed to be designed for much better IIP2 and IIP3 performances.

6.3 Instrumentation Amplifier Used for Measurement

An instrumentation amplifier, Fig. 6.9, is a closed-loop gain block that has a differential input and an output that is single-ended with respect to a reference terminal. Most commonly, the input impedances of the input terminals are balanced and have high values. High input impedance is necessary to avoid loading the previous stage. As with opamps $(A1 - A3)$, output impedance is very low, nominally only a few Milli-ohms, at low frequencies. An instrumentation amplifier (inst-amp) employs an internal feedback resistor network that is isolated from its signal input terminals.

The inst=amp must be able to handle very low input voltages, and also should not add its own noise to the system. Furthermore, an instrumentation amplifier must provide sufficient bandwidth for the particular applications, such as measurement in here. Since typical unity gain small-signal bandwidth fall between 500 KHz and 4 MHz, performance at low gain is easily achieved, but at higher gain bandwidth becomes much more of an issue.
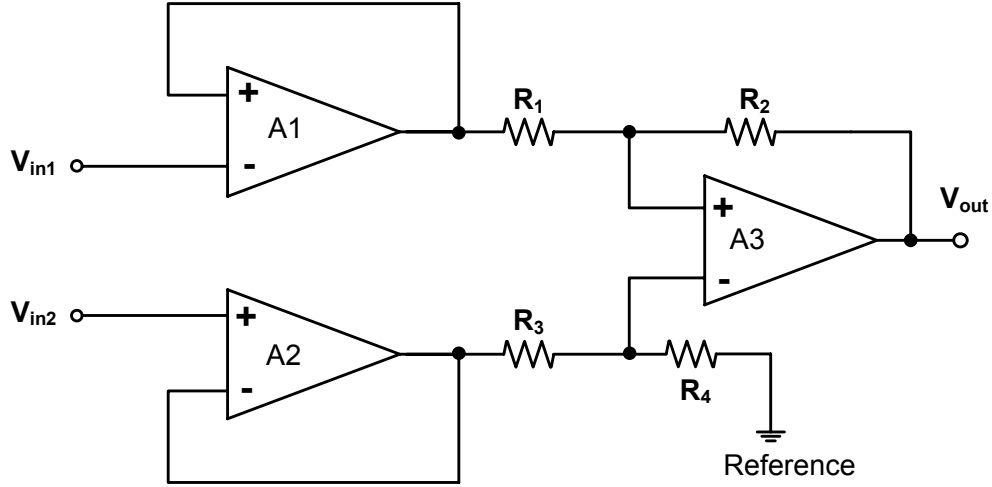
Figure 6.9: Instrumentation amplifier used for measurement setup.

The circuit in Fig. 6.9 shows a 3-opamp in one inst-amp block. If $R_1 = R_3$ and $R_2 = R_4$, then

$$V_{out} = (V_{in2} - V_{in1})\left(\frac{R_2}{R_1}\right). \qquad \text{(Eq. 6.22)}$$

This circuit provides an inst-amp function, amplifying differential signal while reject-ing those that are common mode. In addition, it provides matched, high impedance inputs so that the impedances of the input sources will have a minimal effect on the circuit's common-mode rejection. The designed inst-amp will match the output of the receiver front-end to a 50 Ω output, which is the impedance of the probe station used for measurement.

6.4   Measurement results

The wideband receiver front-end is fabricated in 0.18 μm CMOS technology, shown in Fig. 6.10, which occupies an area of 0.84×1.06 mm^2. A low frequency power-combiner at the output converts the differential output into a single-ended signal for measurement. A quadrature LO is applied off-chip using a signal-generator through a wideband balun
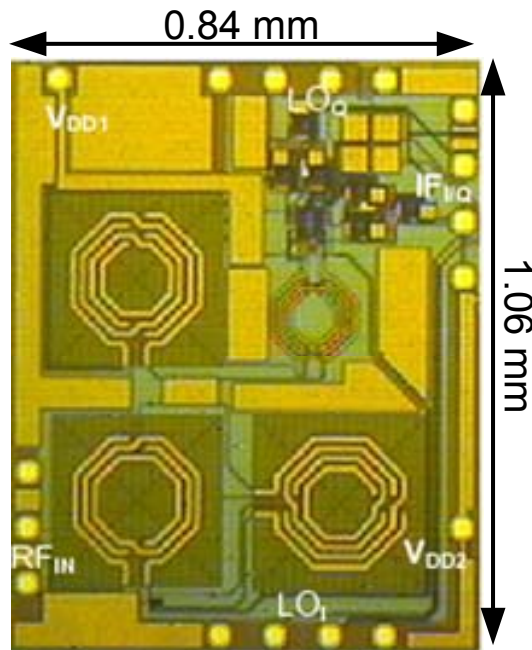
Figure 6.10: Chip microphotograph of the wideband receiver.

and 90° hybrid coupler. From measurement results, the LNA consumes a total current of $I_{LNA} = 2.45$ mA from a 1.8 V supply voltage. The proposed mixer is derived with $V_{DD2} = 2.2$ V to alleviate the headroom issue. The measured input return loss (S_{11}) is plotted in Fig. 6.11 showing a reasonable input matching from $3.1-8$ GHz, which satisfies the requirements. The fluctuation of the graph is expected from measurement setup. In order to make sure that the measurement is valid, all the tests are repeated for almost 10 cheaps. Due to the process variations there are differences between the performances of the one cheap to the other cheap.

The conversion gain (CG) of the receiver is measured and simulated at the output of an on-chip unity-gain buffer, shown in Fig. 6.12. The peak gain is about 39.2 dB. The frequency response of the receiver can be improved with a wider-band baseband filter for higher data rate. The measured 3-dB bandwidth is shown, which is lower than the simulation. The reduction in bandwidth can be described based on the on-chip parasitics, forming a low-pass filter. Furthermore, the unity-gain buffer should be designed with
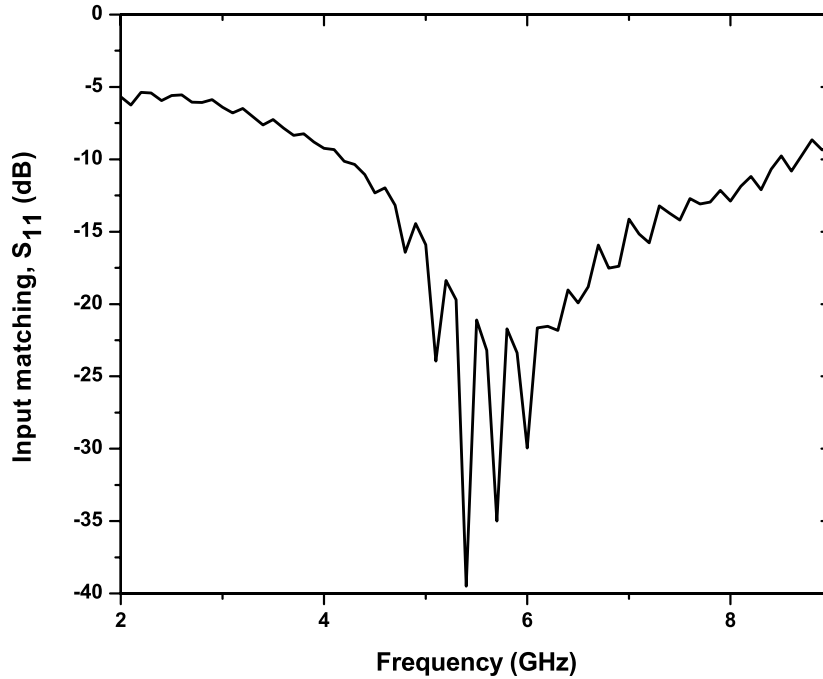
Figure 6.11: Measured input reflection coefficient of the receiver.

much wider bandwidth, although this unity buffer is used for measurement purposes, which in an integrated front-end receiver would be replaced with a channel select filter. The CG's ripple from $3.1-8$ GHz is about 2.5 dB. In order to evaluate whether the circuit can handle large input signals the two-tone test was carried out. For the third-order intermodulation test, two signal with the same amplitude spaced with 10 MHz, were applied to the RF port for $3.1-8$ GHz. Similarly, for the second-order intermodulation test, two-tone were used to measure IIP2. The second-order intermodulation test was simulated directly at the output of the mixer, which shows IIP2$_{max}$ > 48 dBm. The measured IIP2's are listed in table 6.2. Since the off-chip components can have different behavior from frequency to frequency, a small phase or magnitude imbalance in the RF or LO input baluns and hybrid coupler easily dominates the IIP2 measurements. Therefore, it is important to make sure that these devices have the lowest phase imbalance at their operating frequency. Generally, wideband off-chip baluns have high loss and phase

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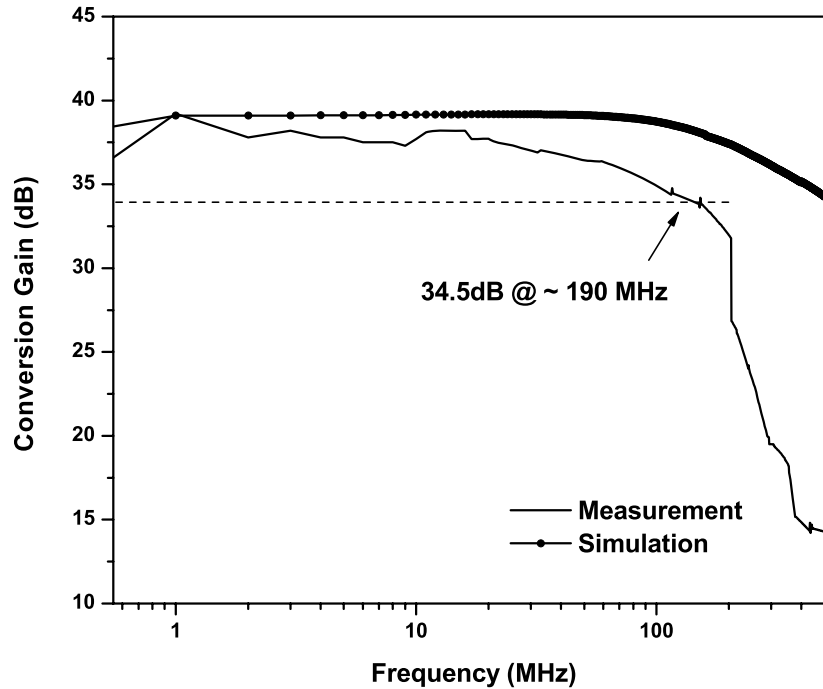
Figure 6.12: Measured/Simulated conversion gain of the receiver at 8 GHz.

imbalance. In order to guarantee the accuracy of the measurement, all losses of the cables and balun were considered during the measurement. In addition, the output unity-gain buffer can degrade the IIP2 performance too.

In Fig. 6.13 the measured third-order intermodulation is shown at 4.48 GHz frequency, for instance. Two-tones are applied at 4.48 GHz and 4.47 GHz respectively, while LO is at 2.2 GHz frequency. The 1 dB difference between the two fundamental tones at 49.96 MHZ and 59.94 MHz, in Fig. 6.13 (screen captured graph), is suspected from uncertainties of the off-chip wideband balun at LO port. Since the wideband off-chip baluns are not very accurate through the whole range of frequency, the phase and amplitude imbalance at the output of the balun may cause distortion in the measurement. The distortion is negligible at the frequencies, which balun has the lowest phase and amplitude imbalance. Similarly, the measured second-order intermodulation of the UWB front-end receiver at 7.21 GHz is plotted in Fig. 6.14.

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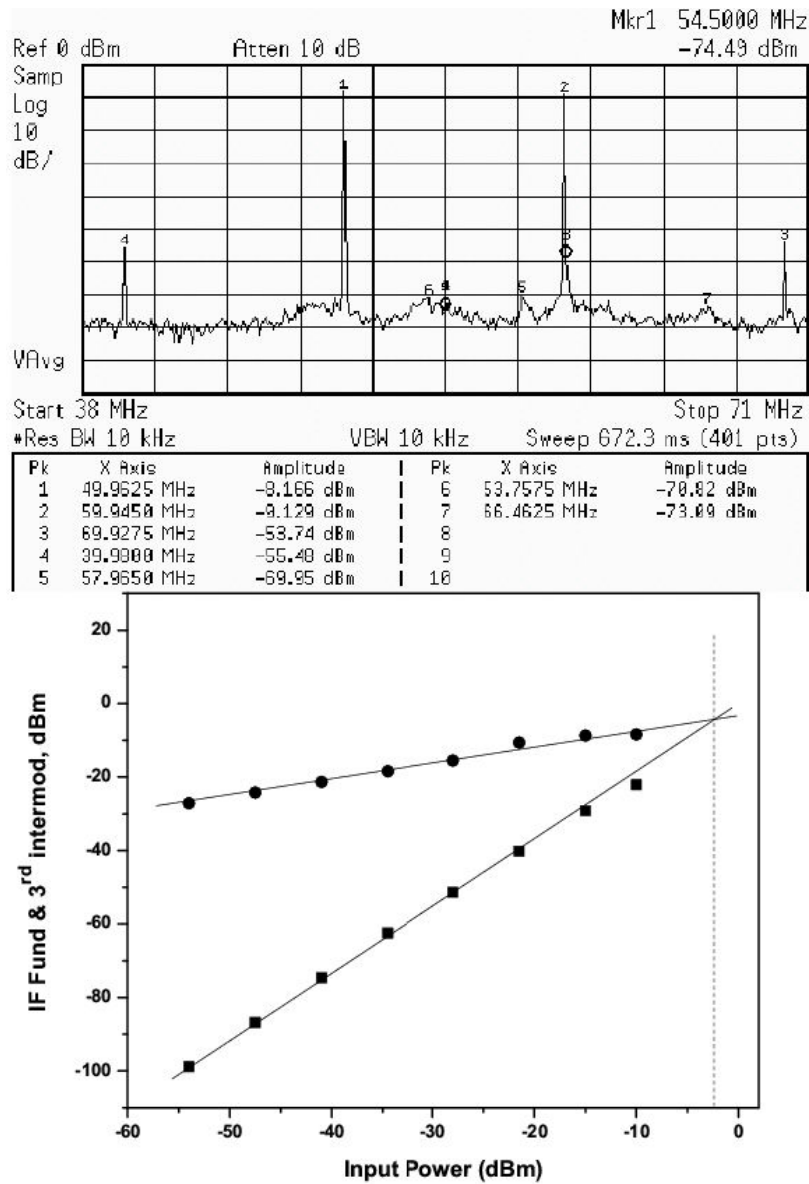
Figure 6.13: Measured IIP3 at 4.48 GHz frequency.

Table 6.2 summarizes some performances of the circuit. Since the LO signal is stronger than the input RF signal, LO-RF coupling is measured to test the effect on the second order intermodulation. The measured LO-RF and LO-IF isolation is plotted in Fig. 6.15. The LO-IF isolation may not be very high since the first stage of the mixer produces an IF equal to the LO frequency. With a low coupling voltage from LO-RF port, a maximum
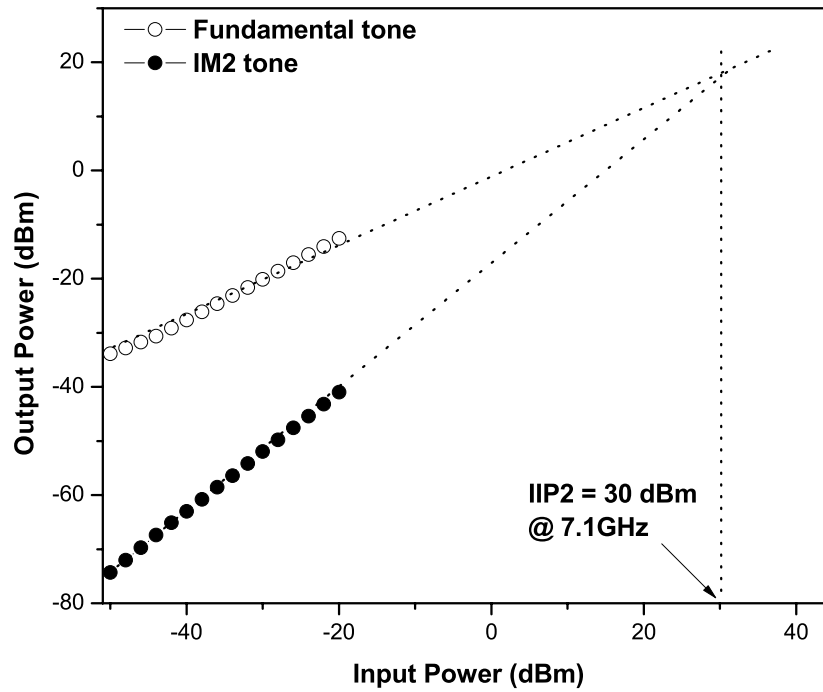
Figure 6.14: Measured IIP2 at 7.12 GHz frequency.
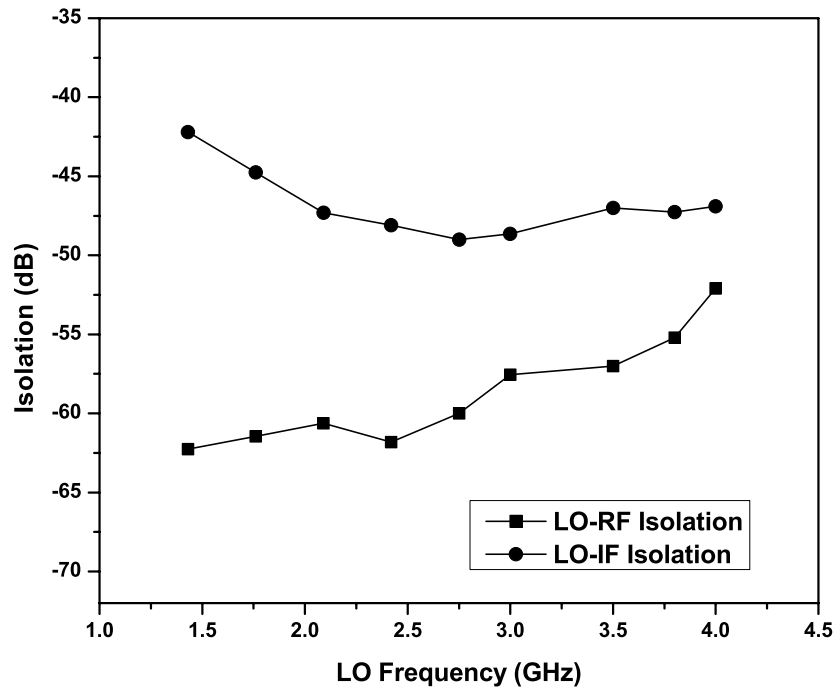
Figure 6.15: Measured isolation of the LO and IF to the RF port.

Table 6.2: Performance summary of the receiver front-end

RF Freq.* (GHz)	Gain$_{max}$ (dB)	IIP3 (dBm)	IIP2 (dBm)	NF (dB)	P1 dB
3.43	32.4	0	33	8.3	-11
4.48	36.1	-2.5	28	5.4	-14
6.6	34	0	29	7.1	-12.1
7.12	35.54	+3.5	30	6	-10.5
7.65	34.8	+3.8	27	7	-10.8

* The LO frequency is selected half of the RF frequency.

value of IIP2 is achievable [64] and less unwanted signals are presented at the output.

In order to measure the noise figure and flicker noise corner frequency, if possible, a wideband low-noise voltage amplifier with a known gain and a bandwidth wider than 500 MHz is used to boost the front-end noise above the noise floor of the spectrum analyzer to reduce the measurement uncertainties. Due to the spectrum analyzer limitations, the flicker noise frequency was extrapolated based on the readings on the spectrum analyzer. The noise figure is measured at different frequencies with a constant IF, recorded in table 6.2. Furthermore, the noise figure is measured at other IF frequencies lower than 120 MHz. Since the input matching at 3.1 GHz is slightly deviated away, the noise figure at this frequency is higher than other frequencies. The input 1-dB compression point is measured at different frequencies as shown in table. 6.2. Two different single tones are applied at f_{RF} and f_{LO}, respectively. The input amplitude of the RF signal is swept, and the output power of the receiver is measured accordingly. The measured gain compression of the output versus RF input power is plotted to find the 1-dB compression point. The performance of the proposed front-end receiver is compared to the other references in Table 6.3.

Table 6.3: Performance Comparison Table

Ref.	Bandwidth (GHz)	Gain$_{max}$ (dB)	IIP3 (dBm)	IIP2 (dBm)	NF (dB)	Power (mW)	Technology
This work	3−8	36.1	> -2.5	< +33	5.4−8.3	50.4*	0.18 μm CMOS
[65]	3−10	15.5	> -6.6	−	5.2−5.4	14.8	0.13 μm CMOS
[66]	3−10	29.1	-13.5	−	4.9−8.8	33	0.13 μm CMOS
[67]	3.1−8	23.2	>-3	<+46	5.2−7.3	18	0.18 μm CMOS9T
[68]	3−5	37	-22	−	3.6−4.1	51$^{\times}$	0.13 μm CMOS

* Including output buffer. LNA+Mixer consume less than 8 mW. $^{\times}$ w/o test buffer.
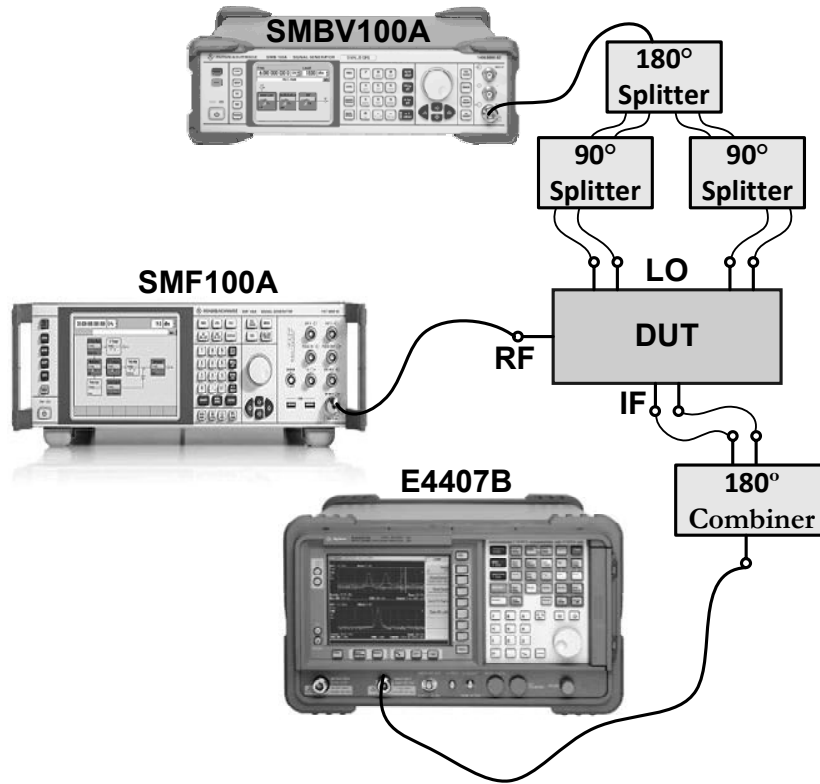

Figure 6.16: Gain measurement setup.

6.5 Measurement Setup Structure

The gain measurement structure of the whole receiver front-end is shown in Fig. 6.16. Note that for an accurate measurement all the cables should have the same length and

shorter cables are preferred over long cables due to their lower losses. The gain of the device under test (DUT) is found as

$$Gain_{receiver} = Gain_{total} - Gain_{buffer} - Gain_{cable-loss} - Gain_{combiner-loss}. \quad \text{(Eq. 6.23)}$$

For noise figure measurement, there are three methods as; Gain method, Y-factor method, and the noise figure meter method. The gain method involves in more measurement steps as well as calculations, but under certain conditions, they turn out to be more accurate. From definition, noise is due to two effects. One is the interference that comes to the input RF system in the form of signals that differ from the desired one. The second is due to the random fluctuation of carriers in the RF system (LNA, mixer, receiver, etc). This effect is a result of Brownian motion [69] of the electrons in device, which is equal to $kT\Delta F$, where $k = 1.38 \times 10^{-23}$ Joules/ΔK, T is temperature in Kelvin and ΔF is the noise bandwidth (HZ). At room temperature (290 ΔK), the noise power density is -174 dBm/Hz. Therefore, from following equation the noise figure is calculated

$$NF_{Gain-method} = 174 dBm/Hz + 10 \log(BW) + Gain + P_{Nout} \quad \text{(Eq. 6.24)}$$

where "BW" is the bandwidth of the output channel, "Gain" refers to the system gain, and "P_{Nout}" is the measured total output noise power. In order to use this method, the gain of the DUT should be predetermined. To measure the P_{Nout}, the input of the DUT is terminated with the 50 Ω impedance, and then the output noise power density is measured with a spectrum analyzer.

In the Y-factor method, which is one popular method for the noise figure measurement, a noise source with known ENR (Excess Noise Ratio) is needed. The setup for the Y-factor method measurement is shown in Fig. 6.17. The ENR accuracy of the noise source contributes heavily to the accuracy of the noise figure measurement. The ENR values provided by the manufacturer assumes perfect matching. Consequently, any

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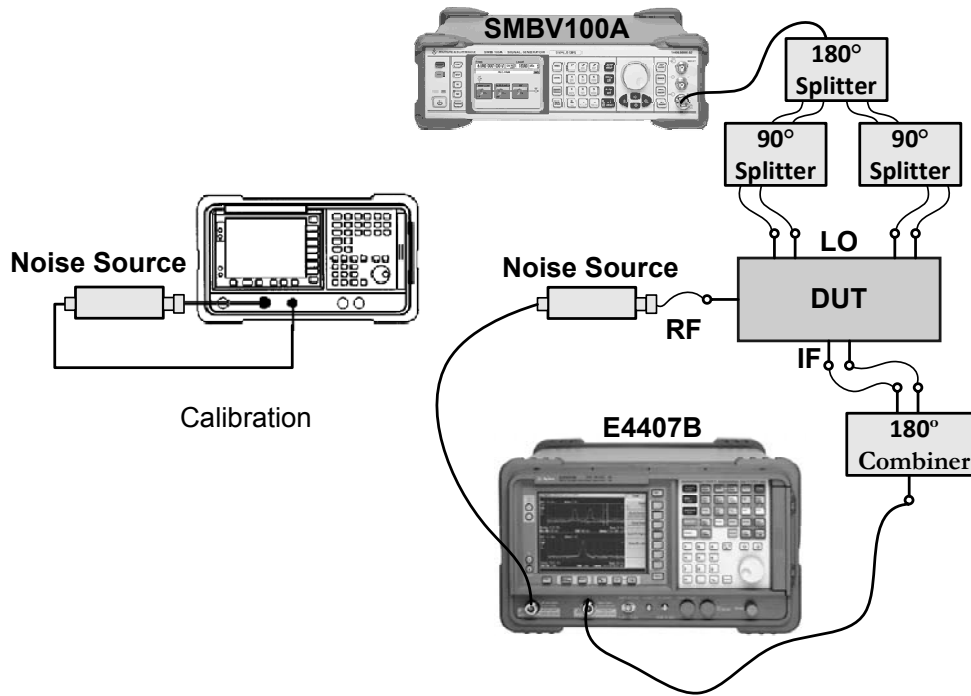
Figure 6.17: Y-factor method in noise figure measurement setup.

mismatches introduces significant ENR inaccuracies. The noise figure in this method is measured by

$$NF_{Y-method} = 10 \log \left(\frac{10^{(ENR/10)}}{10^{(Y/10)} - 1} \right) \qquad \text{(Eq. 6.25)}$$

where Y is the difference between the output noise power density when the noise source is on and off.

In the last method, the noise figure meter generates a pulse signal to drive a noise source to derive the DUT. The output of the DUT is then measured by noise figure analyzer. Since the input noise and signal-to-noise ratio of the noise source is known to the analyzer, the noise figure of the DUT can be calculated internally and displayed.

In the receiver front-end measurement, the noise figure was measured both by the gain method and Y-factor method. However, since in the Y-factor method an accurate wideband noise source at low frequency is hard to find, we mostly relied on the gain-method for the noise figure measurement.

6.6 Alternative Linearity and IIP2 Improvement

The sever linearity and IIP2 requirements in a system architecture, led us to use of the MOS transistor in its triode region since this allow a direct control on the MOS's transconductance value through its V_{DS}. Indeed, the first-order approximation of the drain current I_D of a triode transistor is

$$I_D = \mu_n C_{OX} \left(\frac{W}{L}\right) V_{DS} \left(V_{GS} - V_T - \frac{V_{DS}}{2}\right). \qquad \text{(Eq. 6.26)}$$

The derivation of the $v - i$ characteristic yields

$$g_m = \frac{\partial i_D}{\partial v_{GS}} = \mu C_{OX} \left(\frac{W}{L}\right) V_{DS}. \qquad \text{(Eq. 6.27)}$$

It can be seen by (Eq. 6.26) and (Eq. 6.27) that g_m is proportional to V_{DS} and does not depend on other voltages such as V_{GS} for instance. This perfectly linear relation remains valid between output current and input voltage as long as the MOS transistor remains in the triode region

$$(V_{GS} - V_T > V_{DS}). \qquad \text{(Eq. 6.28)}$$

Consequently, an alternative method to improve the linearity of the mixer is to design a very linear transconductor stage. This means that the MOS transistors in the transconductor stage has to have a nearly constant drain-source voltage (V_{DS}) over the process variations. The proposed method shown in Fig. 6.18 is based on transconductance stage which is introduced in [70] for BiCMOS continuous time filter. The MOS transistors M_1 and M_2 are adjusted to operate in triode region. In order to fix the V_{DS} of M_1 and M_2, Q_3 and R_{tune} are designed to act as a linear voltage source. The V_{DS} of both transistors are then equal to $V_{DS} = V_{BE3} + V_{tune} - V_{BEQ}$, meaning that V_{DS} of M_1 and M_2 would similarly change. Due to the high g_m property of BJT the variation of the V_{DS} in M_1 and M_2 which is originated from device mismatch, is introduced.
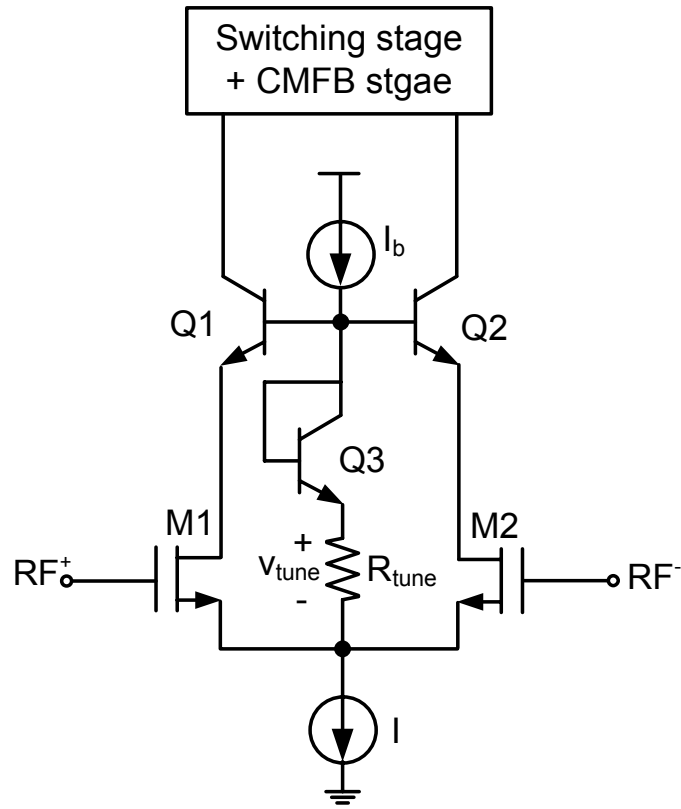
Figure 6.18: Schematic circuitry of the mixer with linear transconductor stage.

Fig. 6.19 illustrates the IIP2 improvement in the proposed technique compare to the conventional direct conversion design over the wide range of LO frequency. In this simulation mismatches are introduced in the device size and biasing voltage. At higher LO-frequency IIP2 start decreasing, although the sensitivity of the IIP2 to the LO-frequency is not monotonic. The two-tone test signals were carried out at different frequencies. It should be noticed that as the bandwidth is wide two-tones should be selected somehow to make sure that the interaction of the fundamental tone with intermodulation tone places at the IF band. This ensures that true IIP2 is analyzed regarding to the bandwidth modulation and two-tone spacing.

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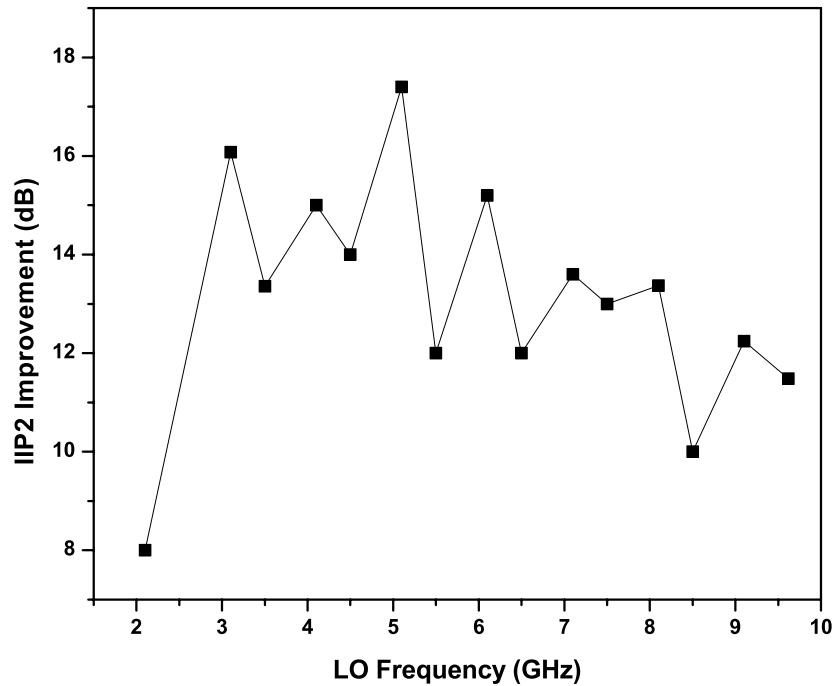
Figure 6.19: Sensitivity of the improved IIP2 versus LO frequency variations. This graph is an IIP2 difference between the conventional direct conversion and proposed mixers in Fig. 6.18.

6.7 Summary

As a result, a half-RF technique is employed in the design of a $3.1-8$ GHz receiver front-end. The single stage low power single-to-differential LNA eliminated the need for an off-chip balun and increases the integrity level of the front-end receiver. Using the proposed technique a good linearity and IIP2 was achieved from receiver front-end. The reduction in flicker noise helps to improve the lower frequency noise figure. A good LO-RF isolation restricts the leakage of the unwanted signals to the RF port, which reduces the second-order harmonic distortion.

Chapter 7

Conclusions and Future Works

Due to the demanding performance requirements for fourth-generation wireless systems, UWB systems are particularly attractive due to their low complexity, high data rate, low power consumption, and robustness to interferes. The most important characteristic of the UWB is the capability of operating in low power regime (transmit power of -41.3 dBm). For a UWB wireless network, the system can operate at very low signal to noise ratios with high bandwidth. This means that a UWB system is able to achieve high data rate with relatively low transmit power.

7.1   Future Work

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