An Energy-Aware CMOS Receiver Front end for Low-Power 2.4-GHz Applications

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***Abstract*—A receiver front end designed in 0.18-µm CMOS consisting of an LNA and IQ mixers is presented. The front end's power consumption is controllable from 5.0 mA down to 1.4 mA. It is proposed to push the receiver requirements to the front-end in order to efficiently control the overall power consumption based on the real-time required noise performance. We show that under good channel conditions, this front end can save up to 70% of its nominal power consumption.**

***Index Terms*—RF Front End, CMOS RF Integrated Circuits, Low Power, System on Chip.**

I. Introduction

THE last decade has seen the near complete integration of the wireless transceiver, and the rise of CMOS as the choice technology in consumer-based wireless applications such as mobile phones and wireless local area network (WLAN). Full system integration continues to be a topic of interest in the research field in order to minimize both the cost and the form-factor of wireless transceivers. However, a new trend is emerging in RFIC System on Chip (SoC) design.

In the interests of longer battery life, ultra-low power design has recently become a hot topic for applications such as wireless personal area networks (WPAN), and wireless sensor nodes. The IEEE 802.15.4 standard has been specifically designed to cater to this demand. Transceivers which follow this standard have been designed to operate using less than 10 mA of DC current [1]. These designs have relied on simplified circuit configurations to minimize power consumption [1]-[5].Despite their relative successes, we believe that significantly more power consumption can be saved both by further simplifying the circuit structures, and dynamically adjusting the performance of the receiver (RX). The latter method is termed energy-aware design and our proposed energy-aware scheme was introduced in [6].

While a radio is designed around its sensitivity, it normally operates under significantly better conditions. The average path loss varies depending on the environment, availability of line of sight (LOS) and distance between the RX and transmitter (TX), among other things [7]. An energy-aware transceiver adjusts its performance according to the amount of received signal strength and uses the optimum power to receive the signal in a given situation.

This work presents the implementation of an energy-aware RX front end for low power, low data-rate applications. We propose to dynamically control the power consumption of an RX front end based on the real-time required noise figure (NF). As a basis for comparison, we will design around the IEEE 802.15.4 standard which operates in the 2.4-GHz Industrial, Scientific and Medical (ISM) band. We focus on the design of the RX front end which generally consumes a large portion of the total RX power. The standard features relaxed requirements in terms of interference rejection, and noise performance which simplifies front end design and will allow us to implement dynamic power control circuitry.

Section II of this work will discuss energy-saving schemes and compare the proposed energy-aware scheme to state-of-the-art methods. Section III will discuss the distribution of power consumption in an RX and how much power can practically be saved. Section IV will present the receiver design methodology and details of the individual circuit blocks. Section V will present measured results and Section VI will conclude our work.

II. Energy-Saving Schemes

A. Proposed Energy Aware Design

The proposed energy-aware scheme involves adjusting the RX front end's power consumption based on its in-situ required NF. While the final design merit for an RX is its bit-error rate (BER), RFIC designers generally split the performance requirements up into nearly independent specifications. In general, signal non-idealities arise due to linear distortion [8], interference, and random noise.

An example of linear distortion is non-ideal filtering. In general, RF components such as the low-noise amplifier (LNA), and down-conversion mixer produce scarce linear distortion as they are generally designed to pass a much greater bandwidth than the signal bandwidth. For example, an 802.15.4 front end must pass the entire 83.5 MHz system bandwidth where the signal bandwidth is only 2 MHz [1].

The effect of interference on a signal's quality is described by the RX n^{th} order intercept (IIP_n), phase noise, image rejection

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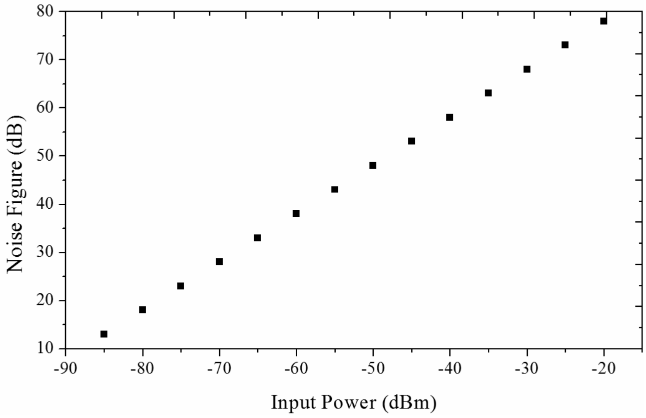

Fig. 1. Tolerable NF versus Received Input power for the IEEE 802.15.4 standard.

ratio (IRR), and 1-dB gain compression ($P_{1\text{-dB}}$). Such performance parameters are not suitable for energy-aware control for several reasons. Starting with linearity, we note that IIP_n and $P_{1\text{-dB}}$ are linked, and in principle the $P_{1\text{-dB}}$ is approximately 9.6 dB lower than the IIP_3 [9]. As the received signal strength increases, the required gain of the system drops. Reducing the system gain generally improves both its IIP_n and $P_{1\text{-dB}}$. However, the required IIP_n reduces making it impractical to control. Phase noise is a parameter of the frequency synthesizer whose power consumption is impractical to control without affecting the loop dynamics of the frequency synthesizer. Lastly, image rejection ratio (IRR), is determined by the matching between the I and Q paths and is not directly related to RX power consumption.

NF on the other hand is directly related to the RX power consumption. The input-referred noise of a MOSFET is approximately (only channel noise is considered),

$$V_{n,in}^2 \approx \frac{4kT\gamma\Delta f}{\alpha g_m} \tag{1}$$

where k is Boltzmann's constant, T is temperature in Kelvin, γ is a parameter approximately equal to 2/3 in saturation for long-channel devices, α is the ratio of g_m to the transconductance when the drain source voltage is zero, and g_m is the device transconductance [10]. Since g_m improves with current consumption,

$$g_m = \sqrt{2\mu_0 C_{ox} \frac{W}{L} I_{DS}} \tag{2}$$

where $\mu_0 C_{ox}$ is process dependent, W/L is the aspect ratio, and I_{DS} is the drain-source current, current consumption can be directly linked to NF. NF is also indirectly related to current consumption through the gain of a cascaded system. The cascaded NF can be calculated as,

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} \tag{3}$$

where F_{total} is the noise factor of the system, F_1 is the noise factor of the first stage, F_2 is the combined noise factor of all subsequent stages, and G_1 is the power gain (which is proportional to the square of the voltage gain) of the first stage. When F_1 is small compared to F_{total}, F_{total} is inversely proportional to the first stage's squared-gain. Assuming we have a common-source LNA representing G_1, its voltage gain is proportional to the square-root of the current consumption, and therefore, F_{total} is inversely proportional to the current consumption.

The tolerable system NF of an IEEE 802.15.4 RX is shown versus received signal strength in Fig. 1 and is based on system simulations in [11] which include the effects of a multipath environment. The bit-error-rate of the system is directly related to the received SNR and hence the system NF. In practice, we can also expect the curve to deviate slightly due to the finite output SNR of the transmitter.

Our discussion suggests that while an ideal energy-aware RX would be able to independently control its noise and interference performance, a sub-optimal design should be able to control its noise performance without degrading its interference performance.

B. An Alternate Energy-Aware Design

An energy-aware method involving control of a transceiver's power consumption based on the required error-vector magnitude (EVM) was proposed in [12]. The principle behind the choice of EVM as a performance measure is its strong correlation to BER. The authors proposed to control the EVM by controlling the biasing and power supply of the RF front end. However, in [12], no attempt to treat noise and interference independently was made. This method would therefore be suboptimal in situations where noise performance is good but interference performance is poor (or vice versa) since the EVM would reflect the poorer of the two performances. As discussed in the previous section, we advocate a two-dimensional approach to energy aware design. However, in this work we concentrate solely on adjusting the RX noise performance.

C. Variable Data Rate Standards

Certain standards such as the mobile WiMax [13] standard support multiple data rates. When channel conditions are good, the receiver can switch to a higher-data-rate modulation scheme and therefore, for the same amount of data, the transceiver is on for a shorter duration. Unfortunately, the channel conditions must be good both in terms of noise and interference simultaneously in order for the transceiver to communicate at higher data rates. The proposed energy-aware method does not suffer such limitations.

D. Other Energy-Saving Schemes

Two other interesting methods for saving power in RX design are the wake-up RX (WuRX) [14], [15] and energy harvesting

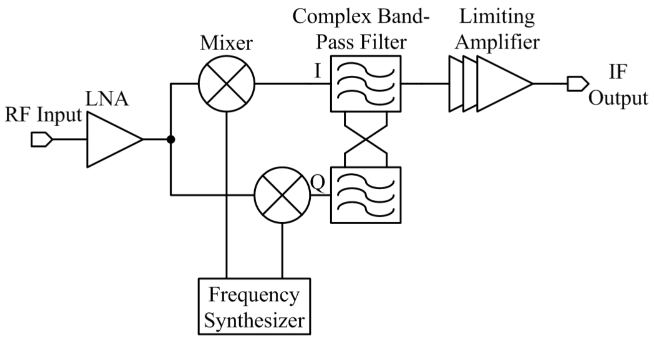

Fig. 2. Typical low-IF integrated receiver.

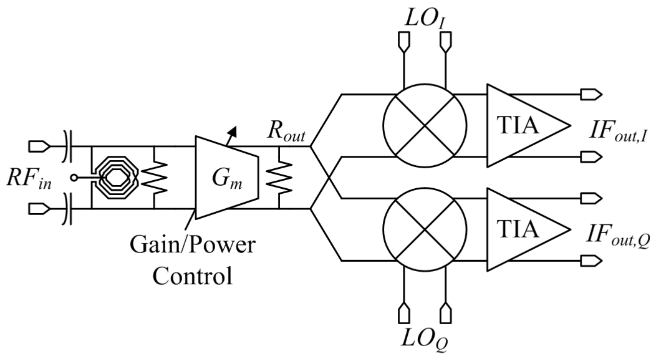

Fig. 3. Model of the proposed RF front end. The LO is supplied by an external signal generator.

[16]. Because a RX generally does not know when it will receive a signal, it is normally on. If the device only receives information for a small period of the time that it is on, then a lot of power is wasted. One method to get around this problem is to use a WuRX. The WuRX has been studied in [14] and [15] for use in wireless sensor nodes where the role of the WuRX is implied in its name. Another possible energy saving scheme is to use energy harvesting. An obvious energy harvesting scheme is to use solar cells to power the RX. However, it is potentially cost saving to harvest electromagnetic energy if an external battery can be avoided. This was used in [16] to power a demodulating circuit for wireless sensor nodes. Intuitively, both of these energy-saving schemes can be used in conjunction with energy-aware design.

It is well known that the gain requirement scales with input power and this fact was exploited in [17] to scale the power consumption of the receiver with the gain requirement. However, the additional link between NF and input power proposed here was not made. The authors in [17] also proposed ultra-low start-up time in order to minimize the total energy used by a receiver.

III. Practical Energy Aware Limitations

A typical low-IF integrated receiver is shown in Fig. 2. Energy-aware receiver design relies on a receiver's ability to regulate its power consumption based on the in-situ required specifications. However, any practical receiver design has overhead power requirements which can be considered fixed. For example, the power consumption of the frequency synthesizer has little correlation with the overall NF of the receiver. Although we can conceivably adjust the frequency synthesizer's output power based on the required NF, there is still a minimum power consumption required by such circuit blocks as the frequency dividers and phase-frequency detector. The goal of the receiver designer therefore should be to minimize the overhead power consumptions, and try to compensate for the degraded noise performance using blocks whose noise performance depends heavily on power consumption.

This leads to our proposed design methodology. By pushing the requirements of the receiver to the front-end LNA, we can increase the amount of controllable power consumption in the receiver. This obviously leads to a more energy-aware design. In order to push the requirements to the LNA, the LNA must be able to provide a high voltage gain. Furthermore, in order to compensate for the high LNA gain, all subsequent blocks up to and including the channel-select filter must exhibit high linearity. High linearity can be achieved in the down-conversion and channel filtering stages by using passive mixers and active-RC filtering [1].

The biggest limitation on the controllability of the receiver power consumption is in the power consumption required by the frequency synthesizer. In [1], and [18], the frequency synthesizer required 9.72 mW, and 12 mW, respectively, while in [19] it required just 2.4 mW. All frequency synthesizers were designed using CMOS for the IEEE 802.15.4 standard but [1] and [18] used 0.18 μm technology and [19] used 0.13 μm technology. Improving technology and frequency synthesizer architectures can therefore lead to very low power overhead for the frequency synthesizer.

Another required power overhead is due to the bandwidth requirements of the op-amps used in the channel filter. In order to prevent intermodulation of high frequency interferers, the channel filter must be linear over the entire system bandwidth which is 83.5 MHz in the case of the IEEE 802.15.4 standard [20]. This system bandwidth directly reflects on the bandwidth requirements of the op-amps.

Lastly there is some power overhead required by support blocks such as bandgap references and calibration circuitry.

IV. Front End Design and Analysis

A model of the proposed energy-aware front end is shown in Fig. 3. The LNA consists of a step-up impedance transformer followed by a variable gain/power transconductor. The transconductor is loaded by the output impedance of the LNA and the input impedance of the quadrature passive mixers. The quadrature passive mixers provide current-mode outputs to a pair of op-amp based transimpedance amplifiers (TIA).

The LO signal is split into I and Q phases using a two-stage poly-phase filter (PPF) which is not shown. The phase splitter reduces the signal swing of the LO which degrades the noise and conversion gain performance of the down-conversion mixer. Rather than buffer the LO, we chose to compensate for the reduced down-conversion mixer performance with a higher gain

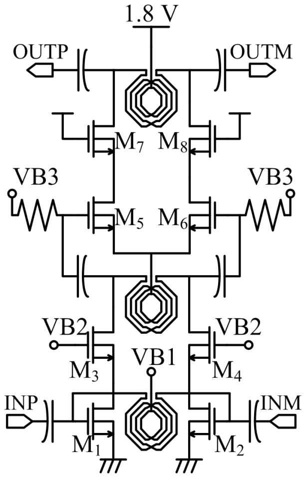

Fig. 4. The proposed Energy-Aware LNA with biasing shown. The biasing voltages are fed from current mirrors.

LNA. This leaves more room for gain control of the LNA.

A. Low-Noise Amplifier Design

As the performance requirements of the receiver were pushed back to the LNA, the LNA is by far the most critical block in this design. The LNA must achieve high gain and low power consumption while allowing variable power control. At the same time, the LNA should be matched to 50 Ω and the input impedance should be independent of the gain state.

We chose a two-stage design with current reuse in order to maximize the gain per power dissipation. Deep n-well transistors were used in order to tie the transistor bulk terminals to their respective sources. This was necessary to prevent an increase in the threshold voltage of the cascade transistors due to the body effect [21]. By keeping a low threshold voltage, the transit frequency (f_T) of the devices is maintained at a high value. All three inductors are 16.9 nH with a quality factor (Q) of 8.2 at the operating frequency. Additional resistors were added in parallel to the inductors (not shown in Fig. 3) in order to broaden the matching-bandwidth for the matching inductor, and the gain-bandwidth for the load inductors.

1) Input Matching

The input of the LNA was matched to a 50-Ω source using a high-pass LC matching network. Compared to a low-pass matching network [22], a high-pass matching network requires only a single inductor (versus two) which can make use of mutual coupling between the coils to boost the effective inductance resulting in considerably smaller die area usage. An additional 1-kΩ resistor (not shown in Fig. 3) was added in parallel with the input inductor in order to broaden the matching bandwidth. The overall Q of the matching network is therefore approximately 2.6. Note that we can consider the input impedance of M_1/M_2 as a capacitor with a quality factor of

$$Q_{Cgs} \approx \frac{5g_{d0}}{\omega_0 C_{gs}} \approx \frac{5\omega_T}{\alpha\omega_0} \tag{4}$$

where g_{d0} is the zero-VDS drain-source conductance, ω_0 is the operating frequency in radians per second, C_{gs} is the gate source capacitance of M_1/M_2 and α is a constant approximately equal to one. If, for example, ω_T/ω_0 is equal to 10 times, we can expect a quality factor of around 50 which is significantly higher than the quality factor of the matching inductor. Therefore to first-order, we can ignore the contributions of the series gate resistance to the input impedance.

The impedance transformation results in a voltage gain of,

$$G_1 = \sqrt{\frac{\omega_0 L Q_{L1}}{R_s}} \tag{5}$$

which is equal to 11.3 dB for this design. L is the inductance, Q_{L1} is the quality factor of the inductor including the additional parallel resistor, and R_s is the source resistance. From (4), we can see that in order to get a wide matching bandwidth and high gain, we need a large inductor, however, this is only true for the first order matching network used. Higher-order networks can offer high gain over a broader bandwidth while maintaining matched input impedance [23], [24].

As the power consumption of the LNA is changed with the gain state, the device capacitances of all transistors and most importantly, M_1 and M_2, are also changed. These changing device capacitances could potentially alter the frequency at which the LNA is matched to the 50- Ω source. We can reduce this effect by ensuring that the resonant frequency between the matching inductor and the device capacitances is significantly higher than the operating frequency (2.4 GHz). The same holds true for the two load inductors. Obviously this puts a restraint on the minimum f_T of the devices.

2) Voltage Gain

The LNA actually consists of three isolated gain stages with the last stage being a transconductance stage loaded by a finite Q inductor and the passive mixer. The first stage is due to the matching network described above. The second gain stage consists of a V-I conversion by M_1 and M_2, and an I-V conversion by the first load inductor. The output impedance of the cascode V-I converter consisting of M_1-M_4 is significantly higher than the parallel parasitic resistance of the first load inductor. As a result, the gain of the second stage can be closely approximated as,

$$G_2 = g_m \omega_0 L Q_{L2} \tag{6}$$

where g_m is the transconductance of M_1 and M_2, and Q_{L2} is the quality factor of the load inductor. The final stage of the LNA is loaded by the quadrature passive mixer and an inductor of the same inductance and Q as the previous stage. The biasing and device sizes are the same as the second stage resulting in the same g_m. Therefore, with G_{mix} as the input conductance of the passive mixer, the overall voltage gain is,

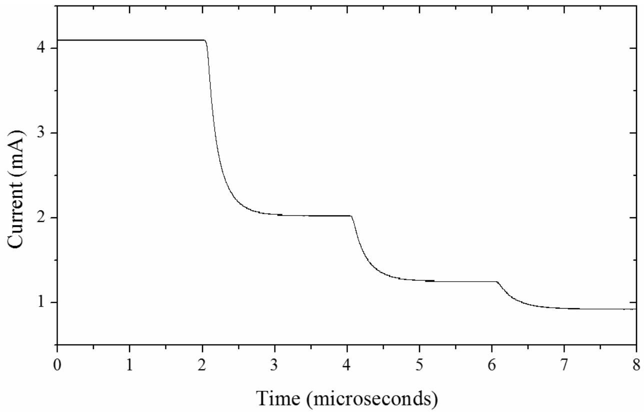

Fig. 5. Simulation of the settling time of the receiver. The receiver settles to the desired state within approximately 1 µs.

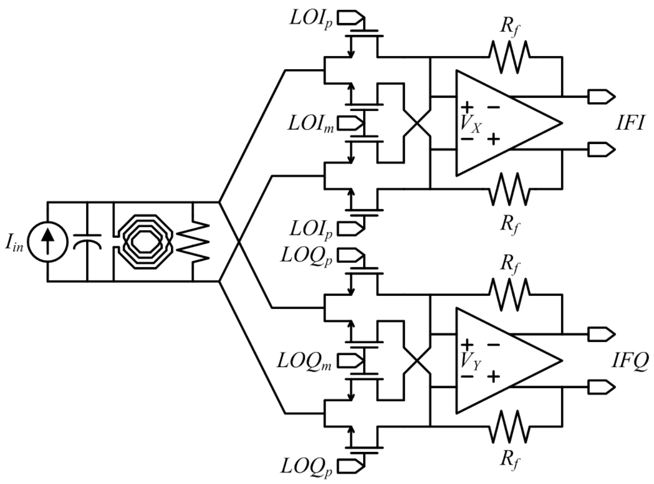

Fig. 6. A model of the LNA-mixer-TIA interface. A Norton equivalent circuit of the LNA is used with an R-L output impedance.

$$G_{LNA} = \frac{(g_m \omega_0 L Q_{L2})^2}{\omega_0 L Q_{L2} G_{mix} + 1} \sqrt{\frac{\omega_0 L Q_{L1}}{R_s}} \quad (7)$$

In order to achieve sufficient gain-bandwidth, Q_{L2} was reduced from 8.2 to approximately 3.4 using additional resistors parallel to the load inductors. Our expression, (7), shows that the LNA gain is proportional to g_m^2.

3) Noise Performance

Under matched conditions, the NF of an LC matching network is 3 dB. This sets the minimum NF of the LNA. However, with sufficient voltage gain in the matching network, the noise contributions of the rest of the circuit can be made small. Inductive degeneration [25] can be considered as an alternative to simple LC matching in order to optimize the noise performance, however, there are tradeoffs. Firstly, with inductive degeneration, the matching gain is still determined by the inductance. With the same total inductance (16.9 nH, for the same gain) and Q (8.2) factor, the series resistance of the inductance is 31.7 Ω. This is enough to achieve -13 dB return loss making the addition of a degeneration inductor pointless. In order to enjoy the low-noise benefits of inductive degeneration, the largest inductor would need to be implemented off-chip (bondwire perhaps). Secondly, inductive degeneration requires at least one additional inductor. Lastly, and perhaps most importantly, the input resistance offered by inductive degeneration is proportional to the transit frequency of the device [25]. As pointed out previously, an energy-aware LNA requires a changeable DC operating point. Changing the DC operating point affects the transit frequency of the devices and therefore indirectly changes the input resistance.

4) Switching Time

As changing the gain state of the receiver involves a change in the DC operating point, the receiver must be able to change state fast enough to meet requirements. The IEEE 802.15.4 standard specifies a 128 µs preamble [20] at the head of each data packet which can be used for the PLL and AGC to lock. An advantage of designing the gain control in the RF section is that RF circuitry is designed with short time constants. Therefore, the circuits can reach steady-state quickly. Fig. 5 illustrates the settling time of the receiver power consumption as the receiver goes from the highest gain state to the lowest gain state. The receiver requires approximately 1 µs for the current consumption to be within 1% of the steady-state value leaving ample time for the PLL to lock.

B. The Passive Mixer

Passive down-conversion was chosen over active down-conversion for the better flicker noise performance, linearity and power consumption. The tradeoff is lower input impedance and conversion gain, and poorer thermal noise performance. A double-balanced passive mixer is shown in Fig. 6. The passive mixer provides a current-mode output to an IF TIA. In a full RX design, the TIA can be replaced by an active-RC filter [1] using a similar op-amp.

Ignoring the frequency translation, to first order, the current-output passive mixer can be analyzed as a simple op-amp in shunt-shunt feedback. Although the performance will be somewhat different, we can use this simplification to make a few general statements about the features of the topology. Increasing the conductance of the switches lowers the input impedance, improves the conversion gain, and improves the noise performance. However, this also reduces the DC loop-gain and increases the loading to the VCO. At frequencies below the dominant pole frequency of the loop-gain, this degrades linearity (IIP_3 for example). Above the dominant pole frequency, the loop-gain is almost independent of the switch conductance. This is an important difference between direct-conversion and low-IF (MHz-range IF) receivers.

As previously pointed out, the frequency translation introduces an additional dimension to the analysis which reduces the accuracy of the simple feedback op-amp model. The next few subsections will discuss the differences in the context of conversion gain by looking at three main parts: the LNA-mixer interface, the mixer core, and the mixer-TIA interface. For the LNA-mixer interface, we are mainly concerned with the passive mixer's input impedance since (7) shows that it will affect the LNA voltage gain. For the passive

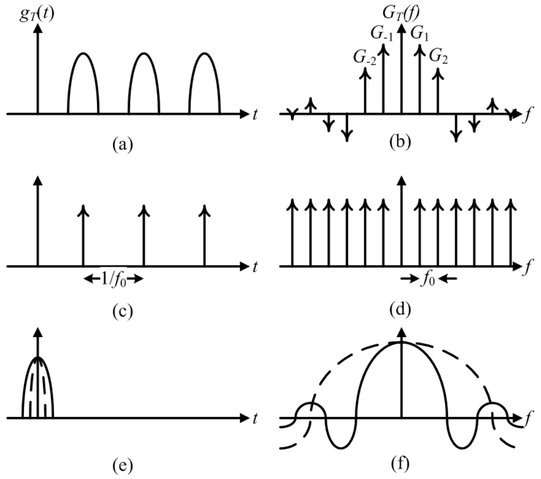

Fig. 7. Decomposition of $g_T(t)$ in the time and frequency domain. (a) $g_T(t)$ (b) $G_T(f)$ (c) pulse train in time (d) pulse train in frequency (e) the sampling function in time (f) the sampling function in frequency. (e) and (f) show the sampling function for two different sampling function widths.

mixer core, we will concentrate on the conversion gain from the switching transistors to the IF. For the mixer-TIA interface, we are mainly concerned with the output impedance which as mentioned, affects loop stability and linearity. We will set up our analyses by briefly discussing convolution matrices [26].

1) Convolution Matrices

A simple model for the time-varying conductance of a single switch (Fig. 6) in the ON state is,

$$g_{T1}(t) = K\left(V_{LO}\cos(\omega_{LO}t) + V_{DC} - V_T\right) \tag{8}$$

where K is a constant which depends on the switch sizes and the technology, V_{LO} is the LO signal swing, V_{DC} is the bias voltage across the gate and source of the switches, and V_T is the threshold voltage of the switches. In the OFF state, $g_{T1}(t) = 0$. As the LO is available in quadrature phases, we can define LOI_p by (8). For the switches driven by LOI_m, LOQ_p and LOQ_m, the cosine in (8) is replaced by negative cosine, positive sine and negative sine respectively. The conductance of these switches are $g_{T2}(t)$, $g_{T3}(t)$ and $g_{T4}(t)$. It should be noted that (8) assumes that the LO signal appearing at the sources of the switching transistors is negligible, which is true for typical biasing conditions. In practice, LO leakage to the mixer input is dependent on the output impedance of the LNA, and it can in turn change the conductance of the switching transistors. However, since we have assumed no leakage, the mixers operation is independent of the LNA output impedance.

From Fig. 7, we can see how $g_{T1}(t)$ to $g_{T4}(t)$ can be mapped into the frequency domain. $g_{T1}(t)$ is a convolution between an impulse train and a sampling function which in the frequency domain is represented by a multiplication between a frequency domain impulse train and a frequency domain sampling function. A mixer multiplies in the time domain, and hence the output in the frequency domain is a convolution of the input and $G_{T1}(f)$. $G_{T1}(f)$ only has values at discrete frequencies because we assumed that the LO is periodic. We can therefore write convolution matrices for $G_{T1}(f)$ to $G_{T4}(f)$ [26]. If only the first two harmonics are considered, then the result is,

$$\mathbf{G_{T1}(f)} = \begin{bmatrix} G_0 & G_{-1} & G_{-2} \\ G_1 & G_0 & G_{-1} \\ G_2 & G_1 & G_0 \end{bmatrix} \tag{9}$$

$$\mathbf{G_{T2}(f)} = \begin{bmatrix} G_0 & -G_{-1} & G_{-2} \\ -G_1 & G_0 & -G_{-1} \\ G_2 & -G_1 & G_0 \end{bmatrix} \tag{10}$$

$$\mathbf{G_{T3}(f)} = \begin{bmatrix} G_0 & -jG_{-1} & -G_{-2} \\ jG_1 & G_0 & -jG_{-1} \\ -G_2 & jG_1 & G_0 \end{bmatrix} \tag{11}$$

$$\mathbf{G_{T4}(f)} = \begin{bmatrix} G_0 & jG_{-1} & -G_{-2} \\ -jG_1 & G_0 & jG_{-1} \\ -G_2 & -jG_1 & G_0 \end{bmatrix} \tag{12}$$

where we have limited $\mathbf{G_{TN}(f)}$ to a three-by-three matrix for simplicity. Note how the G_{-1} in (9) and (10) is in-phase while it is out-of-phase in (11) and (12). This is a simplification since in a real MOSFET, the internal capacitances of the device result in both in-phase and out-of-phase components for each term in (9)-(12). The subscripts, n, for each entry correspond to $f_{RF} + nf_{LO}$. The convolution matrix components for $\mathbf{G_{T2}(f)}$ to $\mathbf{G_{T4}(f)}$ are given in terms of those calculated for $\mathbf{G_{T1}(f)}$. As an example of how to use the convolution matrices, assume we apply a small voltage, V_A which has a spectral component at f_{RF}, across a switch governed by (9). We can calculate the output components at the zero, positive and negative sidebands as,

$$\begin{bmatrix} I_{A,f_{RF}-f_{LO}} \\ I_{A,f_{RF}} \\ I_{A,f_{RF}+f_{LO}} \end{bmatrix} = \begin{bmatrix} G_0 & G_1 & G_2 \\ G_1 & G_0 & G_1 \\ G_2 & G_1 & G_0 \end{bmatrix} \begin{bmatrix} 0 \\ V_A \\ 0 \end{bmatrix} \tag{13}$$

This is obviously just a simple extension of Ohm's law. We can then use Kirchhoff's laws to analyze the entire mixer. The TIA's op-amp is assumed to be ideal at IF frequencies and hence the IF bandwidth is not apparent from our derivations. Let Y_{TIA} be the TIA input admittance, and V_{RF} the voltage across the mixer input terminals. Therefore, we can write,

$$\mathbf{V_X} = \left(\mathbf{G_{T1}} + \mathbf{G_{T2}} + \mathbf{Y_{TIA}}\right)^{-1}\left(\mathbf{G_{T1}} - \mathbf{G_{T2}}\right)\mathbf{V_{RF}} \tag{14}$$

$$\mathbf{V_Y} = \left(\mathbf{G_{T3}} + \mathbf{G_{T4}} + \mathbf{Y_{TIA}}\right)^{-1}\left(\mathbf{G_{T3}} - \mathbf{G_{T4}}\right)\mathbf{V_{RF}} \tag{15}$$

where $\mathbf{V_X}$ and $\mathbf{V_Y}$ are defined in Fig. 6. At high frequencies, the op-amp gain tends to zero, and we can approximate the TIA input admittance as R_f in parallel with some node capacitance,

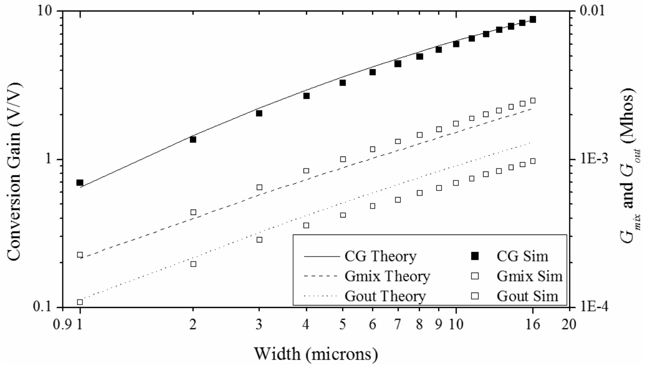

Fig. 8 Comparison between theoretically calculated and simulated conversion gain (CG in V/V), input conductance (G_{mix}) and output conductance (G_{out}). In simulation, the LO was 2.45 GHz, 250 mV_{pk} per phase.

C_X.

2) The LNA Mixer Interface

Based on the above discussion, we can derive the passive mixer's differential input conductance as,

$$G_{mix} \approx 2G_0 - \frac{4G_{-1}G_1R_f}{1+R_f\left(s_1C_X + 2G_0\right)} \tag{16}$$

where s_1 equals to $2\pi(f_{RF}+f_{LO})$. The first term, $2G_0$, can be seen by inspection. However, an additional term arises following our assumption that the TIA input impedance tends towards $R_f||C_X$ at high frequencies. From Fig. 6, the input signal is up-converted due to G_{T1} and forms a voltage at V_X. This high frequency signal then gets down-converted through G_{T2} which is out-of-phase of G_{T1} resulting in an overall negative input admittance term. Similar paths exist through G_{T3} and G_{T4}. If the op-amp bandwidth were infinite, this additional term would not arise.

The additional term in (16) is beneficial in that it increases the input impedance of the passive mixer, and it would seem that if R_f is large and s_1C_X is minimized, G_1 can be made equal to G_0, the input impedance would be infinite. The ratio G_1/G_0 is dependent on the peak to average conductance of the switches, and tends towards a value of one as the duty cycle of the switches is reduced [27]. The ratio of $2G_0$ to s_1C_X will depend on the technology used and the frequency of operation. Clearly for s_1C_X to be considered negligible, the technology's f_T would have to be at least an order of magnitude higher than the operation frequency. Taking into account the op-amp's input capacitance, s_1C_X was found to be significantly greater than $2G_0$ in our design.

3) The Mixer Core

As with our analysis of the input admittance, we can calculate the conversion gain of the passive mixer as,

$$\frac{V_{IFI}}{V_{RF}} \approx -2G_1R_f + \frac{4G_{-2}G_1R_f^2}{1+R_f\left(s_1C_X + 2G_0\right)} \tag{17}$$

$$\frac{V_{IFQ}}{V_{RF}} \approx 2jG_1R_f - \frac{4jG_{-2}G_1R_f^2}{1+R_f\left(s_1C_X + 2G_0\right)} \tag{18}$$

The term $-2G_1R_f$ can be seen on inspection due to the shunt-shunt feedback configuration. Needless to say, solving the problem using higher order matrices will lead to more complex solutions. Once again we note that s_1C_X is large and it therefore limits the influence of the term involving G_2.

4) The Mixer TIA Interface

The op-amp is conveniently designed as a two-stage amplifier where the first stage provides DC gain and the second stage is used to drive the output impedance. Assuming the second stage is a transconductance, G_{m2}, and the first stage provides DC gain, A_1, it is easy to see that the DC loop-gain of the TIA is A_1G_{m2}/G_{out}, where G_{out} is the output conductance of the passive mixer. Reducing G_{out} improves the loop-gain thereby improving the linearity of the TIA while also degrading its phase margin. The resonator at the output of the LNA can be approximated as having conductance G_{LNA} (equal to $(\omega_0LQL_2)^{-1}$) at f_{RF} and infinity at other frequencies. We can then calculate G_{out} as,

$$G_{out} \approx G_0 - \frac{G_1G_{-1}}{G_0 + G_{LNA} + \dfrac{G_{mix}}{2}} \tag{19}$$

We can see from (19) that the output impedance of the passive mixer depends not only on the conductance of the switches, but on the output impedance of the LNA. Note that C_X was assumed to be part of the TIA. The second term in (19) results from mixing up and then back down in frequency. The output impedance was calculated using three-by-three matrices rather than five-by-five due to the computational difficulty.

5) Accuracy of the Analysis

Equations (16), (17), and (19) and their simulated counterparts are plotted versus the switch width in microns (G_n were extracted from the simulation of a single MOSFET). They are plotted on a log scale to illustrate how the theoretical results can be fitter to the simulated data by adding a multiplicative factor. Ignoring the accuracy, the trend derived in the equations holds true in simulation. As mentioned earlier, a real MOSFET includes a distribution of capacitances and resistances which were not modeled by our simple model, and this is the biggest factor contributing to the equations inaccuracy.

6) Overall Implementation

Based on the preceding analyses, we can optimize the switch size, LO strength, and R_f. Increasing the LO voltage improves the conductance of the switches without greatly affecting the switches capacitance. Therefore, for minimum capacitive loading to the frequency synthesizer and LNA, we should maximize the LO voltage. We chose a 250 mV peak per LO phase as this value does not require excessive driving capability of the LO. For R_f, we note from the section above that R_f, to first order, does not affect the op-amp loop-gain. However, if the non-dominant pole is at the output of the op-amp, then a smaller R_f leads to higher op-amp unity-gain bandwidth. As a compromise between overall voltage gain ((17) and (18)), and bandwidth, we selected R_f as 4 kΩ. The simulation data in Fig. 9 illustrates the optimization of the switch width. When using

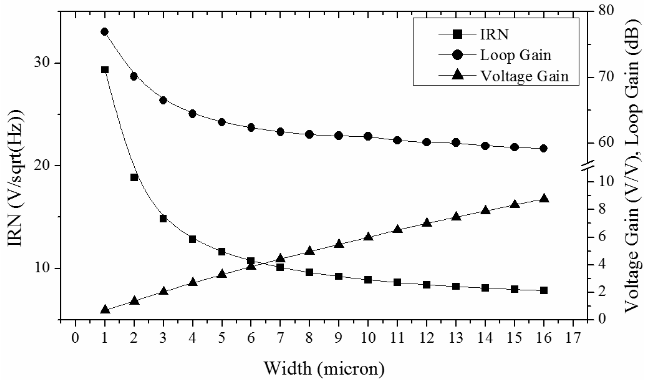

Fig. 9 Switch width optimization including input-referred noise (IRN), op-amp loop-gain, and voltage gain. The LO was 2.45 GHz, 250 mV_{pk} per phase.

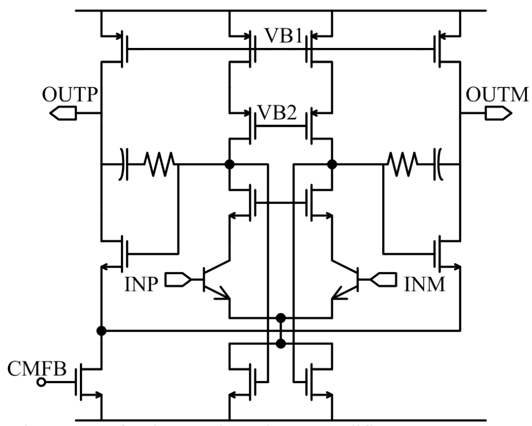

Fig. 10 The op-amp for the transimpedance amplifier

Fig. 9, we must take into account the increasing G_{mix} (Fig. 8) loads down the LNA thereby reducing the LNA voltage gain (this is evident from (7)). Therefore, there is an optimum width for minimum overall NF. For the LNA output impedance, of 880 Ω, this was found to be 4 µm, but because larger switch size is more forgiving in terms of process variation, we chose a switch width of 5 µm.

C. *The Transimpedance Amplifier*

The fully-differential op-amp is shown in Fig. 10. The input differential pair uses parasitic NPN transistors which provide better matching, DC-offset and flicker noise performance than MOS devices [28]. In a CMOS process, NPN bipolar junction transistors (BJT) are formed using the deep n-well, p-well and n-well layers. The current consumption of the op-amp is defined by PMOS current sources, and common-mode feedback (CMFB) is used in the output stage to set the input and output common-mode voltages to 1 V. This common-mode voltage propagates back to the input of the passive mixer. Miller compensation was used to set the phase margin to 60 degrees. The TIAs were designed to consume 100 µA each from the 1.8 V supply.

V. IMPLEMENTATION AND MEASUREMENT

The system described in Fig. 3 was implemented in a low-cost 6 metal 1 poly 0.18 µm RF CMOS process with a 2.5 µm top metal. Fig. 11 shows a micrograph of the fabricated design. The LO polyphase splitter was implemented on-chip as a two-stage RC polyphase splitter. This was done in order to reduce the pad count. Due to the limitation on the number of RF probes which could be used, the biasing circuitry was implemented using on-chip resistors. The drawback is that current consumption of the chip can deviate significantly from the designed value. We used a constant-g_m biasing circuit [21] for the LNA with a resistor which could be varied in three steps. This is an extremely simplistic method for gain tuning and in retrospect, a more robust method involving power detection should have been used. Such circuits are readily found for gain control in automatic gain-control (AGC) loops [1] and often involve decision making by the digital signal processor (DSP).

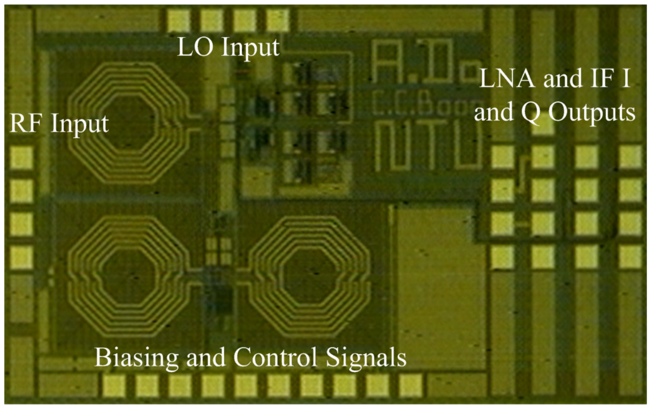

Fig. 11 A micrograph of the fabricated design.

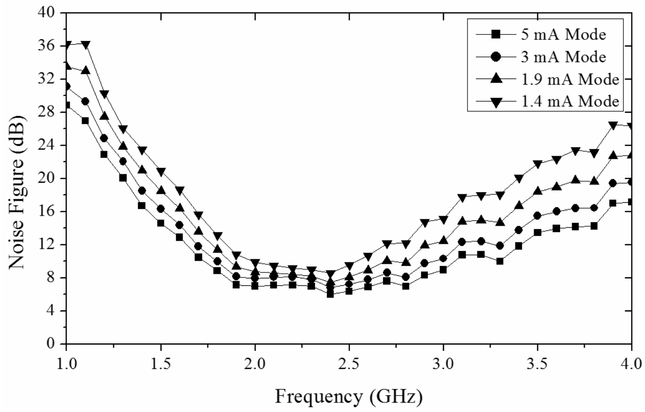

Fig. 12 NF of the LNA in all four gain modes.

A. *Measured LNA Performance*

The LNA was characterized for matching, noise, gain and linearity performance. The NF in all four gain modes is shown in Fig. 12. The LNA achieves a 6 dB NF in the 5 mA mode. The input reflection coefficient and gain are shown in Fig. 13. From Fig. 13, the LNA matching frequency shifted down to 2.25 GHz. However, the two other resonating nodes in the LNA did not experience the same frequency shift. As a result, the voltage gain frequency response is somewhat distorted. The result was a decreased center frequency gain, and a corresponding increase in the minimum NF. The IIP_3 was measured to be -11.5 dBm in

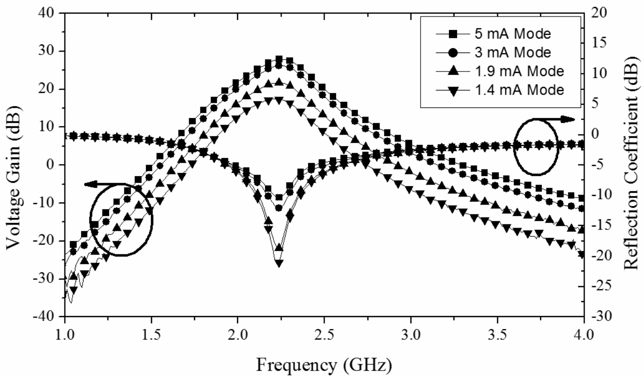

Fig. 13 Voltage gain and input reflection coefficient of the LNA in all four gain modes.

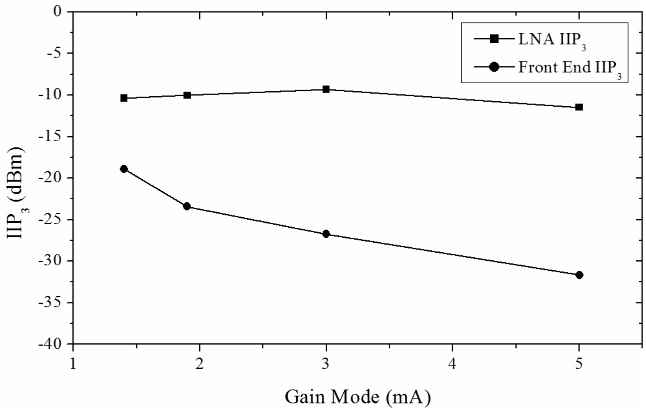

Fig. 14 Measured IIP$_3$ (dBm) versus gain mode (mA) for the LNA only and the full front end.

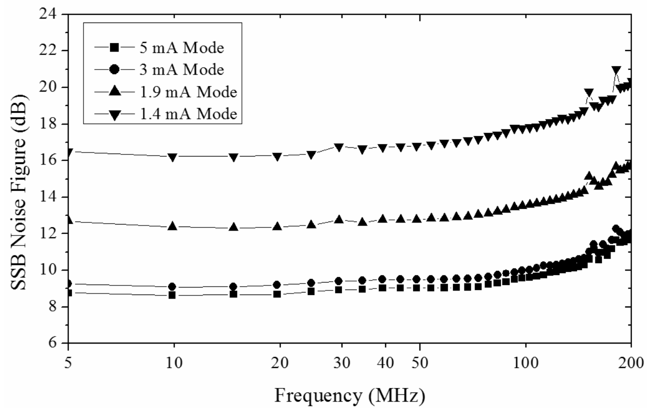

Fig. 15 SSB NF of the front end in all four gain modes. LO was fixed at 2.31 GHz, 0 dBm.

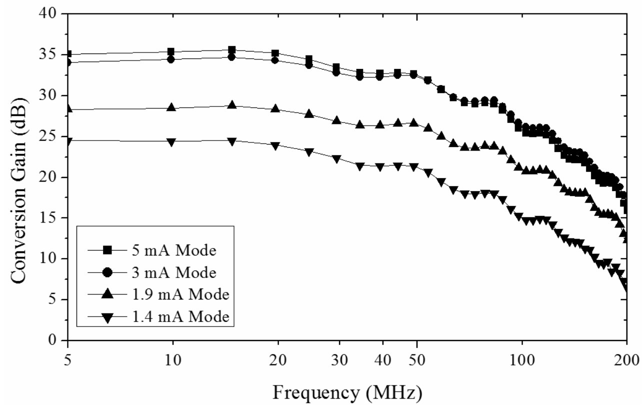

Fig. 16 Conversion gain of the front end in all four gain modes. LO was fixed at 2.31 GHz, 0 dBm.

the highest gain mode and showed slight improvement (1 dB) in lower gain modes. This is shown in Fig. 14. Although the gain drops in lower gain modes, the bias point changes somewhat offsetting the improvement in IIP$_3$.

The LNA was designed for a gain step of 6 dB. However, as previously mentioned, the biasing network was designed using on-chip resistors due to a limitation on the number of probes. Unfortunately, the measured bias current deviated significantly (around 25 % in 5 mA mode) from the nominal value resulting in a change in the gain step. Future iterations of this work will use a more accurate gain-step.

B. Measured Front End Performance

The front end was characterized for noise, gain, linearity and power consumption performance. The noise figure and conversion gain of the front end were measured using the Agilent E4407B spectrum analyzer which has a built in noise figure personality. Unfortunately, neither the spectrum analyzer nor our noise source were designed to be used below 10 MHz. The current consumption in the highest to lowest power modes are 5.01 mA, 2.97 mA, 1.88 mA, and 1.39 mA respectively with a 1.8 V supply. From Fig. 15, the front-end single-sideband (SSB) NF is around 9 dB (approximately 6 dB double sideband (DSB) NF) in the highest gain mode and increases with the reduced LNA gain. The front end gain, as seen in Fig. 16, agrees with the LNA gain. The IIP$_3$ for the front end is -31 dBm in the highest gain mode and improves with lower LNA gain. This is shown in Fig. 14.This was sufficient for our application but can be improved by increasing the loop-gain of the op-amps. The front end gain of 35 dB in the highest gain mode is sufficient such that the noise performance of the subsequent blocks can be made insignificant without requiring high power consumption. Table I shows a comparison between the proposed design and current literature. The NF quoted in this work is SSB NF while that in [22] is DSB NF. [1] and [29] use image-reject mixers which are able to suppress the noise in the image band, however, The work in [29] uses two IFs and it is not clear how well the first image noise is suppressed. The authors of [22] used high Q input matching and active mixing to achieve excellent NF for its current consumption. This came at the cost of a low IIP$_3$ and possibly high flicker noise corner frequency. It should be noted that the key point in [29] was the innovative use of a digital demodulator which allowed the authors to achieve a low overall power consumption and good performance.

VI. Conclusion

Communication between a mobile device and a fixed hub allows for energy-aware design of the mobile RX and TX where the mobile TX's output power is optimized and the mobile RX's sensitivity is optimized. This work has discussed the design and implementation of an energy-aware RX involving optimization based on several different input conditions rather than the

TABLE I
COMPARISON TO PRIOR PUBLISHED WORK

Reference	This Work				[1]	[22]	[29]
Frequency (GHz)	2.3				2.4	2.5	2.4
Current (mA)	5	3	1.9	1.4	5.6[A]	1.16	2.39
Noise Figure (dB)	8.8[B]	9.3[B]	12.7[B]	16.5[B]	5.7	5	12
IIP3 (dBm)	-31	-27	-23	-19	-16	-37	-
Voltage Gain (dB)	35.6	34.7	28.7	24.5	33[C]	43	-
Technology (µm)	0.18				0.18	0.18	0.18

[A] Entire analog front-end included
[B] SSB NF which is approximately 3 dB higher than DSB NF
[C] Only LNA gain included

minimum sensitivity. A design methodology which simplifies the RX design was presented which involves pushing NF requirements to the front end while only maintaining sufficient bandwidth for proper filtering in the IF section. This allows greater control of the front end power consumption. Following circuit analysis of the front end blocks, measurement results of the proposed front end were presented. The front end power consumption exhibited up to 72 % reduction in power consumption with high input power.

APPENDIX

For a sinusoidal LO, G_0 and G_1 were calculated to be equal to

$$G_1 = \frac{V_{LO}}{2\pi}\cos^{-1}\left(\frac{V_T - V_{DC}}{V_{LO}}\right) + \frac{(V_{DC} - V_T)}{\pi} \cdot \sin\cos^{-1}\left(\frac{V_T - V_{DC}}{V_{LO}}\right) + \frac{V_{LO}}{4\pi}\sin 2\cos^{-1}\left(\frac{V_T - V_{DC}}{V_{LO}}\right) \tag{20}$$

$$G_0 = \frac{V_{DC} - V_T}{\pi}\cos^{-1}\left(\frac{V_T - V_{DC}}{V_{LO}}\right) + \frac{V_{LO}}{\pi}\sin\cos^{-1}\left(\frac{V_T - V_{DC}}{V_{LO}}\right). \tag{21}$$

From (20) and (21), if we were to bias the voltage-output passive mixer at the threshold voltage of the transistor (i.e. $V_{DC} = V_T$), the ratio G_1/G_0 would equal to $\pi/4$ which is -2.1 dB. This agrees with the analysis in [27].

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REFERENCES

[1] W. Kluge, F. Poegel, H. Roller, M. Lange, T. Ferchland, L. Dathe, D. Eggert, "A Fully Integrated 2.4-GHz IEEE 802.15.4-Compliant Transceiver for ZigBee™ Applications", *IEEE Journal of Solid-State Circuits*, vol. 41, issue 12, pp. 2767-2775, Dec, 2006.

[2] I. Nam, K. Choi, J. Lee, H. –K. Cha, B. –I. Seo, K. Kwon, K. Lee, "A 2.4-GHz Low-Power Low-IF Receiver and Direct-Conversion Transmitter in 0.18-µm CMOS for IEEE 802.15.4 WPAN Applications", *IEEE Transactions on Microwave Theory and Techniques*, Vo. 55, No. 4, pp. 682- 689, April, 2007

[3] T –K. Nguyen, N –J. Oh, V.–H. Hoang, S. –G. Lee, "A Low-Power CMOS Direct Conversion Receiver With 3-dB NF and 30-kHz Flicker Noise Corner for 915-MHz Band IEEE 802.15.4 ZigBee standard", *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 2, pp. 735-741, Feb, 2006,

[4] T.-K. Nguyen, V. Krizhanovskii, J. Lee, S. –K. Han, S. –G. Lee, N. –S. Kim, C. –S. Pyo, "A Low-Power RF Direct-Conversion Receiver/Transmitter for 2.4-GHz-Band IEEE 802.15.4 Standard in 0.18-µm CMOS Technology", *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, issue 12, pp. 4062-4071, Dec, 2006.

[5] M. Camus, B. Butaye, L. Garcia, M. Sié, B. Pellat, T. Parra, "A 5.4 mW/0.07 mm2 2.4 GHz Front end Receiver in 90 nm CMOS for IEEE 802.15.4 WPAN Standard", *IEEE Journal of Solid-State Circuits*, vol. 43, no. 6, pp. 1372-1383, June 2008.

[6] A. V. Do, C. C. Boon, M. A. Do, K. S. Yeo, A. Cabuk, "An Energy Aware CMOS Front End for 2.4-GHz ISM Band Low Power Applications", *IFIP/IEEE International Conference on Very Large Scale Integration*, Oct 2008

[7] T. S. Rappaport, "Mobile Radio Propagation: Large-Scale Path Loss", *Wireless Communications Principles and Practice*, Second Edition, Upper Saddle River, NJ/USA: Prentice Hall PTR, 2002, Chapter 4, pp. 105-176.

[8] W. Sansen, "Distortion in Elementary Transistor Circuits", *IEEE Transactions on Circuits and Systems – II: Analog and Digital Signal Processing*, vol. 46, no. 3, March 1999, pp. 315-325.

[9] B. Razavi, "Basic Concepts in RF Design", *RF Microelectronics*, Upper Saddle River, NJ/USA: Prentice Hall PTR, 1998, Chapter 2, Section 2.1.1, pp. 22.

[10] T. H. Lee, "Noise", *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd Ed., Cambridge, UK: Cambridge University Press, 2004, Chapter 11, pp. 339.

[11] P. Gorday, "802.15.4 Multipath", Internet: https://mentor.ieee.org/802.15/file/04/15-04-0337-00-004b-802-15-4-multipath.ppt, July 2004 [Oct. 2009].

[12] R. Senguttuvan, S. Sen, A. Chatterjee, "Multidimensional Adaptive Power Management for Low-Power Operation of Wireless Devices", *IEEE Transactions on Circuits and Systems – II: Express Briefs*, vol. 55, no. 9, Sept 2008, pp. 867-871.

[13] S. Lloyd, "Challenges of Mobile WiMAX RF Transceivers", *International Conference on Solid-State and Integrated Circuit Technology*, Oct. 2006, pp. 1821-1824.

[14] N. Pletcher, S. Gambini, J. Rabaey, "A 65uW, 1.9 GHz RF to Digital Baseband Wakeup Receiver for Wireless Sensor Nodes", Custom Integrated Circuits Conference (CICC) September 16-19, 2007, San Jose, CA.

[15] N. Pletcher, S. Gambini, J. Rabaey, "A 2GHz 52pW Wake-Up Receiver with -72dBm Sensitivity Using Uncertain-IF Architecture", *IEEE International Solid-State Circuits Conference*, Feb. 2008, pp. 523-525

[16] T.S. Salter, Bo Yang; N. Goldsman, "Low power receiver design utilizing weak inversion and RF energy harvesting for demodulation", *International Semiconductor Device Research Symposium*, Dec 2007, pp. 1-2.

[17] D. Daly, A. P. Chandrakasan, "An energy-efficient OOK transceiver for wireless sensor networks", *IEEE Journal of Solid-State Circuits*, vol. 42, no. 5, May 2007, pp. 1003-1011.

[18] P. Choi et al., "An Experimental Coin-Sized Radio for Extremely Low-Power WPAN (IEEE 802.15.4) Application at 2.4 GHz", *IEEE Journal of Solid-State Circuits*, vol. 38, no. 12, Dec 2003, pp. 2258-2268.

[19] C. Bernier, F. Hameau, G. Billiot, E. de Foucauld, S. Robinet, J. Durupt, F. Dehmas, E. Mercier, P. Vincent, L. Ouvry, D. Lattard, M. Gary, C. Bour, J. Prouvee, S. Dumas, "An ultra low power 130nm CMOS direct conversion transceiver for IEEE802.15.4", *IEEE Radio Frequency Integrated Circuits Symposium*, April & June 2008, pp. 273-276.

[20] IEEE 802.15.4 Standard For Local and Metropolitan Area Networks, 2003.
[21] B. Razavi, "Basic MOS Device Physics", "Bandgap References", *Design of Analog CMOS Integrated Circuits*, International Edition, Singapore: McGraw-Hill, 2001, Chapters 2 and 11, Section 2.3 and 11.2, pp. 23-24 and 379.
[22] B. G. Perumana, R. Mukhopadhyay, S. Chakraborty, C.-H. Lee, and J. Laskar, "A low-power fully monolithic subthreshold CMOS receiver with integrated LO generation for 2.4 GHz wireless PAN applications," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2229–2238, Oct. 2008.
[23] C. Bowick, "Impedance Matching", *RF Circuit Design*, First Edition, Indianapolis, Indiana, Howard W. Sams & Co., Inc, 1982, Chapter 4, pp. 72-75.
[24] A. Ismail, A. A. Abidi, "A 3-10 GHz Low-Noise Amplifier with Wideband LC-Ladder Matching Network", *IEEE Journal of Solid-State Circuits*, Vol. 39, No. 12, pp. 2269-2277, Dec 2004.
[25] D. K. Shaeffer, T. H. Lee, "A 1.5-V, 1.5-GHz CMOS Low-Noise Amplifier", *IEEE Journal of Solid-State Circuits*, Vol. 32, No. 5, pp. 745-759, May 1997,
[26] S. A. Mass, "Harmonic Balance Analysis and Related Methods", *Nonlinear Microwave and RF Circuits*, 2nd Ed., Artech House, 685 Canton Street Norwood, MA 02062, 2003, Chapter 3, pp. 164-197.
[27] A. R. Shahani, D. K. Shaeffer, T. H. Lee, "A 12-mW Wide Dynamic Range CMOS Front end for a Portable GPS Receiver", *IEEE Journal of Solid-State Circuits*, vol. 32, no. 12, pp. 2061-2070, Dec. 1997.
[28] I. Nam, K. Lee, "High Performance RF Mixer and Operational Amplifier BiCMOS Circuits Using Parasitic Vertical Bipolar Transistors in CMOS Technology", *IEEE Journal of Solid-State Circuits*, Vol. 40, No. 2, pp. 392-402, Feb 2005.
[29] C. –P. Chen, M. –J. Yang, H. –H. Huang, T. –Y. Chiang, J. –L. Chen, M. –C. Chen, K. –A. Wen, "A Low-Power 2.4-GHz CMOS GFSK Transceiver With a Digital Demodulator Using Time-to-Digital Conversion", *IEEE Transactions on Circuits and Systems – I: Regular Papers*, Vol. 56, No. 12, Dec 2009, pp. 2738-2748.

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