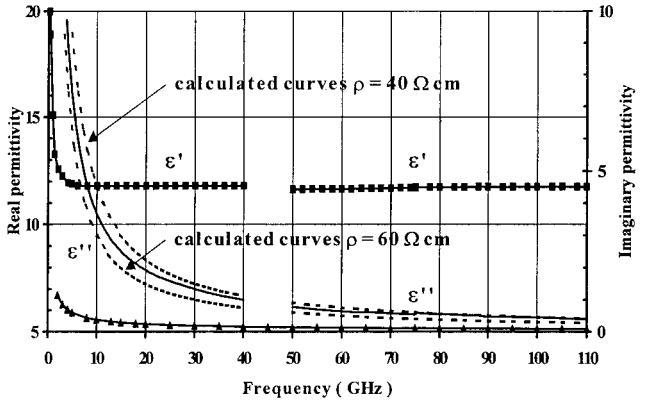

Figure 4 Measured ε_r data for doped silicon in the 0.05–110 GHz frequency range (cell dimension: $t = 3$ μm, $W = 70$ μm, $W+2S = 170$ μm, $h = 230$ μm, length $d = 1$ cm). ■ measured ε_r' values ($\mu_r = 1 - j0$ fixed in the processing method), ___ measured ε_r' values ($\mu_r = 1 - j0$ fixed in the processing method), - - - - - calculated ε_r'' values ($40\ \Omega\ \text{cm} < \rho < 60\ \Omega$ cm). ▲ calculated ε_r'' values for the metallic losses ($\varepsilon_r = 11.7 - j0$ with the above same cell dimension) and repeatability errors (±0.2 dB covering 2–110 GHz)

silicon is 0.4. The error on ε_r'' increases versus frequency and is maximum at 110 GHz (<21.5%). However, as can be seen in Figure 4, the ε_r'' values measured for doped silicon (solid lines) are in good agreement with the manufacturer data, since they are included into the uncertainty domain given by the manufacturer (dotted lines – $\rho = 40$–$60\ \Omega$ cm).

4. CONCLUSION

A very high broadband characterization method of isotropic film-shaped materials was developed. It uses a coplanar line as cell, which does not present air gaps between the conductors and the sample as with the box-shaped cells. Moreover, the coplanar characteristic impedance can be optimized in order to propagate the quasi-TEM dominant mode, on which the extraction method of the substrate properties is based. The complex properties (ε_r, (μ_r) are easily computed from a fast processing method of the coplanar *S*-parameter measurements using analytical relationships. The sample losses can be conveniently measured when they are higher than the coplanar cell conductive losses and the repeatability errors of the test fixture. The experimental results have shown the validity of this method for dielectric materials in the 0.05–110 GHz frequency range.

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NEW SPUR REDUCTION FRACTIONAL-N FREQUENCY DIVIDER

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ABSTRACT: *A spur reduction technique for fractional-N frequency synthesis is proposed. This technique can fully suppress the fractional spurs. Furthermore, it provides a simple solution to spur reduction and requires only two 2-to-1 multiplexers added to the conventional fractional-N frequency divider.* © 2002 Wiley Periodicals, Inc. Microwave Opt Technol Lett 33: 355–358, 2002; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.10320

Key words: *fractional-N; spur; frequency divider*

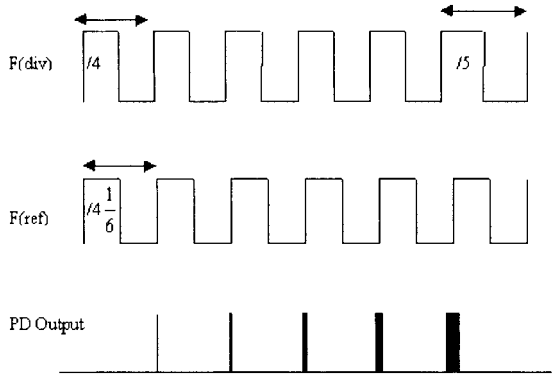

Figure 1 Effect of unequal instantaneous frequencies in a fractional-N synthesizer

1. INTRODUCTION

For frequency synthesis in the GHz range, a fractional-N divider allows PLL Synthesizers to have a frequency resolution finer than the reference frequency. This technique originates from an early digiphase synthesizer [1], which was subsequently referred to as the fractional-N frequency divider [2]. Unfortunately, this technique generates unwanted low-frequency spurs due to the fixed pattern of the dual-modulus divider [3]. These low-frequency spurs are in addition to the reference spurs [4]. Since these spurs can reside inside the loop bandwidth, fractional-N frequency synthesizers are not practical unless fixed inband spurs are suppressed to a negligible level. In a fractional-N frequency divider, a dual-modulus divider, divide-by-(N/N+1), is used. The fractional division is obtained by periodically changing the division value. To achieve a divide-by-$4\frac{1}{6}$ operation, five divide-by-4 operations and one divide-by-5 operation are required. As shown in Figure 1, each of the first five cycles of the divided signal is slightly shorter than the reference period. Consequently, the phase difference between the reference and the feedback signal grows in every period of F(ref), until it returns to zero when the divide-by-5 operation occurs. Thus, the phase detector produces progressively wider pulses, creating a ramp waveform at the output of the loop filter.

Here, we can conclude that if the VCO output frequency is to be equal to $(N+\alpha)F(ref)$, (e.g., $\alpha = \frac{1}{6}$ and $N = 4$ in Fig. 1), then the output of the LPF will be a repetitive ramp waveform with a period $1/(\alpha F(ref))$. If the loop was closed, such a waveform would modulate the VCO, creating sidebands at $\alpha F(ref)$, $2\alpha F(ref)$, etc., with respect to the center frequency. Such sidebands are called fractional spurs. To reduce the fractional spurs, various techniques have been proposed [5–10]. Table 1 summarizes the main features and the associated problems.

2. CIRCUIT DESCRIPTION

Compared to the existing spur reduction techniques, this new spur reduction technique can fully suppress the fractional spurs and does not generate unwanted noise or jitter. The proposed circuit needed only two multiplexers added to the conventional fractional-N divider.

TABLE 1 Fractional-N Techniques

Technique	Feature	Problem
DAC Phase Estimation [5]	Cancels spur by DAC	Analog mismatch
Random jittering [6]	Randomizes divider	Frequency jitter
Δ-Σ modulation [7, 8]	Modulates divider ratio	Quantization noise
Phase interpolation [9]	Inherent fractional divider	Interpolation jitter
Pulse generation [10]	Inserts pulses	Interpolation jitter

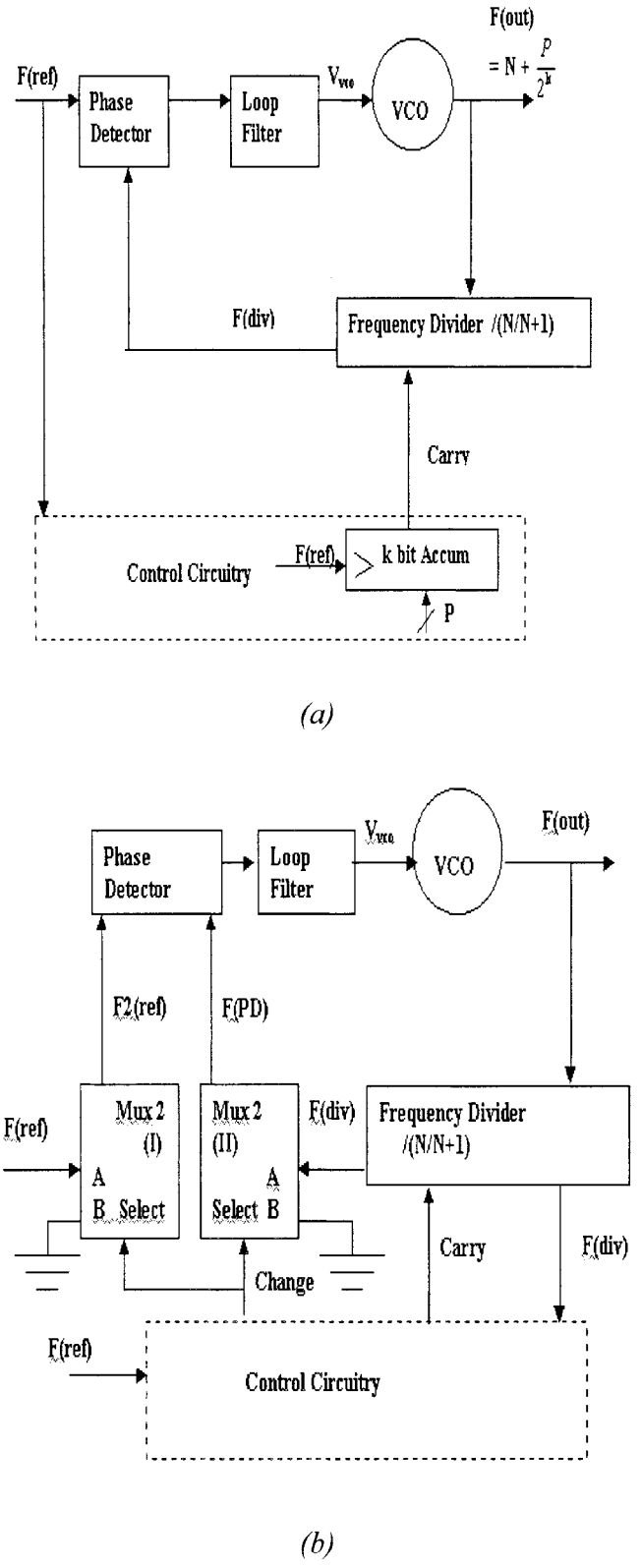

Figure 2 (a): A conventional fractional-N frequency divider. (b): The proposed fractional-N spurs reduction frequency divider

Figure 2 shows the basic architecture of (a) the conventional fractional-N frequency divider and (b) the proposed spur reduction

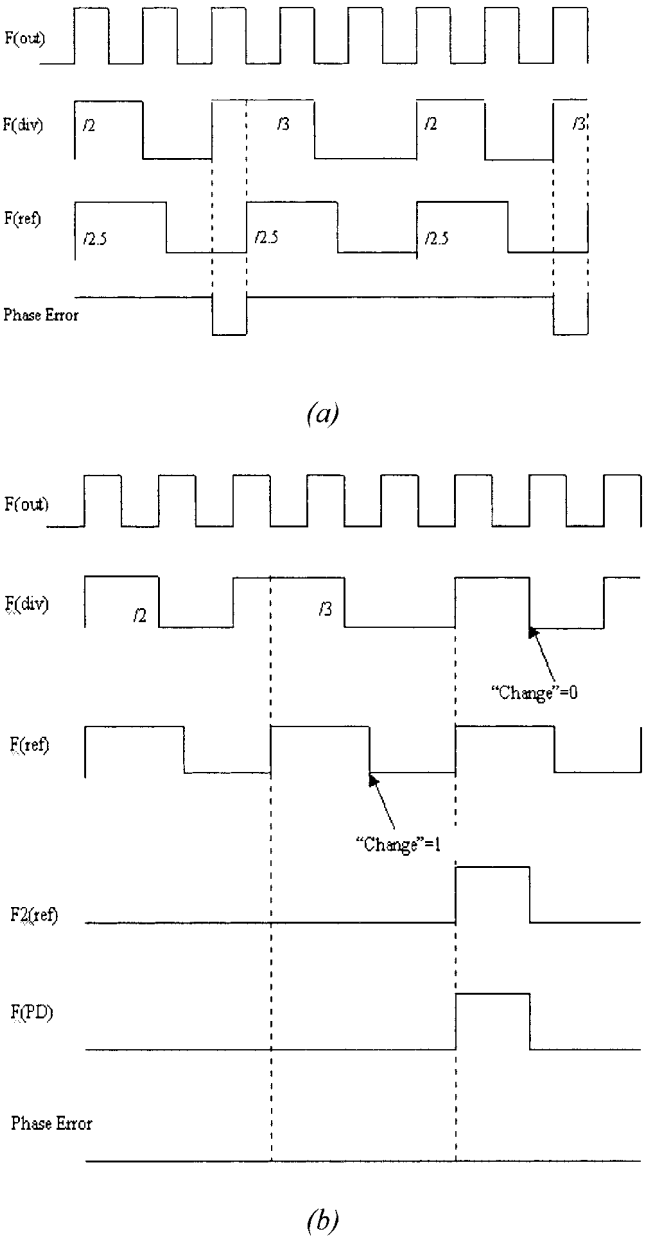

Figure 3 Phase error to achieve divide-by-21/2 (a) without spur reduction, (b) with spur reduction technique

frequency divider. A 2-to-1 multiplexer is used to select between f(ref) and Gnd, while the other multiplexer selects between *f*(div) and Gnd. When Change is "0" both the outputs of the multiplexers are grounded. When Change is "1," F(ref) and F(div) will be selected by each of the multiplexers. The multiplexer is implemented using pass transistor. For a fractional-N divider, in order to achieve a division by N + s/q, where s and q are integers, (q-s) divide-by-N cycles and s divide-by-N+1 cycles need to be performed. The basic technique is to compare the phase of F(ref) and F(div) only at the end of every q cycles. To implement this, the signal "Change" will be set to "1" by the control circuitry precisely after the accumulation of q falling edges of f(ref), and subsequently at every $(r \times q)^{th}$ falling edge of f(ref), where r is an integer. "Change" will be set to "0" at the first falling edge of f(div), and subsequently at every $(r \times q + 1)^{th}$ falling edge of F(div). For example, if a division of 9 + 1/20 is required, where N = 9, s = 1, and q = 20, at the 20, 40, 60…, and every multiple

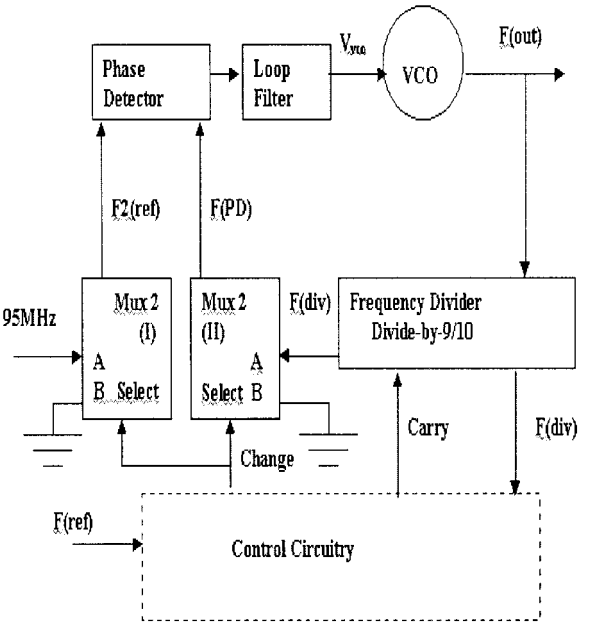

Figure 4 Block diagram for the simulation of the new fractional-N technique

of 20 falling edges of F(ref), Change will be set to "1." While in the 1, 21, 41, 61…, and every multiple of (20 × r + 1) of falling edge of F(div), Change will be set to "0."

The signal Carry controls the modulus of the frequency divider. When Carry is "1," a division by N+1 is performed, while a division by N is performed when Carry is "0." If Change is initially "0," F2(ref) and F(PD) are both grounded, which gives the phase detector a zero output. In order to achieve a divide-by-N+$\frac{2}{5}$, two division by N+1 cycles are done after every three division by N cycles. So the carry of the accumulator is the sequence of {0001100011…}, where division by N+1 corresponds to a "1."

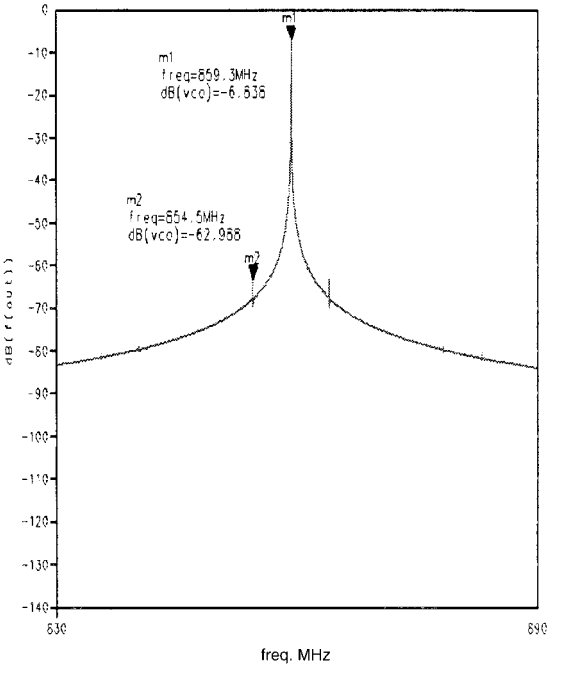

Figure 5 Simulation results of a conventional fractional-N PLL

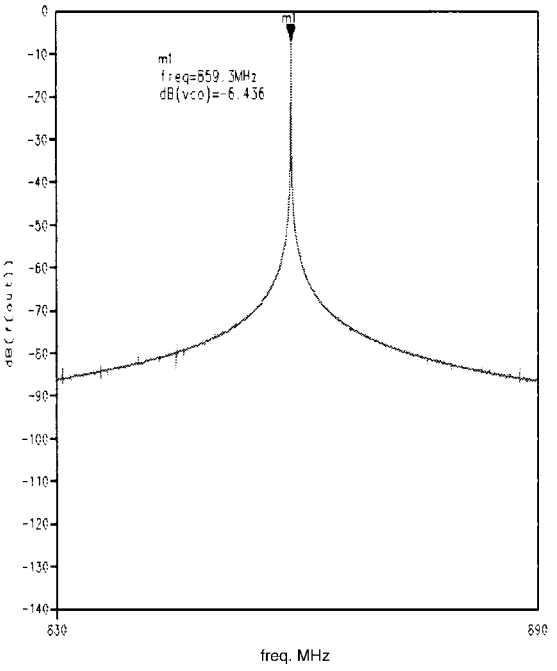

Figure 6 Simulation results of the new fractional-N PLL with spur reduction circuit implemented

Hence, when the carry of the accumulator is the sequence of {0001100011…}, then "Change" will have the sequence of {0000100001…}.

Figure 3 shows that the phase error in (a) has now been eliminated by the proposed spur reduction technique in (b). This is because at the transient period of the new fractional-N divider, there is no comparison done between F(ref) and F(div), thus minimizing the phase error. Only at the last pulse of F(ref) is compared to F(div).

3. SIMULATION RESULTS

A closed-loop simulation was carried out to evaluate the performance of the spur reduction technique. The setup of the simulation is shown in Figure 4. The output tuning range is centered at 855 MHz. Here, a division of 9 + 1/20 is to be achieved. In order to achieve fast settling time, the signal Change is set to "1" for the initial 105 μsec, thus disabling the function of the multiplexers for that period of time. Hence, it is at the steady state that both multiplexers are operational. Consequently, the settling time of the phase-lock loop will not be affected by the introduction of the extra circuitry.

Figure 5 shows the simulation results of conventional PLL, while Figure 6 is the simulation results of the PLL with the spur reduction technique implemented. Fractional spur is shown as a sideband in Figure 5, while in Figure 6 all fractional spurs are eliminated. The effect of reference spurs which is caused by the mismatch of phase detector is not taken into account in the simulation, as it is considerably smaller in magnitude compared to the effect of fractional spurs.

4. CONCLUSION

A new spur reduction frequency divider is proposed. The advantage of this technique, besides its ability to totally eliminate all fractional spurs, is its simplicity, requiring only an extra 2-to-1 multiplexer. The simulation is done using 0.25-micron chartered semiconductor technology, and simulated using the HP Advanced Design System.

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ESTIMATION OF THE RADIATION PATTERNS OF DIVERGING/FOCUSING TYPE OF LEAKYWAVE ANTENNAS

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ABSTRACT: *In this article, an extension of "field regions" to estimate simply and qualitatively the feature of the radiation patterns for the diverging/focusing systems with the inherent phase error on their aperture is discussed and applied to the curved leakywave structure. The result will be especially useful relating to the design of the curved leakywave structure in the microwave/mm-wave applications.* © 2002 Wiley Periodicals, Inc.
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Key words: *field region; diverging/focusing systems; curved leakywave structure*

1. INTRODUCTION

As the use of millimeter-wave spectrum in many applications, including the indoor wireless LAN(WLAN) is increasing, development of antennas suited for each purpose is desired. For example, the transmitting/receiving antennas with relatively wide responding angle can be obtained from the curved leakywave structures [1–3].

In this article, we attempt to extend the concept of "field regions" [4] addressed with relation to the unfocused large apertures, into the diverging and focusing systems, and use it to discuss qualitatively well-known or indefinite features for these systems.