

A 1.2 V 2.4 GHz Low Spur CMOS PLL Synthesizer with a gain boosted Charge Pump for a Batteryless Transceiver

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Abstract — This paper presents a low power 1.2 V, 2.4 GHz low spur, Quadrature PLL synthesizer for IEEE 802.15.4 batteryless transceiver in CMOS 0.18 μm technology. The PLL employs a 1 MHz fully programmable divider with an improved CML 2/3 prescaler, a novel bit-cell for the programmable counters and a novel charge pump with gain-boosted technique to reduce the PLL reference spurs. The PLL consumes a power of 1.85 mW at 1.2 V power supply with the programmable divider consuming only 350 μW . The phase noise of the PLL is -112.77 dBc/Hz at 1 MHz offset and the spurs are -46.2 dB below the carrier and the PLL is successfully tested with the energy harvesting circuit.

Index Terms — Phase locked loop (PLL), Frequency synthesizer, Voltage controlled Oscillator (VCO), current-mode logic (CML), D flip-flop (DFF) Prescaler, Charge Pump.

I. INTRODUCTION

The rapid evolution of the communication industry has tremendously increased the demand for low-cost and low power fully integrated RF transceivers at GHz operation. Of the various wireless communication standards developed, IEEE 802.15.4/Zigbee were tailored towards low data rate and low power wireless solutions with emphasis on sensor network applications. Frequency synthesizers play an important role in communication and timing systems. Most of the work published so far in the literature have demonstrated the improvements in phase noise, spur-suppression, settling time, tuning range and programmability of the dividers [1],[2] and the design of low voltage frequency synthesizers [3], and specifically low voltage prescalers are very challenging. This paper emphasize on the design of a low voltage PLL synthesizer with an improved CML 2/3 prescaler, a novel-bit-cell for the counters and a proposed gain boosting charge pump which is integrated with a direct conversion transmitter, low-IF receiver [4] and an energy harvesting circuit.

II. PLL SYNTHESIZER ARCHITECTURE

The implemented PLL design shown in Fig.1 has an improved programmable divider, a novel bit-cell for the programmable (P) and Swallow (S) counters and a pro-

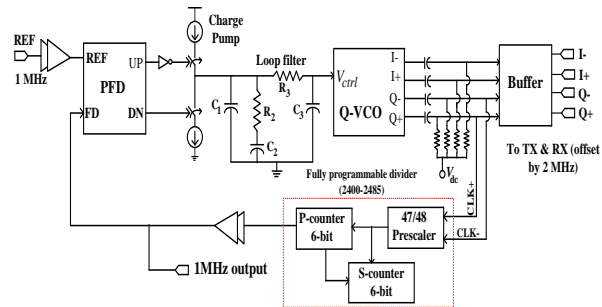


Fig. 1. Implemented 2.4 GHz PLL Synthesizer

posed charge pump. The differential outputs ($Q+$, $Q-$) of the VCO drives the CML 2/3 prescaler, while the other outputs $I+$, $I-$ are connected to the dummy prescaler for a balanced load. Since the receiver is offset by 2 MHz from the transmitter, we have chosen the reference frequency of 1 MHz and the divider is programmable from 2400-2480 with 1 MHz resolution.

A. Low-voltage fully programmable divider

The fully programmable divider is implemented by a 47/48 prescaler, a 6-bit programmable P -counter and a 6-bit Swallow S -counter similar to the design reported in [2]. However in this design, the 47/48 is implemented using both CML and dynamic logic flip-flops as shown in Fig.2a. The dynamic logic 2/3 prescaler reported in [5] has a maximum operating frequency of 6.5 GHz at 1.8-V power supply and as the power supply reduces to 1.2-V, the maximum frequency of operation drops to 2.6 GHz. As a result, we have chosen to implement 2/3 prescaler using CML and the divide-by-16 circuit using a dynamic logic.

Most of the CML 2/3 prescalers [1], [6] reported thus far have used two flip-flops (FF's), an AND and an OR gates where both the logic gates are embedded into the first flip-flop. As a result, the first flip-flop has more stacked transistors and thus has slow sensing speed from the input to output node compared to that of the 2nd flip-flop. In the improved design, we have replaced an OR and AND gate with two OR gates as shown in Fig.2a. Since only one OR

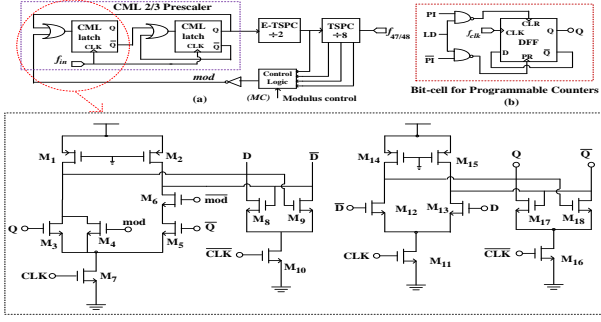


Fig. 2. (a) 47/48 prescaler with improved CML 2/3 prescaler (b) bit-cell for programmable counters

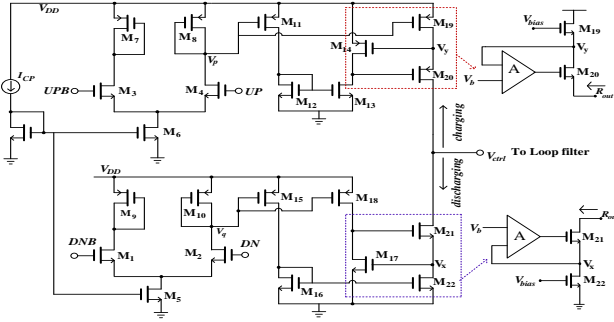


Fig. 3. Proposed gain-boosted charge pump

gate is embedded into a flip-flop, both the flip-flops has symmetrical structure and has same sensing speed from the input to output node, resulting in improved speed of operation. The 47/48 prescaler can operate up to 5 GHz and consumes only $450 \mu\text{A}$ from 1.2-V power supply.

In the conventional PLLs, the maximum number of bit-cell's stacked transistors in the programmable counter are at least 5 [5], [7] and this limits the low-voltage operation of the programmable divider. In this work, a novel gate level logic bit-cell is implemented as shown in Fig.2b. The bit-cell is designed using a DFF with preset (PR) and clear (CLR) functions and two NAND gates. Here, PI is the programmable input and if $LD=0$, the bit-cell acts as divide-by-2 and when $LD = 1$, the bit-cell transfers the loaded PI input to the output. The programmable divider consumes around $350 \mu\text{W}$ from 1.2 V power supply.

B. Proposed Gain-boosted charge pump

One of the common techniques used for reducing the mismatch currents is to increase the length of transistors in the output stage or increasing output impedance. The charge pump reported in [8] uses gain boosting technique to reduce the mismatch currents. However, in [8], current mismatches exists due to single ended input switches (UPB, DN) of the charge pump implemented by PMOS and NMOS. On other hand, other charge pumps implemented with NMOS only switches have assymetrical charging and discharging paths. Fig.3 shows the proposed charge pump with NMOS only switches and gain boosting

stages added in the pump-up and pump-down sub-circuits, making the charging and discharging paths symmetrical. In the pump-up sub-circuit, transistors M_{14} , M_{19} and M_{20} are used for gain boosting while the transistors M_{17} , M_{21} and M_{22} are used for gain boosting in the pump-down sub-circuit. During the discharging mode ($DN=1$ and $UP=0$), the current I_{CP} is steered through M_2 to the output with the help of M_{10} , M_{15} , M_{16} and M_{22} . Here, the drain voltage of M_{22} is held at V_{gs} by M_{17} . If the drain voltage of M_{22} starts to decrease, M_{17} starts shutting-off, causing the gate voltage of M_{21} to increase, and pulls back the drain voltage of M_{21} . Thus, the drain current of M_{21} remains constant and the same applies to the gain boosting stage of pump-up sub-circuit. This technique allows the charging and discharging currents to be constant and reduces the mismatch current flowing in to the passive filter. For a charge pump current of $25 \mu\text{A}$, the mismatch current reduces by nearly 3 times and the spurs due to mismatch current improves by nearly 10 dB compared to the chargepump without gain boosting stage.

C. VCO, Phase Frequency Detector and Loop Filter

The VCO used in this design is parallel Q-VCO compared to series Q-VCO implemented in [2] due to lower supply voltage. The tuning range of the VCO designed is 2.35-2.7 GHz and the gain is 280 MHz/V. The simulated phase noise of the VCO is -116 dBc/Hz at 1 MHz offset and consumes a power of 1.3 mW at 1.2 power supply. The basic tri-state PFD is used in this design and the dead zone removal pulse width is around 8 ns. The loop filter used in this design is 3rd order loop with a bandwidth of 45 kHz. The values of C2, C1, R2, C3, and R3 are 121 pF, 7.5 pF, 116 k Ω , 6.2 pF and 92 k Ω respectively. The settling time of the PLL is around 58 us which is nearly 3.3 times smaller than the value required by IEEE 802.15.4 standard. The core area of the PLL synthesizer is $0.9 \times 0.85 \text{mm}^2$.

III. MEASURED RESULTS

For silicon verification, the fully integrated 1 MHz resolution PLL frequency synthesizer is integrated with a low-IF receiver and a direct conversion transmitter and is fabricated in GlobalFoundries 0.18 μm technology. Fig.4a shows the PCB test board and measurement setup of the PLL, while Fig.4b shows the packaged chip. The input signal is provided by the Agilent 33120A arbitrary signal generator and output signals are captured by the Lecroy wave master 8600A 6G oscilloscope. The output spectrum and phase noise of the synthesizer is measured using the Agilent E4407B 9 kHz-26.5 GHz spectrum analyzer.

Initially, regular power supplies are connected to the chip and the performance of the PLL synthesizer is measured. Once the PLL is calibrated, the power supply to the chip is disconnected and an energy harvesting circuit is connected to provide the power supply. The interface for

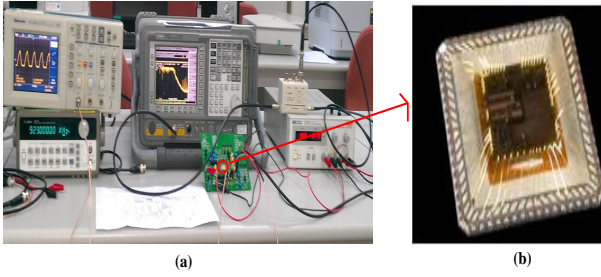


Fig. 4. (a) Test setup of PLL (b) Packaged PLL chip

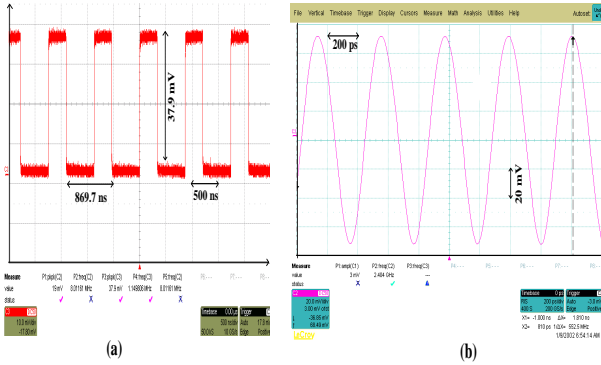


Fig. 5. (a) Programmable divider 1 MHz output (b) VCO output

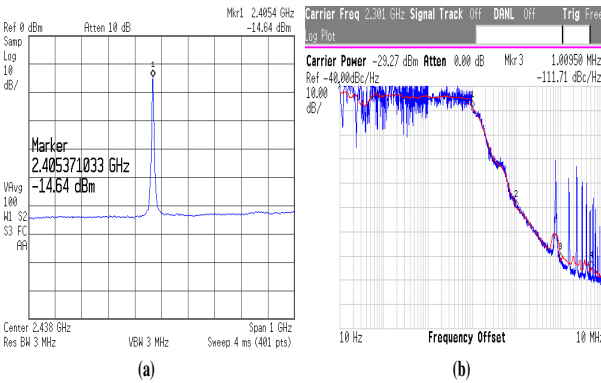


Fig. 6. (a) Measured PLL output spectrum (b) Phase noise

the energy harvesting circuit [9] is designed on the PCB board, while the energy harvesting circuit is implemented on the separate PCB board. Fig. 5a and Fig.5b shows the measured 1 MHz output of the programmable divider and VCO output signal respectively. The measured tuning range of the Parallel-QVCO is 2.17 GHz-2.48 GHz. Fig.6a and Fig.6b shows the measured PLL output spectrum and phase noise plots respectively. The measured phase noise of the PLL is -112.77 dBc/Hz at 1 MHz offset and the reference spurs are -46.2 dB below the carrier. The PLL consumes only 1.85 mW at 1.2 V, while the fully programmable divider consumes less than 0.35 mW. Table I compares the performance of the implemented PLL with other designs in the literature. The PLL is implemented along with the energy harvesting system reported in [9]

TABLE I
PERFORMANCE OF PLL SYNTHESIZERS AT 2.4 GHz

Design Parameters	[1]	[3]	This work
Process (μm)	0.18	0.18	0.18
Channel Spacing	5 MHz	-	1 MHz
Tuning Range (GHz)	2.4-2.48	2.4-2.64	2.17-2.48
Loop filter	on-chip	on-chip	on-chip
Phase Noise (dBc/Hz)	-108.55	-110.5	-112.77
Reference Spurs (dBc)	-40.84	-39.5	-46.2
Power Consumption	7.95 mW	14.4 mW	1.85 mW

and tested successfully.

IV. CONCLUSION

We have presented a detailed design of CMOS fully programmable frequency synthesizer tested with energy harvesting circuit which consumes less than 2 mW of power and suitable for a battery-less system. The frequency synthesizer is implemented in RF CMOS 0.18 μm technology at 1.2 V power supply using proposed low power building blocks such as low power CML 2/3 prescaler, bit-cell for the counters and a gain boosting charge pump.

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