

A 1.8-V 6.5-GHz Low Power Wide Band Single-Phase Clock CMOS 2/3 Prescaler

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Abstract—In this paper, the switching and short-circuit power consumption and the operating frequency of the extended true single-phase clock (E-TSPC) based divide-by-2/3 prescaler is investigated. Based on this analysis, a new ultra low power wide band 2/3 prescaler is proposed and implemented using a GlobalFoundries 0.18 μm CMOS technology. Compared with the existing E-TSPC architectures, the proposed 2/3 prescaler is capable of operating up to 6.5 GHz and eliminates the switching and short circuit power of the first D flip-flop (DFF) during the divide-by-2 operation and also the short-circuit power consumption in the first stage of the second D flip-flop. When compared under the same technology at supply voltage of 1.8-V, a 50% reduction in total power consumption is achieved during divide-by-2 operation. The proposed divide-by-2/3 unit consumes a power of 1 mW and 1.8 mW during divide-by-2 and divide-by-3 modes respectively.

Index Terms—DFF, frequency synthesizer, E-TSPC, true single-phase clock(TSPC), high speed digital circuits, Dual modulus prescalers.

I. INTRODUCTION

THE Rapid evolution of the communications industry has greatly increased the demand for lower cost, lower power and wider bandwidth RF circuits operating at microwave frequencies with higher level of integration. Intensive effort has been made to develop RF integrated circuits and systems at the range of gigahertz using low-cost CMOS process [1]. Low Power consumption helps to increase the battery life time and to reduce the operating temperature.

Frequency dividers (FDs) also called prescalers are used in many communications applications such as frequency synthesizers, timing-recovery circuits and clock generation circuits. The prescaler is employed in the feedback path of the synthesizer, takes a periodic signal and generate a periodic output signal whose frequency is a fraction of the input frequency. The prescaler is one of the most critical block in the frequency synthesizer since it operates at the highest frequency and consumes large power. Thus the power reduction in the first stage of the prescaler is important in realizing a low power frequency synthesizer.

The state of the art CMOS $N/(N+1)$ prescalers can be designed using different styles such as injection locked FDs (ILFDs) [2] or current-mode logic (CML) latches [3], [4]. ILFDs have a very narrow locking range and requires a large chip area. Normally, high speed flip-flop based prescalers are designed using current-mode logic (CML) latches. However, a major disadvantage associated with conventional prescalers

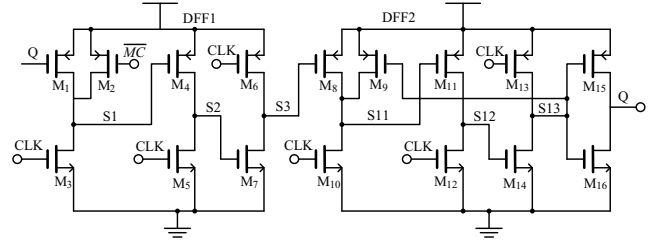


Fig. 1. E-TSPC 2/3 prescaler in [8]

using CML circuits stems from the large load capacitances seen by the circuit blocks, which limit the maximum operating frequency and current-drive capabilities and increase the total power consumption [3], [4].

Alternatively, flip-flop based prescalers can be designed using dynamic logic flip-flops such as true single-phase clock (TSPC) [5] and extended true single-phase clock [6]. The prescaler based on dynamic logic flip-flops have lower power consumption and low frequency of operation compared to that of CML logic style. However, the highest achieved operating frequency by TSPC and E-TSPC based prescalers [7], [8] are 5 GHz and 4.5 GHz respectively. In this paper, a new ultra low power wide band single-phase clock 2/3 prescaler is proposed which can be used in constructing the prescaler for wide-band and multi-band applications without using CML logic style prescaler in the first stage, thus avoiding the driving capability issues and reducing overall power consumption of the prescaler.

II. E-TSPC 2/3 PRESCALER

The TSPC 2/3 prescaler reported in [7] consumes very low power and has the maximum operating frequency of 5 GHz. However, its operating frequency drops to 4.5 GHz when it is used in the design of 32/33 prescaler. The E-TSPC 2/3 prescaler reported in [8] which is improved version of [6] has a maximum operating frequency of 4.5 GHz, but our resimulation with optimized transistor sizes shows that it can extend its operation up to 7.5 GHz. The prescaler in [8] consists of two DFFs and two NAND gates embedded in the flip-flops as shown in Fig.1. The total load capacitance of the prescaler is given by (1) which is calculated by using the methods described in [9].

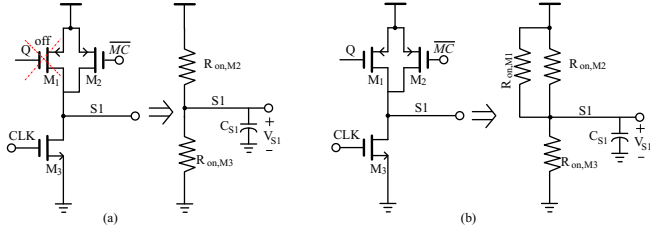


Fig. 2. First stage of the DFF1 during the divide-by-2 operation

$$C_{L_E-TSPC} = C_{dbM13} + 2C_{gdM13} + C_{dbM14} + 2C_{gdM14} + C_{gM1} \quad (1)$$

where C_{gM1} is approximately equal to

$$C_{gM1} \propto \frac{C_{gdM1} + C_{gdM2}}{2} \quad (2)$$

When \overline{MC} is '1', the prescaler operates in the divide-by-3 mode where two flip-flops DFF1 and DFF2 actively participate in the operation. When \overline{MC} is '0', the prescaler operates in the divide-by-2 mode, where PMOS transistor M_2 is always ON suppressing the switching activities in DFF1 such that the nodes S1, S2 and S3 remain at logic '1', '0' and '1' respectively. Thus the switching power is saved in DFF1 during the divide-by-2 operation. However, there always exists very high short-circuit power in the first stage of the DFF1 and improper device sizing can still result in switching activities in the DFF1 during the divide-by-2 operation.

A. Short-Circuit and Switching Power Analysis: Divide-by-2 mode

1) M_2, M_3 ON and M_1 OFF: Fig.2a shows the first stage of DFF1 in prescaler [8] where the PMOS transistor M_2 is ON for the entire divide-by-2 operation and M_3 is ON for half of the input clock period during which there exists a direct path between the supply and ground resulting in high short-circuit power as shown in Fig.3. The shaded region indicates the short-circuit period. Let I_{sc1} be the short-circuit current that flows from the supply to ground when M_2 and M_3 are turned-ON and I_{sc2}, I_{sc3} be the short-circuit currents due to finite rise (t_r) and fall (t_f) time of the clock signal. The total short-circuit power in the first stage is estimated by the methods in [10], which is given by (3).

$$P_{sc1} = \frac{V_{dd}}{T_{clk}} \left(\int_0^{t_r} I_{sc2} + \int_{t_r}^{\frac{T_{clk}}{2} - t_f} I_{sc1} + \int_{\frac{T_{clk}}{2} - t_f}^{\frac{T_{clk}}{2}} I_{sc3} \right) \quad (3)$$

The analysis in [8] shows that the nodes S1, S2 and S3 remains at logic '1', '0' and '1' respectively during the divide-by-2 operation reducing the switching power. However, this is not always true as node S1 doesn't settle to logic '1' and its value depends on the sizing of the transistors M_1, M_2 and M_3 . Since M_2, M_3 have finite ON resistance, the node voltage V_{S1}

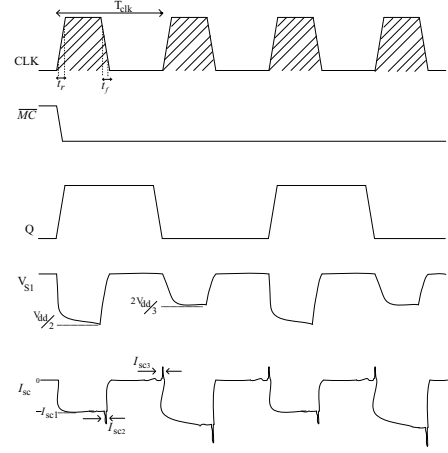


Fig. 3. Short-circuit and switching power analysis of First stage DFF1 during the divide-by-2 operation

is decided by the sizing of transistors M_2 and M_3 as given by (4), (5). The load capacitance C_{S1} at node S1 is given by (6).

$$V_{S1} = \frac{R_{ON,M3}}{R_{ON,M3} + R_{ON,M2}} * V_{dd} \quad (4)$$

$$V_{S1} = \frac{W_{M2} \mu_p}{W_{M2} \mu_p + W_{M3} \mu_n} * V_{dd} \quad (5)$$

$$C_{S1} = C_{dbM2} + 2C_{gdM2} + C_{dbM3} + 2C_{gdM3} + C_g \quad (6)$$

where W_{M2}, W_{M3} are the widths of the transistors M_2, M_3 and C_g is the gate capacitance of the next stage transistor connected to node S1. From (5), if $W_{M2} \mu_p = W_{M3} \mu_n$, the voltage at S1 continuously charges and discharges between V_{dd} and $V_{dd}/2$ as shown in Fig.3 and thus causes switching power in the first stage. There is also the high possibility that M_2 turns-ON causing the short-circuit power in the second stage of DFF1 for a period equal to half of the clock period and also a considerable amount of switching power. The worst case would be when $W_{M2} \mu_p < W_{M3} \mu_n$ where node S1 settles to a voltage lesser than $V_{dd}/2$, turning ON M_4 completely and cause continuous switching activities and high short-circuit power P_{sc2} in second stage of the DFF1.

2) M_2, M_3 and M_1 ON: Fig.2b shows the first stage of DFF1 when M_2 is always ON, M_3 turns ON for every half of the input clock period and M_1 turns ON for half clock period for every 2 clock cycles. Since M_1, M_2 and M_3 have finite ON resistance and width of M_1 and M_2 are same (assuming $R_{ON,M2} = R_{ON,M1}$), voltage at node S1 is given by (7), (8) and load capacitance C_{S1} is given by (9).

$$V_{S1} = \frac{R_{ON,M3}}{R_{ON,M3} + \frac{R_{ON,M2}}{2}} * V_{dd} \quad (7)$$

$$V_{S1} = \frac{W_{M2} \mu_p}{W_{M2} \mu_p + 2W_{M3} \mu_n} * V_{dd} \quad (8)$$

$$C_{S1} = C_{dbM2} + 2C_{gdM2} + C_{dbM3} + 2C_{gdM3} + C_g + C_{dbM1} + 2C_{gdM1} \quad (9)$$

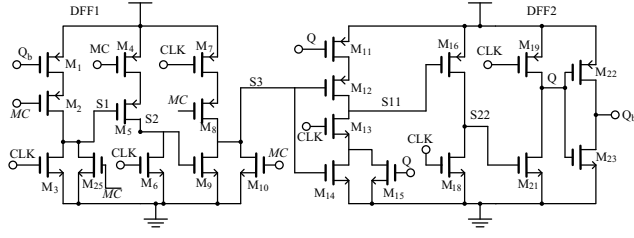


Fig. 4. Proposed Wideband 2/3 prescaler

Fig.7 shows that if $W_{M2} \mu_p = W_{M3} \mu_n$, node S1 discharges to a voltage of $2/3(V_{dd})$ (M_1 and M_3 ON) and to a voltage of $V_{dd}/2$, when M_1 is OFF and M_3 is ON. Since node S1 continuously charges and discharges between V_{dd} , $V_{dd}/2$ and $2/3(V_{dd})$, there exists switching power in the first and second stages of DFF1 during the divide-by-2 operation. Finally, the total power consumption of DFF1 during the divide-by-2 operation is given as follows:

$$P_{DFF1} = (P_{sc1} + P_{sc2}) + \frac{V_{dd}}{T_{clk}} \left(2 \int_0^{t_{r3}} I_{sc5} \right) + (f_{clk} V_{dd}^2 C_{S1}) + (f_{clk} V_{dd}^2 C_{S2}) \quad (10)$$

where C_{S1} , C_{S2} are load capacitances at nodes S1 and S2 and P_{sc1} , P_{sc2} are the short-circuit power consumption of the first and second stages of DFF1. I_{sc5} is the short-circuit current in the third stage due to finite rise and fall times. If $W_{M2} \mu_p > W_{M3} \mu_n$, the voltage at node S1 discharges from V_{dd} to a value greater than $V_{dd}/2$, thus turning OFF M_4 completely and eliminates the switching and short circuit power in the second stage of DFF1. Neglecting the short-circuit power due to finite rise and fall times, the total power consumption in DFF1 is given by (11)

$$P_{DFF1} = P_{sc1} + (f_{clk} V_{dd}^2 C_{S1}) \quad (11)$$

From the above analysis, it is found that the switching power is not zero in DFF1 during the divide-by-2 operation and there also exists high short-circuit power in the first two stages of DFF1 for every half of the input clock period. The prescaler in [8] also needs an extra inverter to provide the control logic \overline{MC} . To overcome all these problems, a new low power, wide band single-phase clock 2/3 prescaler is proposed in the section-III.

III. PROPOSED WIDE BAND 2/3 PRESCALER

The Proposed wide band 2/3 prescaler consists of two D flip-flops and two NOR gates embedded in to the flip-flops as shown in Fig.4. The first NOR gate is embedded in the last stage of DFF1 and second NOR gate is embedded in the first stage of DFF2. Here, additional transistors M_2 , M_{25} and M_4 are added in DFF1 to eliminate the short-circuit power during the divide-by-2 operation. The switching of division ratios between 2 and 3 is controlled by logic signal MC . The total load capacitance of the proposed prescaler is given by (12)

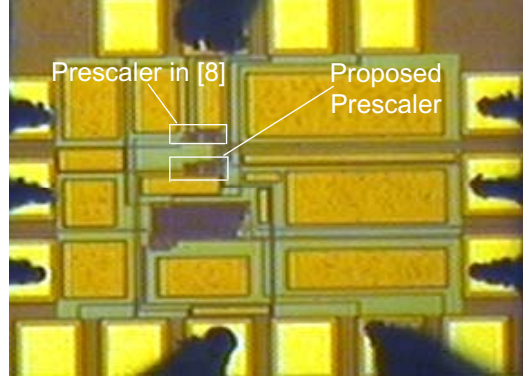


Fig. 5. Die photograph of the proposed prescaler and prescaler in [8]

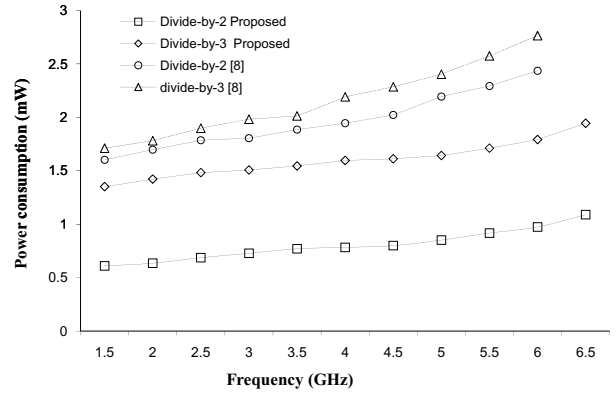


Fig. 6. Measured power consumption of Proposed prescaler and prescaler in [8]

$$C_{L_proposed} = C_{dbM19} + 2C_{gdM19} + C_{dbM21} + 2C_{gdM21} + C_{gM1} \quad (12)$$

A. Divide-by-2 operation

When logic signal MC switches '0' to '1', the proposed prescaler switches to divide-by-2 operation. At the rising edge of first clock cycle, nodes S1, S2 and S3 switch to logic '0' and remain at same level for the entire divide-by-2 operation since transistors M_2 , M_5 and M_8 turn-OFF completely, thus removing the switching power contribution of the DFF1. During the divide-by-2 operation, only DFF2 actively participates in the operation and contributes to the total power consumption since all the switching activities are blocked in DFF1. Thus the proposed prescaler has the benefit of saving more than 50% of the power compared to the prescaler in [8]. Since one of the transistors M_{12} or M_{14} is always turned-OFF, the short-circuit power in the first stage of DFF2 is also eliminated. Thus a considerable amount of power is also saved during the divide-by-3 operation. The die photograph of the proposed prescaler and prescaler in [8] is shown in Fig.5. The simulation results shows that the prescaler in [8] has the maximum operating frequency of 7.5 GHz while that of the proposed prescaler is slightly higher and equal to 8 GHz.

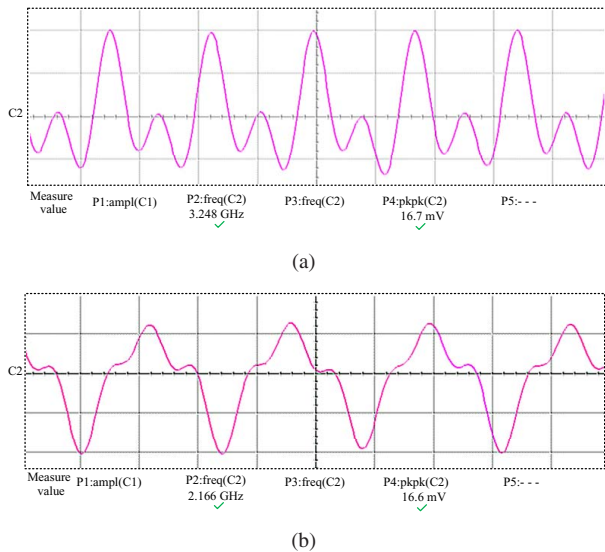


Fig. 7. Measured results of 2/3 prescaler(a)Divide-by-2 (b)Divide-by-3 at an input frequency of 6.5 GHz

IV. SIMULATIONS AND SILICON VERIFICATIONS

A complete analysis and comparison of the performance of the proposed wide-band 2/3 prescaler and E-TSPC based prescaler in [8] is carried out on the ground that the prescaler in [8] has the best performance in literature that is designed using single-phase clock flip-flops. The simulations are performed using Cadence SPECTRE RF for a 0.18 μ m CMOS process. The simulation results shows that the proposed 2/3 prescaler has the maximum operating frequency of 8 GHz with a power consumption of 0.92 mW, 1.73 mW during the divide-by-2 and divide-by-3 modes respectively. The 2/3 prescaler in [8] has maximum operating frequency of 7.5 GHz with a power consumption of 1.67 mW, 1.77 mW during the divide-by-2 and divide-by-3 modes respectively.

For silicon verification, the proposed 2/3 wide-band prescaler and the 2/3 prescaler in [8] are fabricated using the GlobalFoundries 1P6M 0.18 μ m CMOS process. On-wafer measurements are carried out using an 8 inch RF probe station. The input signal for the measurement is provided by the 83650B 10 MHz-50 GHz HP signal generator and the output signals are captured by the Lecroy Wavemaster 8600A 6G oscilloscope. The measurement results shows that the proposed wide-band 2/3 prescaler has maximum operating frequency of 6.5 GHz slightly higher than that of the 2/3 prescaler in [8], whose maximum operating frequency is found to be 6 GHz. The maximum frequency of operation that could be achieved compared to simulations is limited by large parasitics and buffer at the output stage. Fig.6 shows the power consumption of the proposed prescaler and the prescaler in [8] at different frequencies. Fig.7 shows the measured output waveform of the proposed wide-band 2/3 prescaler at an input frequency of 6.5 GHz in divide-by-2 and divide-by-3 modes respectively. Table I compares the performance of the proposed 2/3 prescaler and the 2/3 prescaler reported in [8] at 6 GHz.

TABLE I
PERFORMANCE OF DIFFERENT PRESCALERS

Design Parameters	Prescaler in [8] resimulated	Proposed Prescaler
Process (μ m)	0.18	0.18
supply voltage (V)	1.8	1.8
Max.Frequency (GHz) (Sim/Measured)	7.5 / 6	8 / 6.5
Power(mW) (sim/measured) Divide-by-2 mode	1.63 / 2.2	0.82 / 0.97
Power(mW) (sim/measured) Divide-by-3 mode	1.85 / 2.62	1.61 / 1.78

V. CONCLUSION

In this paper, the short-circuit and switching power consumption of the 2/3 prescaler in [8] is analyzed and a new low power single-phase clock 2/3 prescaler is proposed whose measured maximum operating frequency is 6.5 GHz. The proposed 2/3 prescaler saves more than 50% of power compared to that of the 2/3 prescaler in [8] in divide-by-2 mode and also eliminates short-circuit power in the first stage of DFF2, thus reducing the total power consumption during divide-by-2 and divide-by-3 modes. The design is silicon verified using the GlobalFoundries 0.18 μ m CMOS technology. The proposed 2/3 prescaler consumes a power of 1 mW and 1.8 mW at 6.5 GHz during divide-by-2 and divide-by-3 modes respectively and provides a solution to the low power PLL synthesizer for WiMax and IEEE 802.11a/b/g WLAN applications.

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