A 1-V CMOS Ultralow-Power Receiver Front End for the IEEE 802.15.4 Standard Using Tuned Passive Mixer Output Pole

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***Abstract*—A novel receiver architecture is proposed which uses a voltage-mode passive mixer with a tuned output pole. Using this technique, it is shown that the IF section's IIP_3 requirements are relaxed by up to 33 dB for the IEEE 802.15.4 standard. This allows for use of an ultralow power IF section without linearity compensation. The overall receiver front end consisting of an LNA, a mixer and a third-order channel-select filter is designed in 0.18 µm CMOS technology with a 1-V supply voltage, and post-layout simulations show a 5 dB NF with only 1.7-mW total power consumption.**

***Index Terms*—RF Front End, CMOS RF Integrated Circuits, Low Power, System on Chip.**

TABLE I
OVERALL SENSITIVITY VERSUS MIXER TYPE FOR RECENT LOW-POWER FRONT ENDS

Reference	[2]	[3]	[4]	[5]	[6]	[7]	[8][B]
Sen_{NF} (dBm)	-91.3	-92	-91.9	-91	-89.7	-87	-90.7
Sen_{IIP3} (dBm)	-110	-68	-127	-118	-126	-112	-88
Mixer Type[A]	PC	A	PV	PV	PC	A	PC
Tech. (nm)	180	180	130	90	180	180	180
Power (mW)	10	1.4	0.75	4.05	6.3	10.8	5.4
IF Power (mW)	5.76[C]	0.5	0.75	1.15	4.5	-	0.36

[A] A: Active, PV: Passive Voltage-mode, PC: Passive Current-mode
[B] Second gain mode
[C] Estimated only.

I. INTRODUCTION

THE IEEE 802.15.4 standard [1] was designed to cater to the increasing demand for low-power, low data-rate applications such as wireless sensor networks, and wireless personal area networks (WPAN). Such applications often require mobile devices or devices in remote locations without a connection to the power mains. Therefore, low power consumption is a critical requirement for extending the battery life of such devices.

This work deals with the upper band of the IEEE 802.15.4 standard which is the 2.4-GHz Industrial Scientific and Medical (ISM) band. The system bandwidth is 83.5 MHz from 2.4 GHz to 2.4835 GHz. The standard offers 16 channels with 5-MHz spacing, and an IEEE 802.15.4 signal occupies a 2-MHz bandwidth and provides a data rate of 250 kb/s. The standard features relaxed requirements in terms of adjacent and alternate channel interference (+0 dBc and +30 dBc respectively) and a sensitivity requirement of -85 dBm.

This work focuses on receiver architecture design for low-power operation. In section II we make the case for the use of passive mixing over active mixing. In section III, we discuss the proposed passive mixer topology and show that it can offer a 33 dB improvement in IF section IIP_3. In section IV we discuss the overall system design, and in section V we present simulation results of the proposed design. The design has been sent for fabrication in a 0.18 µm RFCMOS process and will be subsequently characterized.

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II. THE CASE FOR PASSIVE MIXERS

Among recent low-power research works, architectures using passive mixers have generally out-performed those using active mixers in terms of overall sensitivity (for the IEEE 802.15.4 standard) [2]-[8]. This is mainly attributable to the fact that passive mixers minimally distort the input signal (due to the passive operation), and do not add flicker noise to the system. However, a standard Gilbert-Cell mixer does both. Given the IEEE 802.15.4 standard receiver blocking profile [7], we can calculate the sensitivity based on IIP_3 as,

$$Sen_{IIP3} = 3P_{blk} + SNR_{req} - 2IIP_3 \quad (1)$$

where P_{blk} is the interfering power, SNR_{req} is the required output signal to noise ratio (SNR), and IIP_3 is the receiver input-referred third order intercept power. From [9], we estimate the SNR_{req} to be approximately 14 dB while P_{blk} is -52 dBm in the worst case when the input power is 3-dB higher than the required sensitivity (-85 dBm [1]). The sensitivity based on noise figure (NF) can be easily calculated as,

$$Sen_{NF} = NF + 10\log(kT\Delta f) + SNR_{req} \quad (2)$$

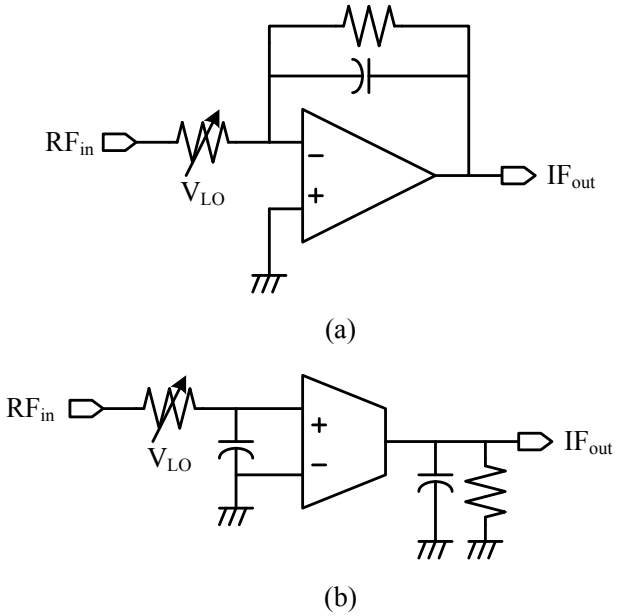

Fig. 1 A simplified illustration of connection between (a) a current-mode passive mixer and an op-amp based filter, and (b) a voltage-mode passive mixer and a g_m-C based passive mixer.

where $kT\Delta f$ is -111 for a 2 MHz signal bandwidth. Table I shows the sensitivity of designs [2]-[8] and the mixer type used. We have included the overall power consumption as was published, but it is important to note that different works presented more or less complete systems. Furthermore, certain designs [3], [4] were not specifically designed for the IEEE 802.15.4 standard. Table I clearly shows the advantage of using passive mixers in IEEE 802.15.4 systems. Of the two designs using active mixers, [3] fails to meet sensitivity requirements based on IIP_3, and [7] requires more power consumption than other works.

Two different types of passive mixers have emerged in recent literature, namely, current-mode and voltage-mode passive mixers. Current-mode passive mixers use a passive switching stage followed by a transimpedance amplifier (TIA) [6] in order to convert the switching stage's output current into a voltage. Voltage-mode passive mixers require that the following stage have high input impedance so that the output of the switching stage is in voltage form. Therefore, current-mode passive mixers connect naturally with op-amp based channel-select filters (CSF), while voltage-mode passive mixers connect naturally with G_m-C type CSFs. This is illustrated in Fig. 1. The switching stages are represented by variable resistors controlled by a local oscillator (LO) voltage, V_{LO}.

The required filter should be of high enough order to remove the unwanted adjacent and alternate channel interference.

III. The Proposed Passive Mixer Architecture

As the RF circuitry (LNA, Mixer) must pass the entire system bandwidth (83.5 MHz for the IEEE 802.15.4 standard),

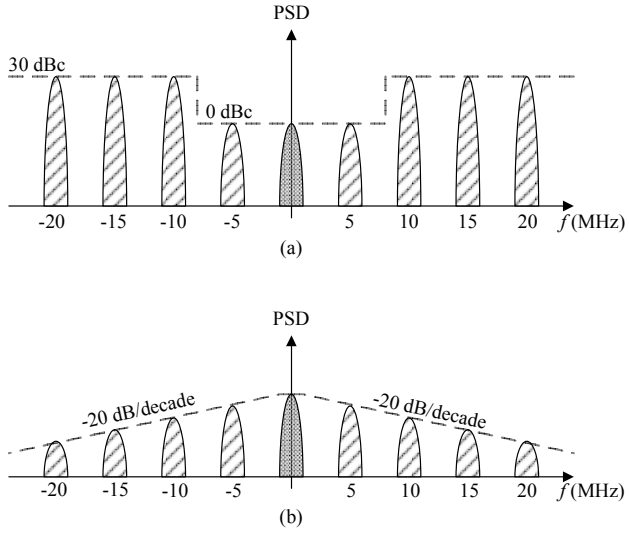

Fig. 2 Illustration of the effect of a single pole low-pass filter on IEEE 802.15.4 standard interference. The striped signals are interferers while the shaded signal is the desired signal.

the IIP_3 requirements are based on worst-case interference. Blocks following the CSF such as limiting amplifiers, variable-gain amplifiers (VGA), etc, do not need to meet such stringent linearity requirements since all of the interference is presumed to have been filtered off by the CSF. However, the CSF itself must still meet IIP_3 requirements which are tightened by the high gain of the RF front end required for good noise performance.

The high IIP_3 requirements of the IF section has led most designers to chose one of two options. The first option is to use a comparatively low RF section gain [4] (only 17 dB) and boost the noise performance of the IF section, which requires more power consumption in the IF section. The second option is to use highly linear CSFs such as op-amp based filters [10] as was done in [2], [4] and [5]. Op-amp based filters are able to achieve excellent linearity, but require a high loop-gain [11] possibly over the entire system bandwidth to reliably do so.

In this work, we propose an alternate method for relaxing the IIP_3 requirements of the IF section without requiring high power consumption. Going back to Fig. 1b, we note that the voltage-mode passive mixer is effectively an RC low-pass filter at the IF in cascade with a G_m-C type filter. In general, the real pole formed by the switch resistance and the output capacitance is not used for filtering because of the considerable variation in the switch resistance. The switch resistance can vary due to variations in the LO voltage (V_{LO}), the switch threshold voltage, the switch size, and even the output impedance of the previous stage (the LNA output resistance affects the passive mixer output resistance [8]). As the passive switching stage is highly linear, using the passive mixer's output pole provides filtering at no cost in noise, linearity or power consumption; it is essentially "free". As this pole is a first-order low-pass filter, it works best when coupled with a direct-conversion system. Fig. 2 shows the effect of the free pole on IEEE 802.15.4 interference.

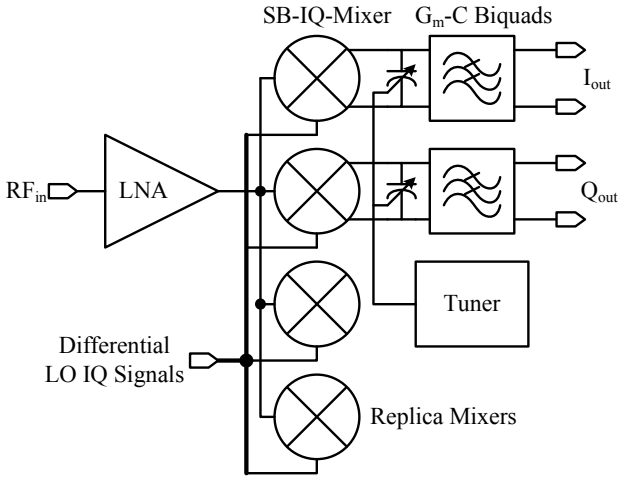

Fig. 3 Block diagram of the receiver front end. Differential LO IQ signals are externally derived and injected into the system. Replica mixers are used as part of the tuning circuitry for the passive mixer output pole. Single-balanced passive mixers convert the single-ended RF signal to a differential IF signal.

The most stringent IIP_3 requirement is based on the intermodulation of two tones at 10 MHz and 20 MHz offset from the desired signal. Before filtering, their IIP_3 requirement for -85 dBm sensitivity and 14 dB SNR is approximately -30 + G_{RF} dBm (using (1) where once again we take the signal strength to be 3 dB above the sensitivity level). Here G_{RF} is the gain in dB of the LNA plus the mixer. A first order filter provides 20 dB/decade or 6 dB/octave attenuation above the corner frequency. Given a 1-MHz signal bandwidth [2] at zero-IF, the corner frequency is set at 1 MHz. Therefore, after filtering, the 10 MHz tone is reduced by 20 dB and the 20 MHz tone is reduced by 26 dB. The new IIP_3 requirement of the filter is therefore -63 + G_{RF} dBm. This is a 33 dB improvement in the IIP_3 requirements over the standard case. Likewise, considering interfering tones at 5 MHz and 10 MHz offset from the desired tone, the improvement is 24 dB.

This 33 dB improvement can potentially be used to either improve the noise performance of the overall design by increasing the RF gain, or to reduce the current consumption of the IF section by using nonlinear G_m-C filters. The latter approach was adopted here. To give an idea of the importance of reducing IF section power consumption, we have included the IF section power consumption of recent works in Table I. The average IF section required 48% of the total receiver front end power consumption. The next section will describe the system design.

IV. Receiver Design

A block diagram of the receiver is shown in Fig. 3. The entire system uses a 1-V supply. The tuning circuitry is only operational in the tuning mode and therefore doesn't contribute to the overall power consumption. Differential IQ LO signals are derived externally to the system. The RF section consists of a single-ended LNA connected to voltage-mode passive mixers. The output pole of the passive mixers

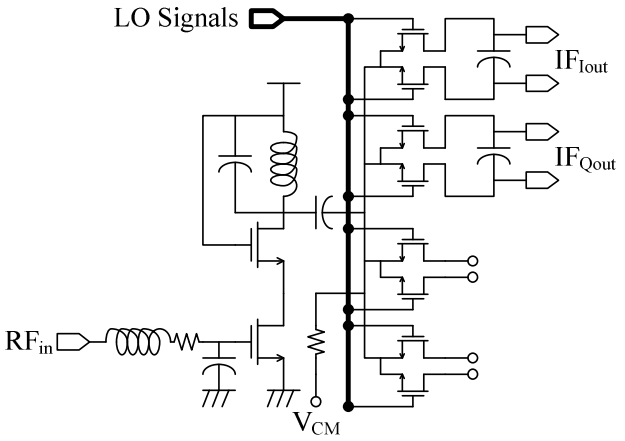

Fig. 4 Schematic of the LNA and single-balanced mixers including replica mixers used for tuning.

together with the G_m-C biquads form third-order butterworth type filters. The individual circuit blocks are described in more detail next.

A. The LNA and Mixers

A schematic of the LNA and mixers is shown in Fig. 4. Input matching is achieved using a series resonant network with a resistor in series. Under matched conditions, the noise figure of the matching network is 3 dB [12], and the voltage gain of the matching network is equal to the quality factor (Q) of the network. In this work, an 11.5 nH inductor was used resulting in a Q of 3.54 and a voltage gain of 11 dB. An LC tank was used to tune the output node of the LNA. The load inductor was 6.5 nH with a Q of 8.6 resulting in an effective output resistance for the LNA of 860 Ω. The LNA includes three gain control steps of 6 dB to ease the gain compression requirements of the IF section, and to allow for reduced power consumption at high input signal levels [8].

Single-balanced passive mixers were used to convert the single-ended RF signal into a differential IF signal. This allowed the use of a single-ended LNA thereby saving half of the LNA power consumption. The justification for this strategy is the relaxed IIP_2 requirements of the IEEE 802.15.4 standard. The main concern is unwanted DC-offset related to the self-mixing of either LO signals or strong interfering signals. Self mixing of LO signals results in a static DC offset which must be filtered before introducing any high gain stages to the signal. We can estimate the require IIP_2 based on self mixing of interfering signals as,

$$IIP_{2,req}(dBm) \geq 2P_{blk} - Sen + SNR_{req} \quad (3)$$

where Sen is the required sensitivity. Given alternate channel interferers equal to -52 dBm, the required IIP_2 is 2(-52) – (-82) + 14 = -8 dBm. The achieved IIP_2 of the down-converter can be estimated as P_{LO}/G_{leak} where G_{leak} is the ratio of the differential RF signal at the gates of the switching stages to the single-ended RF signal at the source of the switching stages (note that G_{leak} does not include common-mode leakage) and

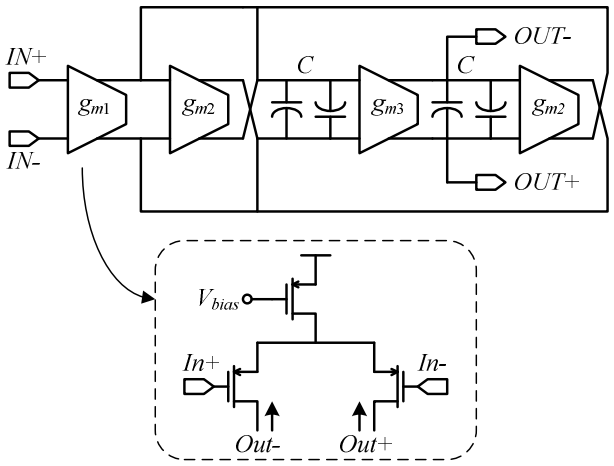

Fig. 5 Configuration of the G_m-C biquad and a transconductor.

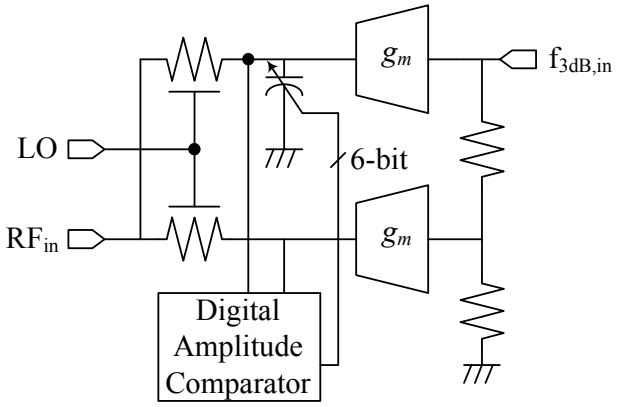

Fig. 6 Illustration of the passive mixer output pole tuning loop. The mixer is represented by variable resistors and the digital amplitude comparator provides peak detection, filtering, and analog to digital conversion.

P_{LO} is the LO power. G_{leak} is effectively a single-ended to differential leakage gain. In [13], it is shown that the IIP_2 of active mixers has similar dependency, while IIP_2 on the order of +40 dB is typical.

B. The Channel-Select Fitler

A third-order low-pass butterworth filter has two complex poles and a single real pole. As previously mentioned, the real pole is formed at the output node of the passive mixer. Therefore, each G_m-C filter needs only provide a pair of complex conjugate poles. A diagram of the G_m-C biquad is shown in Fig. 5. The DC gain of the filter is equal to g_{m1}/g_{m2} while the corner frequency is equal to $C^{-1}\sqrt{(g_{m2}g_{m3})}$ and the Q is equal to $\sqrt{(g_{m3}/g_{m2})}$. With four variables and three equations, we have one degree of freedom. This is used to select g_{m1} to provide the desired overall noise performance of the receiver system. The individual transconductors are configured as simple differential pairs. Using the passive mixer pole tuning method described in Section III, linearization of the transconductors [13] was not required. This allowed for the design of ultralow power biquads without sacrificing either noise or linearity performance.

As flicker noise is an important consideration in the design, PMOS devices were used as the inputs of the differential pairs. Although PMOS devices are generally slower than NMOS devices, the operation frequency of the biquads is low. With only a 1-V supply voltage, selection of the common-mode voltage of the IF section is important [14] as it will determine the maximum output swing of the filter. The common-mode voltage, V_{CM} was set at 0.3 V which allows approximately 0.5 $V_{pk\text{-}pk}$ of differential output swing. Gain compression requirements were further relaxed by the gain control in the LNA.

C. The Passive Mixer Tuning Loop

The principle of the tuning loop is illustrated in Fig. 6. The passive mixers are represented by variable resistors controlled by the LO signal. The output pole of the passive mixer consists of the resistance of the passive mixers and a bank of digitally controllable metal-insulator-metal (MIM) capacitors. A replica of the passive mixers without the output capacitors is also implemented. At the desired pole frequency, the real passive mixer will have a 3-dB lower output impedance than its replica.

A signal at the desired pole frequency (1 MHz in this case) is fed into the passive mixers' outputs via high output impedance transconductors which do not affect the passive mixers' output impedances. The 3-dB lower output impedance of the real passive mixer is imitated on the replica side by a 3-dB attenuation of the 1 MHz tuning signal. The output amplitudes of the transconductors are then detected and compared. This signal is filtered and fed into a digital comparator. The output of the comparator drives a 6-bit counter which is connected back to the passive mixers output capacitor to close the loop.

If the transconductor output on the real side is lower than that on the replica side, then the counter count down in order to lower the capacitance, and vice-versa. The tuning scheme implemented in this work is rather primitive and is only designed to illustrate the potential of tuning the output pole of the passive mixer. In a more advanced implementation, a successive approximation architecture [15] for the loop would reduce the required tuning time significantly.

V. Simulation Results

The design has been implemented in a 0.18 μm RFCMOS process and sent for fabrication. The process features a 6 metal layers including a 2.5 μm thick top metal for inductor design, and both 2-metal and 3-metal MIM capacitors for high density capacitance. The overall performance of the receiver front end is shown in Table II and compared with recent literature. At this phase of the design, the proposed design compares favorably to recent literature, although the raw performance attained by [4] is still superior. It should be noted that in [4], several techniques were used which may or may not be allowable in a robust design, such as the lack of input matching [16], and the lack of an LNA. As this is only simulated performance, we expect the overall performance may degrade in measurement.

TABLE II
SIMULATED PERFORMANCE OF THE PROPOSED DESIGN

Reference	[2]	[3]	[4]	[5]	This Work
Frequency Band (GHz)	2.4	2.4	2.4	2.4	2.4
[A]RF Bandwidth (GHz)	0.5	0.35	0.35	3.0	0.4
Power Consumption (mW)	10	1.4	0.75	4.05	1.7
IF Power (mW)	5.76[C]	0.5	0.75	1.15	0.31
Noise Figure (dB)	5.7	5.0	5.1	6.0	4.8
IIP_3 (dBm)	-16	-37	-7.5	-12	-12
[A]Technology Node (μm)	0.18	0.18	0.13	0.09	0.18

[A] Estimate when necessary
[B] CMOS only
[C] Estimated only

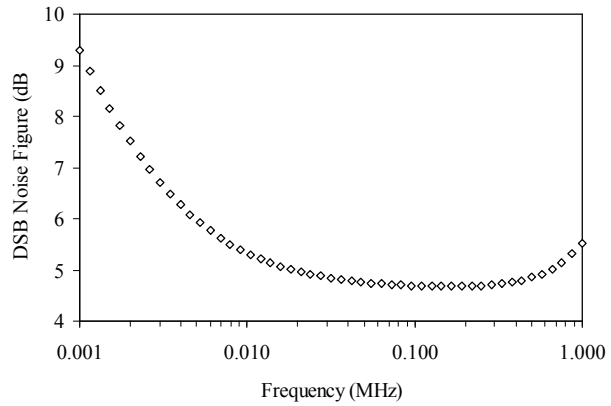

Fig. 7 DSB NF of the full receiver front end. The flicker noise corner frequency is approximately 10 kHz.

A. *Noise Figure and Gain*

The overall double-sideband (DSB) NF of the design is shown in Fig. 7. The minimum NF obtained was 4.8 dB. The flicker noise corner frequency is around 10 kHz and is significantly lower than sufficient in order to minimize overall flicker noise contribution. Fig. 8 shows the front-end gain up to both the CSF input and the CSF output. The LNA and mixer gain is 30 dB while the overall gain is 47 dB. The attenuation at 10 MHz is 20 dB and 60 dB respectively. The overall gain and out-of-channel attenuation are high enough that the following stages noise and linearity performance will not significantly affect the overall receiver performance.

B. *IIP_3*

Due to limitations in the device models used, IIP_3 results of devices operating at zero drain-source voltage are highly inaccurate [17]. Regardless, passive mixers have been shown to demonstrate high IIP_3 [18]. Therefore, in this section, we only demonstrate the effect of the use of the passive mixer output pole on the IIP_3 of the CSF. The IIP_3 of the CSF can be simulated by taking interfering tones at either 5 MHz and 10 MHz, or at 10 MHz and 20 MHz. The requirement for the former condition is looser than the latter, but conversely, the receiver IIP_3 under such conditions is worse. Fig. 9 shows the IF section IIP_3 under the former condition with and without the additional mixer pole. As expected, the improvement is 24 dB.

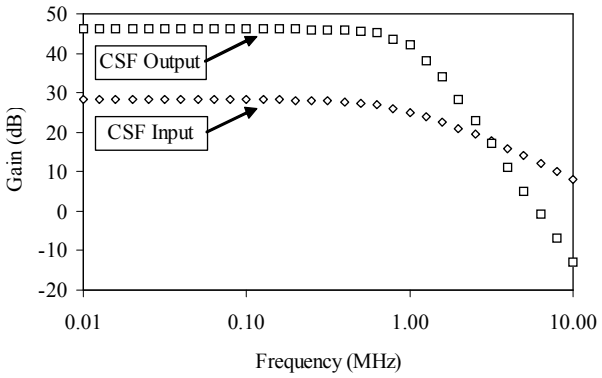

Fig. 8 Gain of the receiver front end up to the CSF input and the CSF output.

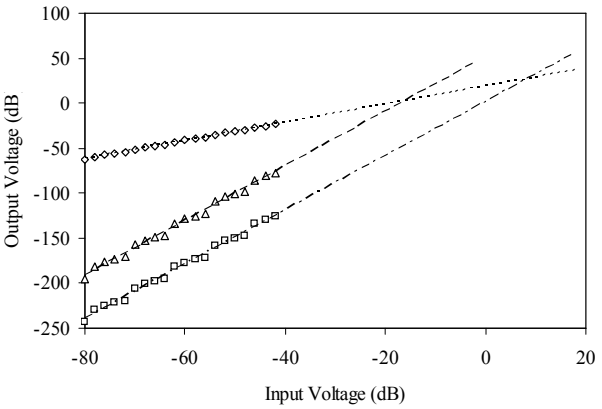

Fig. 9 IIP_3 of the CSF with and without the mixer output pole. The input tones are at 5 MHz and 10 MHz offset from the desired signal.

The IIP_3 is +8.3 dBV which is equivalent to 18.3 dBm into a 50-Ω resistor. Therefore, with 30 dB front-end gain, the overall IIP_3 is expected to be approximately -12 dBm.

VI. CONCLUSION

This work has presented a novel receiver architecture for low power low data-rate applications. Operating in the 2.4 GHz ISM Band, the proposed architecture improves IF stage IIP_3 by up to 33 dB for the IEEE 802.15.4 standard. This allows for use of a nonlinear low-noise IF section. The proposed idea was implemented in a 0.18-μm RFCMOS process and has been sent for fabrication. The proposed system compares favorably to recent literature while consuming the lowest power in the IF section among the designs.

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