RF & MMW FROM 5G TO BEYOND 6G

Research Area

- RFIC : Transceiver, LNA, PA, PLL, Mixer, VGA, Phase-Shifter, *et al.*
- Frequency: From DC to beyond 300GHz
- Process: CMOS (TSMC 28nm, GF RF SOI 45nm), III-V (Wolfspeed GaN, InGaAs etc)

Research Applications

- Mobile Wireless Communication
- High-speed Wireline Communication
- Vehicular Communication and Radar
- THz Communication

Assoc. Professor
Boon Chirn Chye
Program Director,
RF & MM-wave,
VIRTUS, NTU

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Web: https://www3.ntu.edu.sg/home/eccboon/

Research Funding in Recent 5 Years

Research Leadership in RF/MMW IC

Source of Grant/ Project Title	Quantum ($) Cash Only (Total including in-kind)	Role	Grant Period
Keysight Technologies Singapore – NTU Joint R&D: Transceiver test and development applicable for V2X-System and mmW	$133,750.00 ($1,650,000 in kind in test equipment)	PI	22 January 2020 to 21 January 2023
A*STAR (STAT Board)/ Transceiver Development Applicable for Hybrid "C-V2X+DSRC" V2X-System	S$2,889,900.00	PI	1 November 2019 to 31 October 2022
MIT-NTU: LEES-SMART-IRG/ LEES III-V + CMOS Circuits & System towards Commercialization (5 Projects)	S$2,465,760.00	PI	Since 1 April 2012 to 31 December 2021
MOE AcRF Tier 2/ CMOS Terahertz Plasmonic Interconnect towards Tera-scale Computing	S$788,736.00	PI	28 January 2019 to 27 January 2023
Delta Electronic-NTU, Wireless Het. Net. Transceiver Chipset	S$1,031,798.00	PI	01- July 2016 to 30 June 2021

Research Leadership in RF/MMW IC

Some Other Projects as PI

Completed projects

Project Title	Grant Type	Amount Approved	Role	Project Start Date	Project Actual Completion Date
LEES III-V + CMOS Circuits & System Towards Commercialization	Singapore-MIT Alliance for Research and Technology (SMART) Centre	496,800.00	Principal Investigator (Project)	01-Jul-2017	30-Jun-2019
LEES III-V + CMOS Circuits & System Towards Commercialization		496,800.00	Lead Principal Investigator	01-Jul-2017	30-Jun-2019
Monolithic Terahertz Passive Components in Advanced CMOS Technology: From Fundamental Understandings to Integrated Circuit Applications	AcRF Tier 1	133,300.00	Principal Investigator (Project)	01-Nov-2016	30-Apr-2019
Monolithic Terahertz Passive Components In Advanced CMOS Technology: From Fundamental Understandings To Integrated Circuit Applications	MOE Academic Research Fund Tier 1	133,300.00	Lead Principal Investigator	01-Nov-2016	30-Apr-2019
An Integrated Platform Approach Towards Non-Invasive Continuous Blood Glucose Monitoring Addressing Clinical Need for Early Diagnosis and Improved Compliance	SMART Innovation Grant	248,500.00	Principal Investigator (Project)	01-Jul-2016	30-Jul-2017
An Integrated Platform Approach Towards Non-Invasive Continuous Blood Glucose Monitoring Addressing Clinical Need For Early Diagnosis And Improved Compliance		248,500.00	Lead Principal Investigator	01-Jul-2016	30-Jul-2017
Circuit Design for GaN Based DC-DC Converter Power Supply	Global Foundries Singapore Pte Ltd	121,800.00	Principal Investigator (Project)	01-Jun-2016	31-Dec-2019
10GiFi Research & Development of Ultra-wideband RF Transceiver	Huawei Technologies Co Ltd	867,140.19	Principal Investigator (Project)	15-Jul-2014	14-Feb-2019
10GiFi Research & Development Of Ultra-Wideband RF Transceiver		867,140.19	Lead Principal Investigator	15-Jul-2014	14-Feb-2019
Project 2: Electronic Circuit Design, Communication	Singapore-MIT Alliance for Research and Technology (SMART) Centre	836,400.00	Principal Investigator (Project)	01-Apr-2014	31-Mar-2016
Project 2: Electronic Circuit Design, Communication		836,400.00	Lead Principal Investigator	01-Apr-2014	31-Mar-2016
SMA Graduate Fellowship Research Supplement -Sharma Sunny	SMA Graduate Fellowship Research Supplement	97,192.25	Principal Investigator (Project)	13-Jan-2014	12-Jan-2018
Admission year: Jan 2014		94,892.08	Lead Principal Investigator	13-Jan-2014	12-Jan-2018
SMA Graduate Fellowship Research Supplement -Yu Haohong	SMA Graduate Fellowship Research Supplement	89,173.31	Principal Investigator (Project)	05-Aug-2013	04-Aug-2017
High Thermal Resolution Ultra-Low Power Integrated Imager: Fund. Issues in CMOS	AcRF Tier 2	885,352.00	Principal Investigator (Project)	01-Jul-2013	30-Sep-2016

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IPs in RF IC.

Patents (For multi-company patents, only one is shown here randomly)

1. *Qiu Ping, **C.C. Boon**, Chew Kok Wai, Yeo Kiat Seng, Do Manh Anh, Chan Lap and Lim Suh Fei, "Tunable high quality factor inductor", Patent number (US patent issued) 8237531, Aug. 2012. (CSM)
2. **P. Choi, S. Goswami, **C. C. Boon**, L. S. Peh, H-S. Lee "A Fully Integrated RF Front-End for High Power Wireless Applications". US Provisional Application No.:62/003574. June. 2014.
3. Sunny Sharma, C.C Boon, Lin Jiafu, "Server Apparatus and Wearable Device for Blood Glucose Monitoring and Associated Methods", PCT Application No: 11201704055Y, Filing Date 18 May 2017.
4. **M. D. Mao*, **C. C. Boon**, **P. Choi, L. S. Peh, "DC-DC Converter and Power Amplifier". STLO Ref: US Provisional Patent Application No. 62/256,535, Nov. 2015.
5. D. Ezri, S. Shilo, **X. Yi, **C. C. Boon**, "A Communication Transmitter and Method", European Patent Office, PCT/EP2015/063511, publication date 22 Dec. 2016.
6. *Sunny Sharma, C.C Boon, "Analog-to-Digital Converter", Grant, Patent No. 9742424, 22 August 2017.
7. D. Disney, **C. C. Boon**, F. Meng, **X. Yi, "Integrated DC-DC Boost Converter with Gallium Nitride Power Transistor", US Patent Application 20190020272, 7 Dec. 2017.
8. Miao Yannan, Yi Xiang, Yang Kaituo and Wen Zhencai. "Voltage-controlled Oscillator, Quadrature Voltage-Controlled Oscillator and Communication System," CN106921345A, July 2017 (Publication date)
9. Miao Yannan, Yi Xiang, Yang Kaituo and **Wen Zhencai**. "Complex Impedance Network Suitable for Dual Band Carrier Aggregation," CN107040239A, Aug. 2017 (Publication date).
10. Yi Xiang, Yang Kaituo, **Boon Chirn Chye** and Miao Yannan. "Low-Noise Amplifying Circuit and Receiver," WO2018040521, Aug. 2018 (Publication date).
11. Devrishi Khanna, Yang Kaituo, Wang Xiaoying, **Boon Chirn Chye**, Zhang Junping and Liang Dong, "Low-Noise Negative Voltage Stabilizer," CN110531817A, Dec. 2019(Publication date).
12. Yang Kaituo, **Boon Chirn Chye**, Cheng Qianfu and Zhang Junping. "Receiver and Low-Noise Amplifier," WO2020140918, Sep. 2020 (Publication date).
13. **P. Choi^, **C. C. Boon**, L. S. Peh "DC-DC Converter with Embedded Clock". PCT 62/296702, Taiwan Patent Application No. 106105280. March. 2017.
14. **Zhipeng Liang, Chirn Chye Boon, Xiang Yi, and Jack Sheng Kee, "Time-to-digital converter," Grant, 27 August 2019 (DE).
15. **D. Khanna, **C. C. Boon**, K.T. Yang and K. J. Sheng, "Charge-Based Charge Pump ith Wide Output Voltage Range", Grant, patent number 10707750, 7 July 2020 (DE).
16. **K.T. Yang, **C. C. Boon**, D. Khanna and K. J. Sheng, **, "Low Noise Amplifier", Grant, patent number 10659011, 19 May 2020 (DE).
17. **C.Y. Li, **X. Yi, **C. C. Boon**, J.P. Zhang, "一种功率检测器", ID85533667CN01, China Patent Application number 201711148084.3, Filed Date 17 Nov. 2017.
18. **K.T. Yang, **X. Yi, **C. C. Boon**, J.P. Zhang, "Signal Receiving Circuit, Signal Processing Chip, Communications Device, and Signal Receiving Method", Patent number 11128333, Grant, 21 September 2021 .
19. **P. Choi, D. Antoniadis, **C. C. Boon**, E. A. Fitzgerald "Apparatus and Method for Wireless Communication". The PCT Application No. PCT/SG2019/050262, 10 May 2019.
20. **P. Choi, D. Antoniadis, **C. C. Boon**, E. A. Fitzgerald "Apparatus and Method for Wireless Communication". European National Phase Application No.: 198032435, Japanese National Phase Application No.: 2020-564218, Nov 2020. Published Number and Date: 2021-523646 - 09/02/2021.
21. **K.T. Yang, **C. C. Boon**, **T. Guo, Y.T. Dong, "Current-Mode Receiver Architectures with High Linearity", NTU Ref: 2021-219-01-SG PRV, provisional patent application number 10202104946R, Filed Date 14 May. 2021. (CV2X)
22. **T. Guo, **C.C. Boon**, K.T. Yang, A. Zhou., "A high Q microstrip line with novel big-small-holes periodically perforated ground metal in CMOS process", NTU Ref:2021-037-01-SG PRV, provisional patent application number 10202102018P, Filed Date 26 Feb. 2021 (CV2X).
23. **Y.T. Dong, **C.C. Boon**, K.T. Yang., "Dual-Path Sub-Sampling PLL with Feedback Phase Noise Cancellation Technique Inventors", Singapore provisional patent application number 10202109804S, Filed Date 7 Sep. 2021 (CV2X).
24. **P. Choi, **C. C. Boon**, L. S. Peh "High Voltage Logic Circuit", patent number 10923473, Grant, 16 Feb. 2021 (LE)
25. **Y.T. Dong, **C.C. Boon**, Z. Liu, Z.J. Yang., "In-Phase Injection-Coupled Quadrature Voltage-Controlled Exploiting Negative Resistance Based Coupling Cell", Singapore provisional patent application number 10202113360R, NTU REF: 2021-521-01-SG PRV, Filed Date 2021 (MOE T2).

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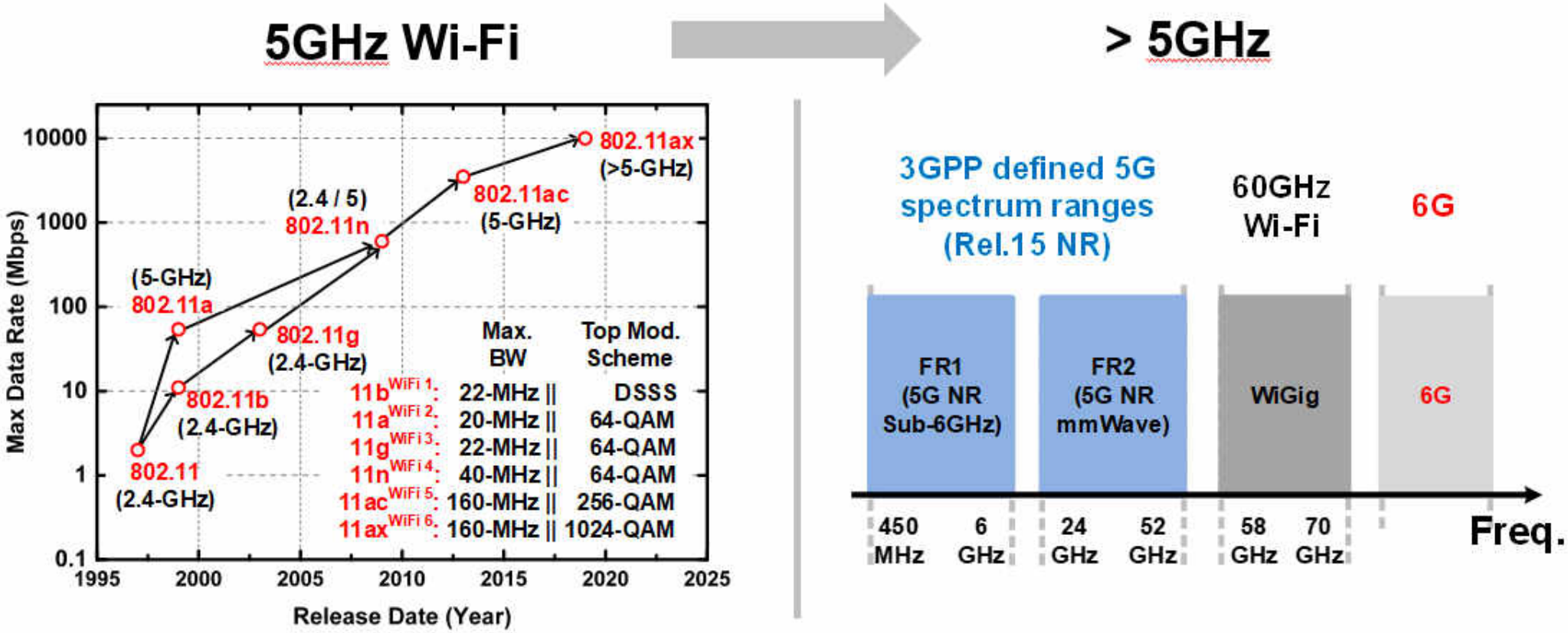
RF CMOS Receiver Front-End (ISSCC 2021)



Better sensitivity / Further coverage in demand!

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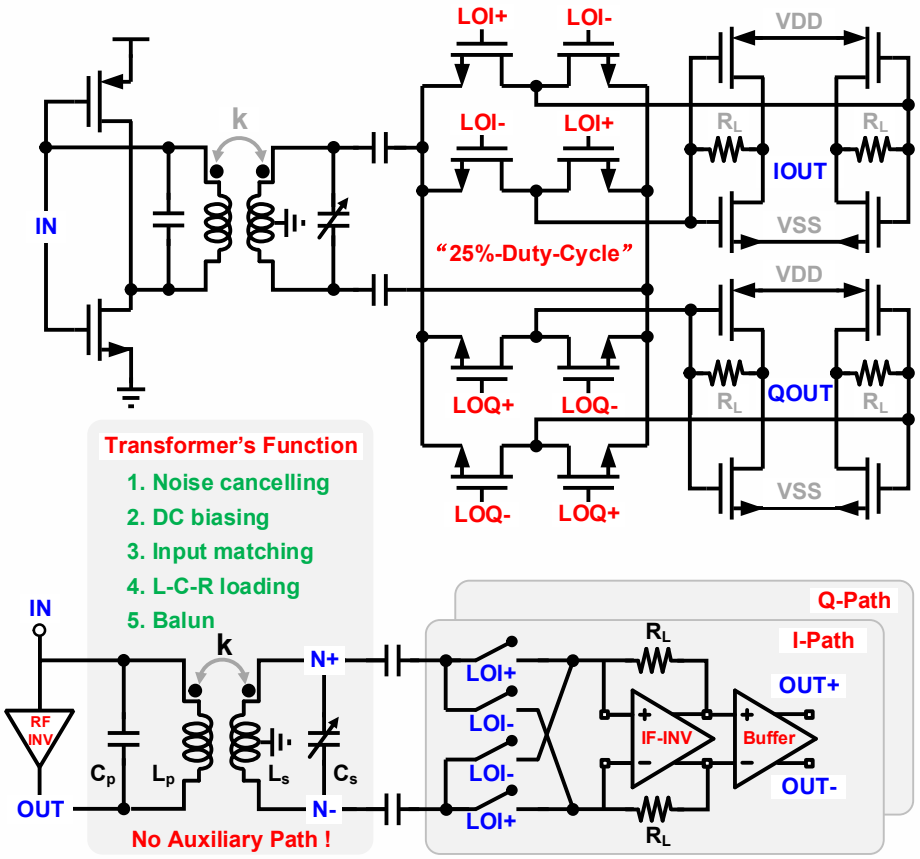
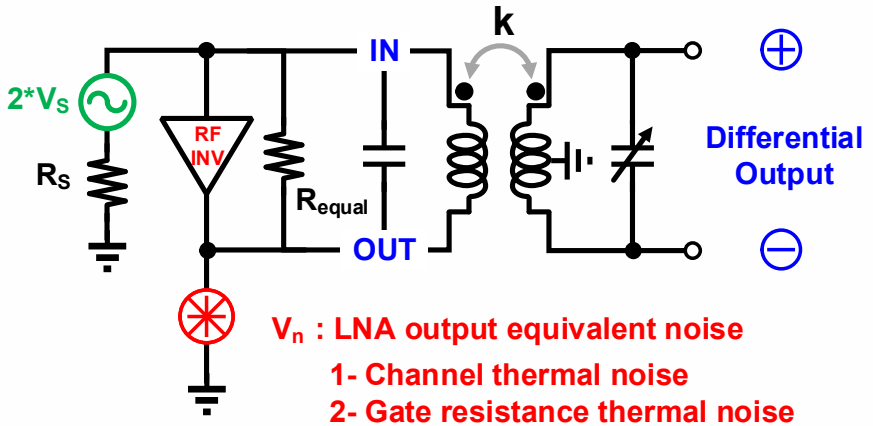
REF 1: K.T. Yang, C. C. Boon, ISSCC 2021

RF CMOS Receiver Front-End (ISSCC 2021)





	IN	OUT	Diff. Output
Signal	V_s	$-A_v V_s$	$(1+A_v)V_s$
Noise	αV_n	V_n	$(1-\alpha)V_n$
	$\alpha = R_s/(R_s + R_{equal})$		

Transformer-based noise-cancelling without Aux-Path.
Transformer provides multiple advantages:
DC biasing / L-C-R loading / Input matching / Noise cancelling / Passive balun.
Achieves a noise figure of 1.75dB with 25mW at 5GHz.
Suitable for frequencies larger than 5GHz.

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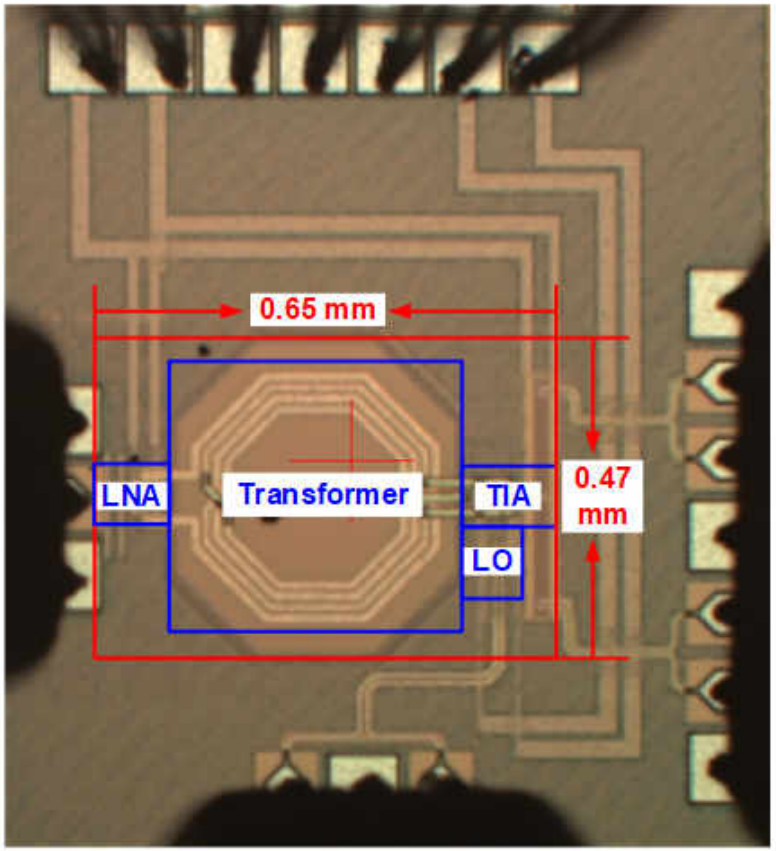
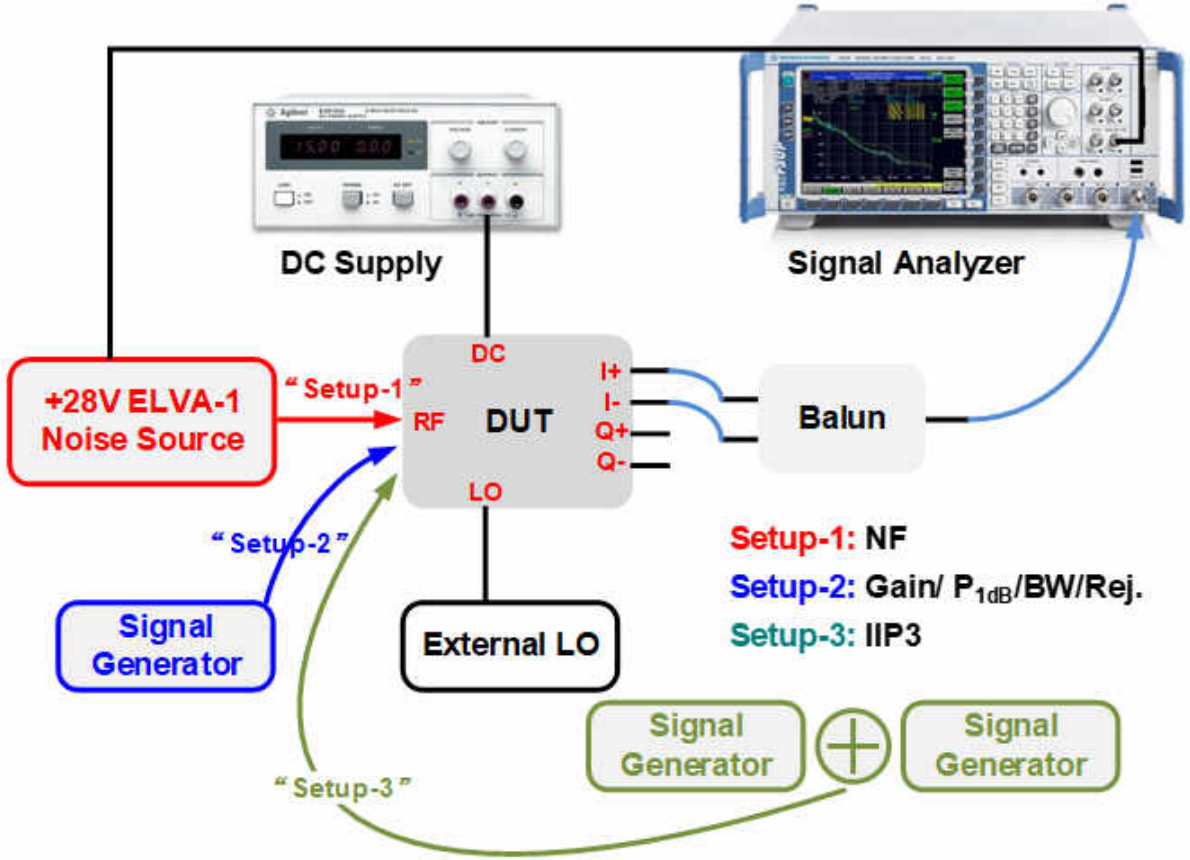
REF 1: K.T. Yang, C. C. Boon, ISSCC 2021

RF CMOS Receiver Front-End (ISSCC 2021)





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REF 1: K.T. Yang, C. C. Boon, ISSCC 2021

RF CMOS Receiver Front-End (ISSCC 2021)

	[5]	[6]	[1]	[4]	This Work
Architecture	LNA+Gm	LNA+Gm	FTNC	IND-NC	TBNC
RF Frequency [MHz]	5100-5900	100-2800	80-2700	5000	4500-5500
Gain [dB]	18/39	50	70	31	42
NF [dB]	1.9/2.4 @5.5GHz	1.8 @2GHz	1.9 @2GHz	1.8 @5GHz	1.75 @4.9GHz
IIP3 [dBm]	-14 **	5 *	13.5 *	-8.8 **	-11 **
Active Area [mm2]	0.56	0.8	1.2	0.62	0.31
Supply Voltage [V]	1.2	1.1	1.3	1/1.2	1.2
Current [mA]	35 (RX+LO)	22 (RX) 3-11 (LO)	24 (RX) 3-36 (LO)	21 (RX) 60 (LO)	16 (RX) 5 (LO)
CMOS Technology	65nm	40nm	40nm	65nm	40nm

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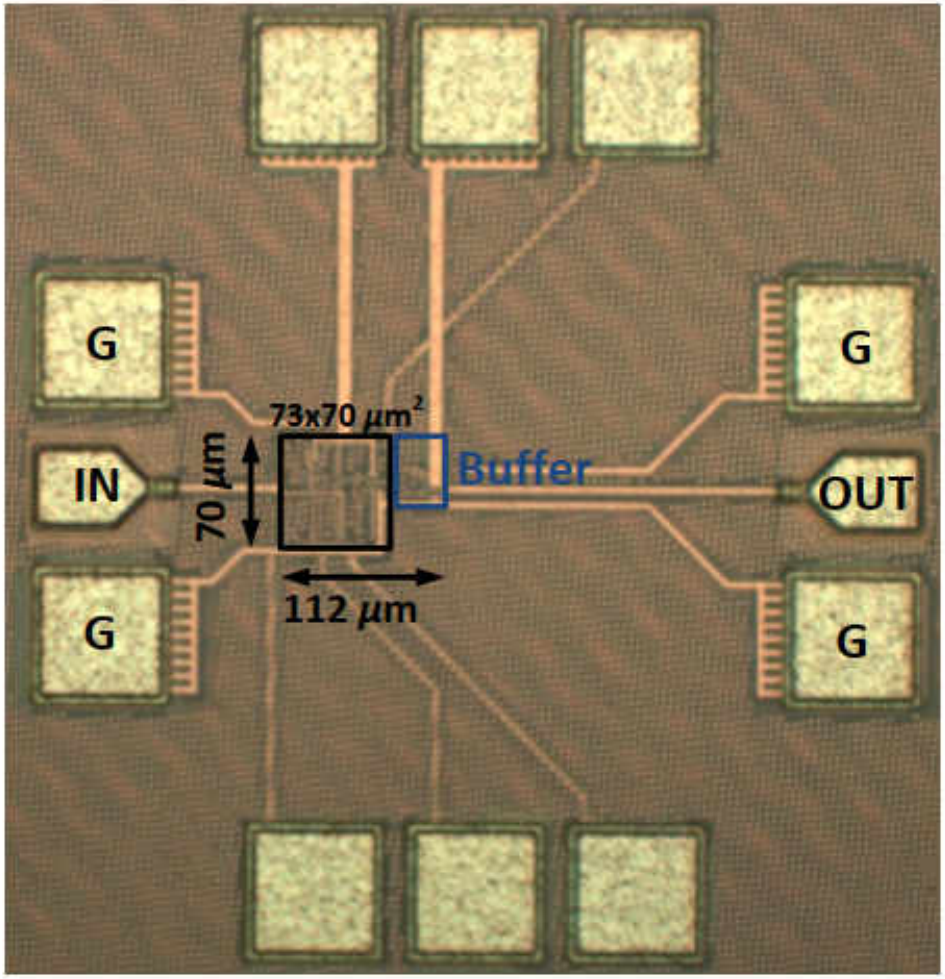
REF 1: K.T. Yang, C. C. Boon, ISSCC 2021

RF CMOS LNA (ISSCC 2022)

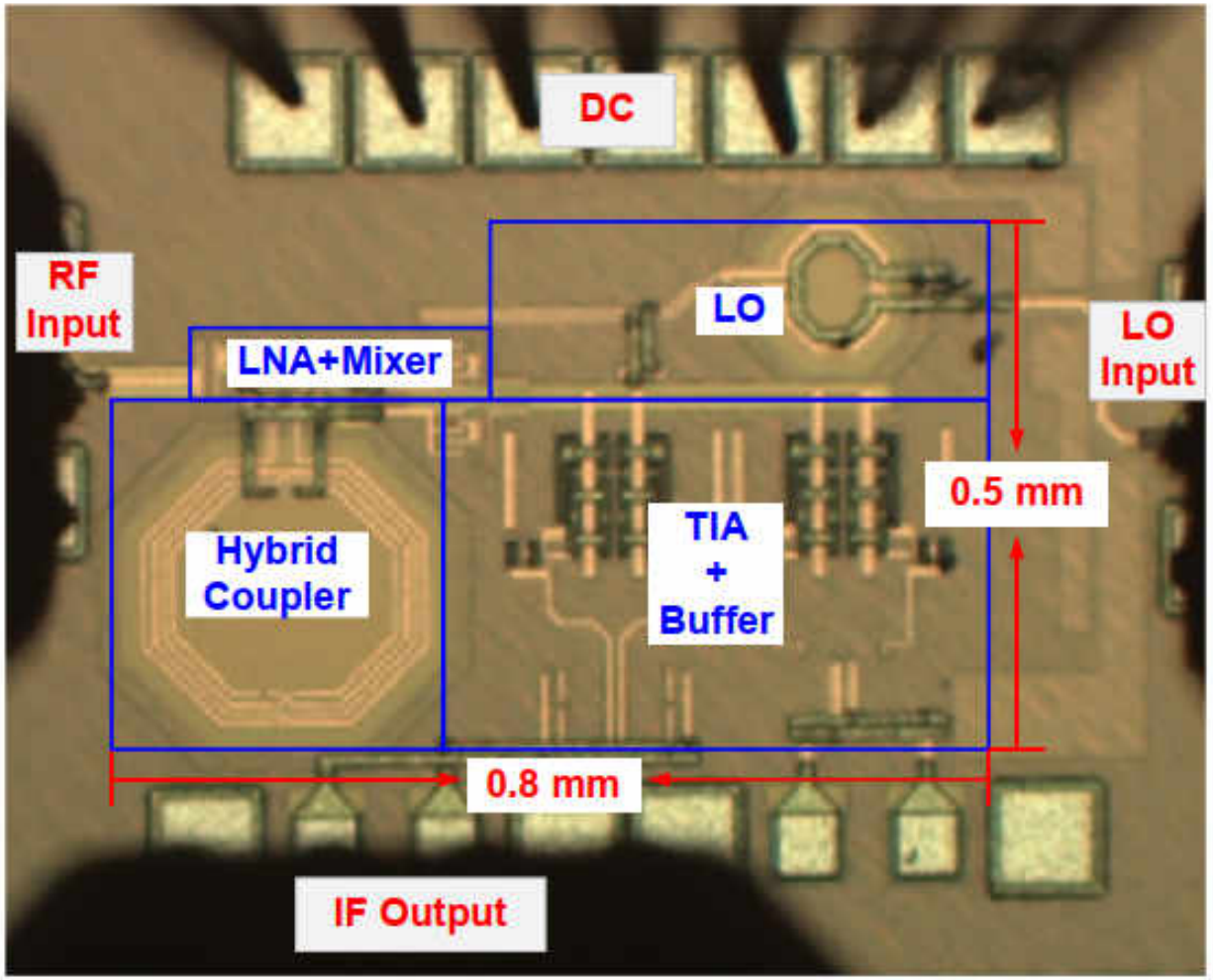


A 0.0078-mm^2 3.4-mW Wideband Positive-Feedback-Based Noise-Cancelling LNA in 28-nm CMOS Exploiting Gm-Boosting

NANYANG TECHNOLOGICAL UNIVERSITY

REF: Z. Liu, C. C. Boon, ISSCC 2022

RF CMOS Receiver Front-End (ISSCC 2022)



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REF: K.T. Yang, C. C. Boon, ISSCC 2022

Testing Results of LNA

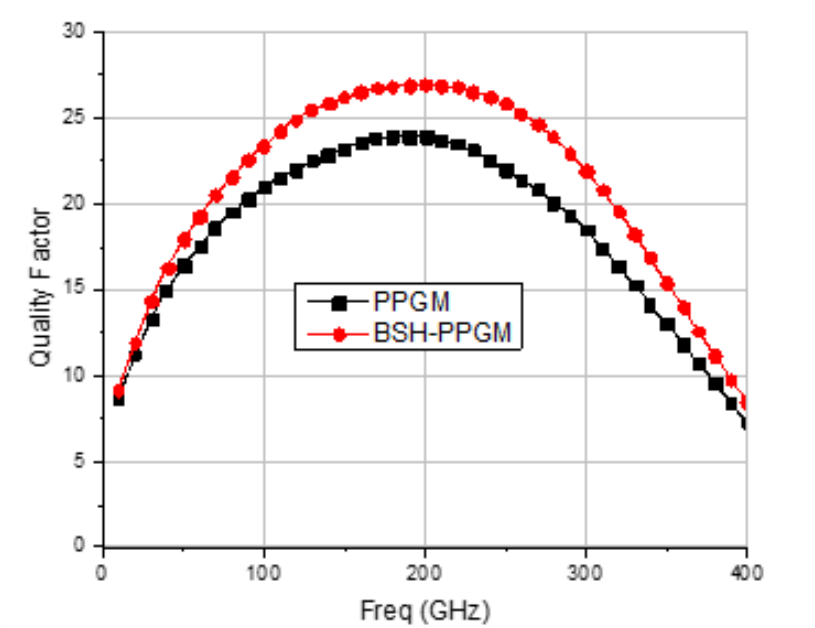
- A positive-feedback-based NC LNA with CM and active feedforward is demonstrated and tested. The POC measured results have achieved the lowest power consumption (3.4mW) while achieving highest gain (19.6dB) and smallest footprint (0.0078mm^2) with comparable NF (2.7dB) among the arts [1-4].
- This is easily translated to lowest cost for mass production with minimum power consumption among state-of-the-arts.

Testing Results of Receiver

- This work presents several current-mode receiver architectures with no LNA employed, which combines the advantages of conventional current-mode and mixer-first architectures, creating low input impedance at both RF and IF input.
  The measured POC receiver has achieved a high In-band (IB)-IIP3 in current-mode and the lowest NF at 5GHz in voltage-mode, where the core circuit occupies a smallest area of 0.4mm2 among similar works. The low NF and high gain at voltage mode as well as high IB-IIP3 and low power at current mode makes it a high performance and highly versatile receiver.

- **Both works are accepted for ISSCC 2022, which is known as the Olympic of IC design. Note that in 2022, 4 ISSCC papers accepted from Singapore (from both industry and academia), where these are the 2 from NTU.**

6G & Beyond- Metal Fill to Improve Q and for Tuning @ mmW & THz



This invention is applied to RF/MMIC designs especially to high frequency circuits in 6G applications where quality factor is extremely tough. It can be used in other processes where both metal density and quality factor performance are required and can also be used to tune the bandwidth of the circuit passband and stopband in 5G/6G applications. Firstly, this invention can improve passive devices quality factor by optimizing ground metal structure by 12% without adding additional manufacturing cost, to improve their passive device models. Secondly, this invention can be used in RF/mm-Wave circuits where passive devices are used.

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REF: T. Guo, C.C. Boon, K.T. Yang, A. Zhou., "A high Q microstrip line with novel big-small-holes periodically perforated ground metal in CMOS process", NTU Ref:2021-037-01-SG PRV, provisional patent application number 10202102018P, Filed Date 26 Feb. 2021

6G & Beyond- Metal Shape for Low Loss @ mmW & THz

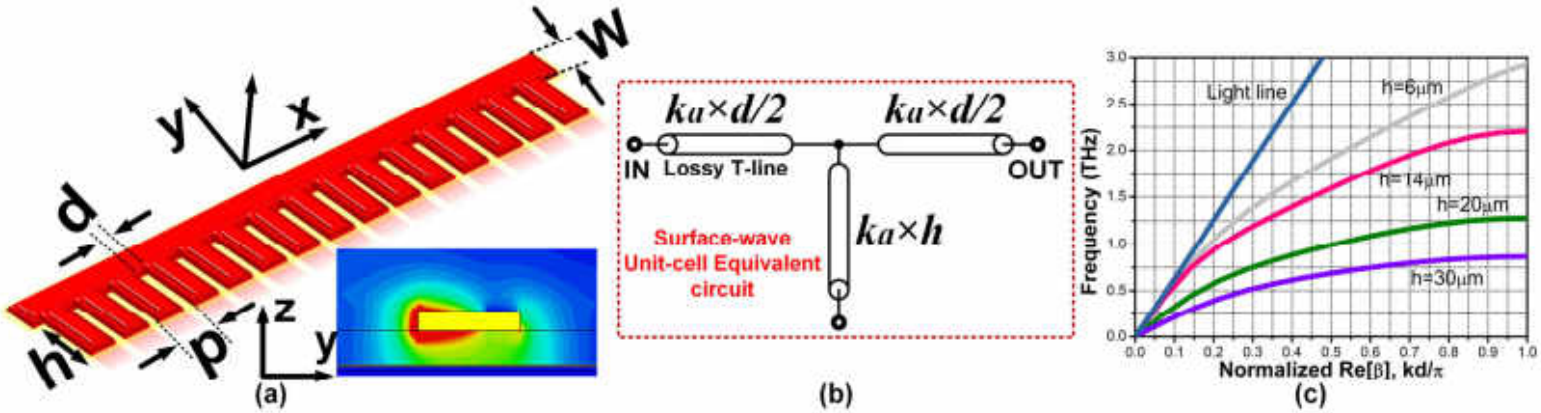

Fig. 3. (a) 3-D view of the spoof SPPs metawaveguide and the simulated *E*-field distribution at the *yz* plane. (b) Modeling of metawaveguide unit-cell by a proposed lossy T-section equivalent circuit. (c) Eigenmode simulation result of dispersion relationship.

B. Modeling of Spoof SPPs Metawaveguide

SPPs propagating at the flat interface between a real metal and a dielectric medium are inherently 2-D EM waves. Localization of SPPs is possible since the wavevector in the dielectric is much smaller than the wave propagation constant, resulting in evanescent field decay on both sides of the interface [14]. As depicted in Fig. 3(a), by corrugating periodic sub-wavelength metal strips onto the conventional waveguide, highly localized SPPs can be established and propagated on flat metals and dielectric [15]. The near-field results evaluated on the *yz* plane in Fig. 3(a) show that the EM energy can be constrained into a volume much smaller than the diffraction limit $(\lambda_0 / 2n)^3$, where $n = \sqrt{\varepsilon}$ is the refractive index of the dielectric medium. With the field enhancement, the condensed *E*-field localization enables on-chip low loss and low crosstalk transmission in the sub-THz region.

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REF: Y. Liang, **C. C. Boon**, IEEE Transactions on Microwave Theory and Techniques, accepted, Oct. 2022. TSMC 65nm RFCMOS.

6G & Beyond- Cross-talk & effect on gain & Noise of Metal @ mmW & THz

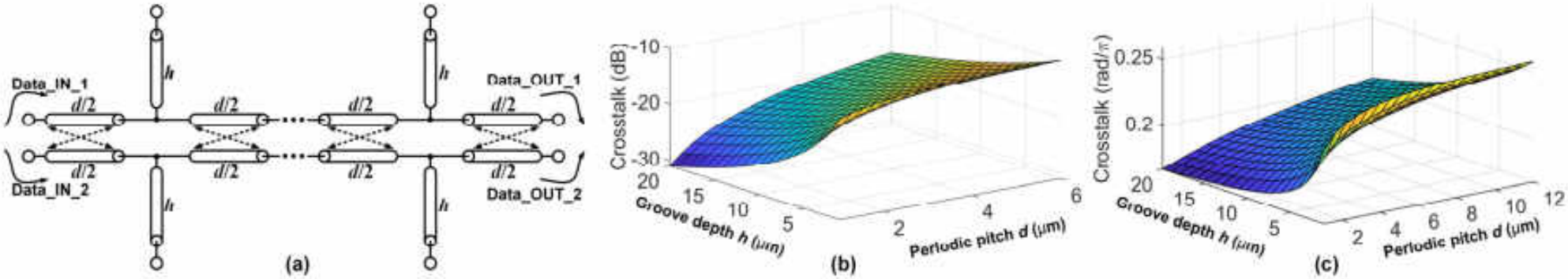

Fig. 4. (a) Coupled T-section model developed to estimate the crosstalk effect of the two closely packed SPPs metawaveguides. Analytical (b) crosstalk magnitude (dB), and (c) coupling phase (rad/π) with respect to h (μm) and d (μm).

EM coupling between traces introduces a coupled phase shift, as illustrated in Fig. 4(c). Similarly, the coupled phase shift can be manipulated by both d and h. Such a slow-wave property is particularly interesting for scenarios where a specific coupled phase shift is required, but the effective coupled-line length is fixed for maintaining the minimum footprint. This result has been applied to the coupled oscillator for in-phase power combining within a smaller area (Section III. B).

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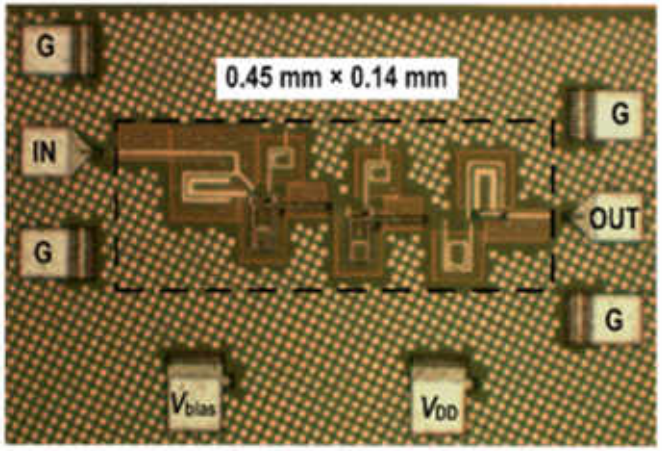
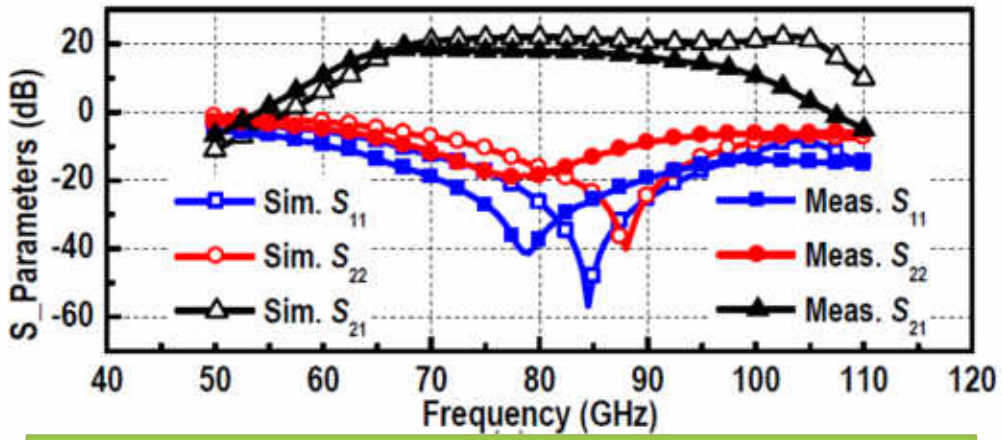
REF: Y. Liang, **C. C. Boon**, IEEE Transactions on Microwave Theory and Techniques, accepted, Oct. 2022. TSMC 65nm RFCMOS.

6G & Beyond: Widest Bandwidth Highest BWER 100GHz LNA

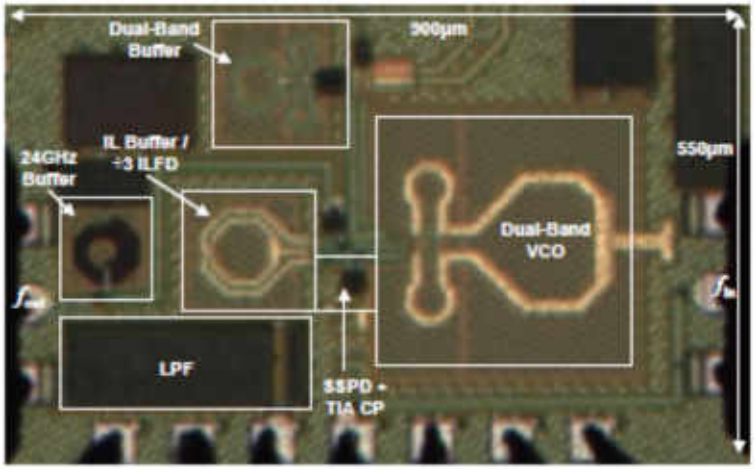




Overcoming Gain Flatness, Wideband Gain Trade-off for MMW Application.
G.Y. Feng, **C.C. Boon, IEEE JSSC, 2017**

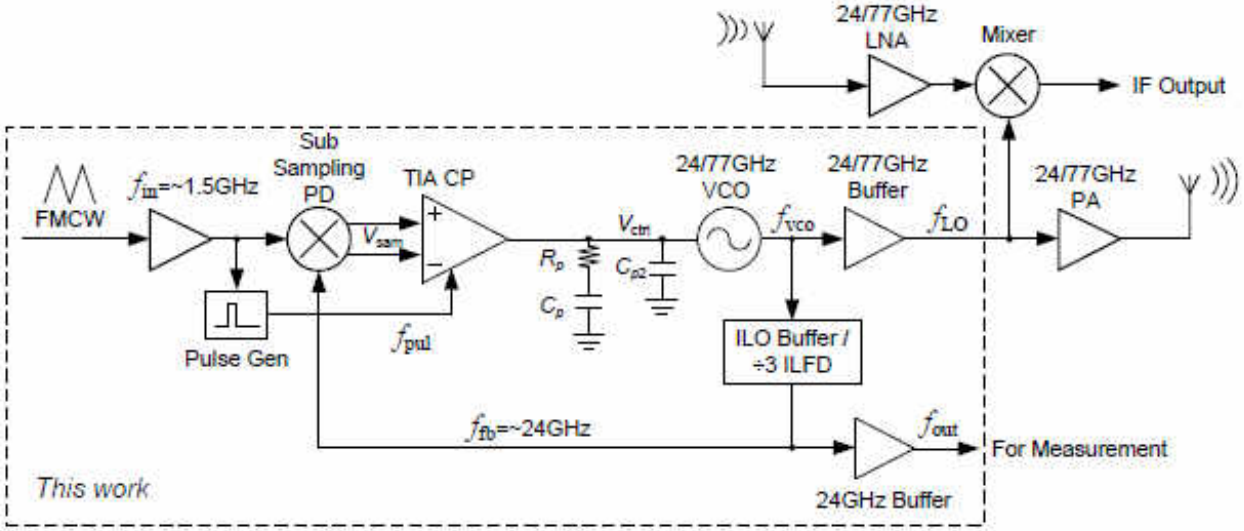
	[4] TMTT 2012	[5] TMTT 2015	[6] ISSCC 2010	**This Work**
Technology	45nm SOI CMOS	28nm CMOS	65nm CMOS	**65nm CMOS**
Topology *	3-stage CS	2-stage Cas.	3-stage Cas.	**3-stage Cas.**
Power Gain [dB]	10.7@95GHz	13.8@66GHz	17.5@77GHz	**18.5@67GHz**
BW ** [GHz]	18	18	17 #	**30**
NF_{min} [dB]	6.0	4.0	7.4	**6.1**
P_{1dB} ## [dBm]	N/A	-12.5	-22.0	**-11.8**
P_{DC} [mW]	52	24	30	**27.4**
Size [mm²]	0.32	0.38	0.37	**0.24**
FoM † [GHz/mW]	0.40	2.43	0.95	**3.00**

MM-Wave RFIC: 24/77GHz Dual-Band vehicle FMCW Radar



←Best phase noise
← Best power efficiency

X. Yi, C. C. Boon, "Low Phase Noise Dual-Band Sub-Sampling Phase-Locked Loops". US Provisional Application & IEEE Access 2019.



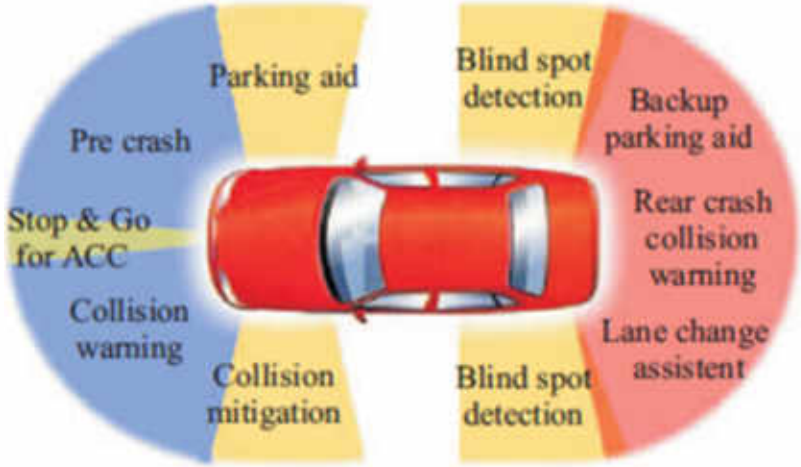


Fig. 1. Automotive radar applications

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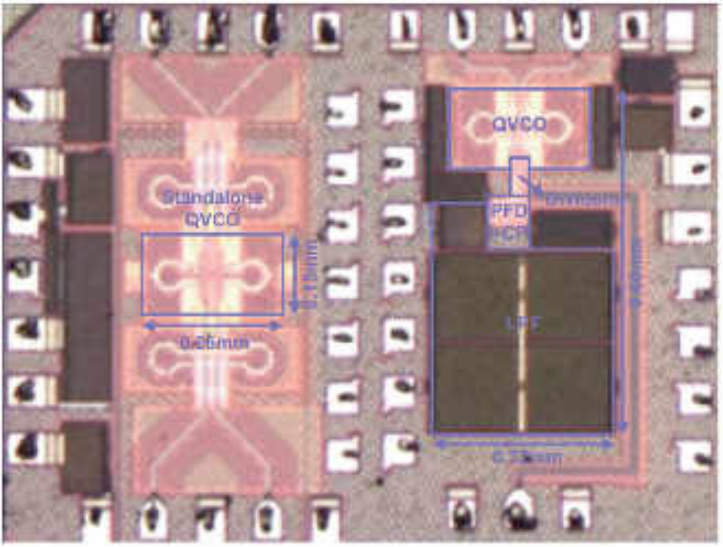
MM-Wave RFIC: 57.9-68.3GHz PLL (ISSCC)



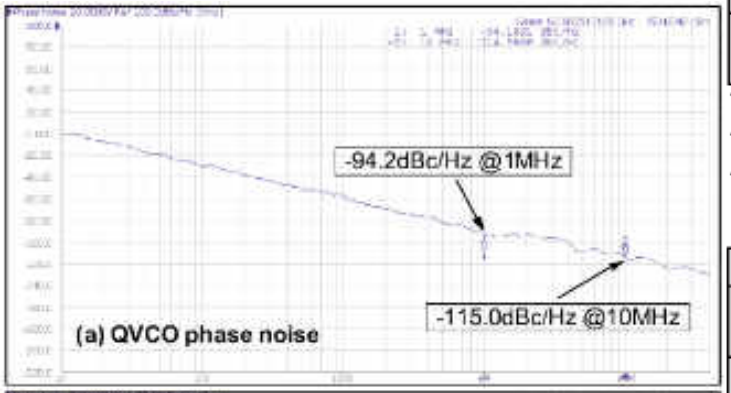
REF 2: X. Yi, C. C. Boon, et al. ISSCC. Fast settling due to high reference freq., Ultra low phase noise (low jitter), energy efficiency.

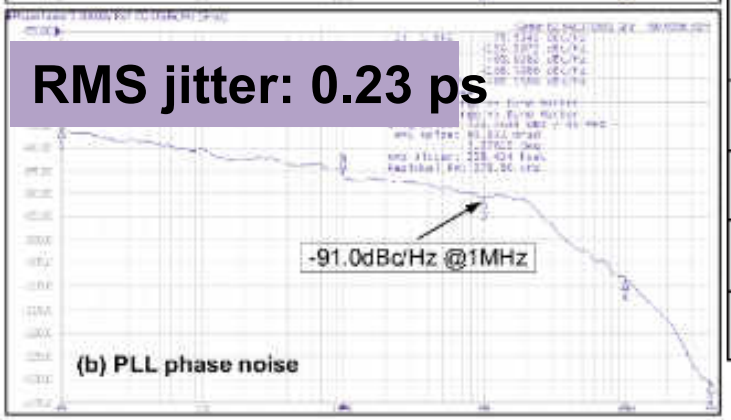
60GHz Quadrature VCO Comparison								
Ref.	Tech. (nm)	V_{DD} (V)	Operating Range (GHz)	P.N.@1MHz (dBc/Hz)	FOM* (dBc/Hz)	FOM_T** (dBc/Hz)	Phase Error	Power (mW)
[2]	65 CMOS	1.0	56.0~60.4 (7.6%)	-95/-97	-176.9/ -178.9	-174.6/ -176.6	<1.5°	22
[4]	45 CMOS	1.1	57~66 (14.6%)	-75***	-156.3	-159.6	n.a.	28
This work	65 CMOS	1.2	57.88~68.33 (16.6%)	-94.2	-179.6	-184.0	<0.7°	11.4

* FOM = P.N. – 20log($f_0/\Delta f$) + 10log(Power/1mW)

** FOM_T = FOM – 20log(% of Operating Range/10%)

*** PLL phase noise

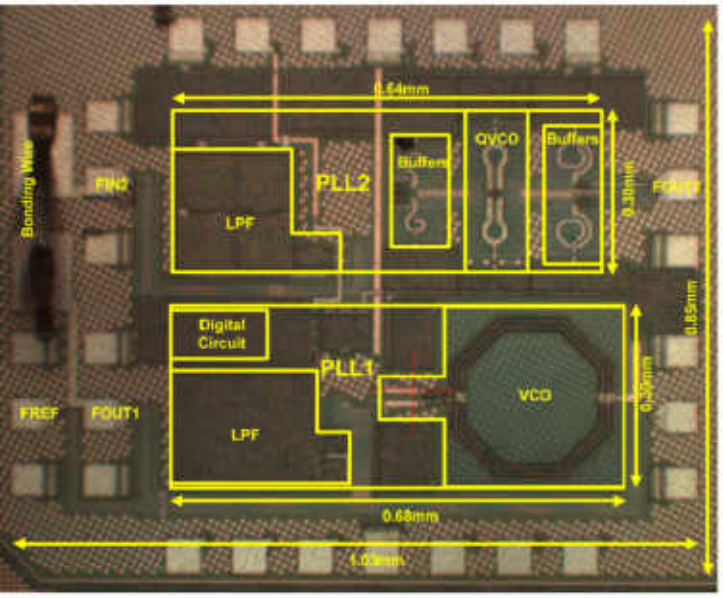




RMS jitter: 0.23 ps

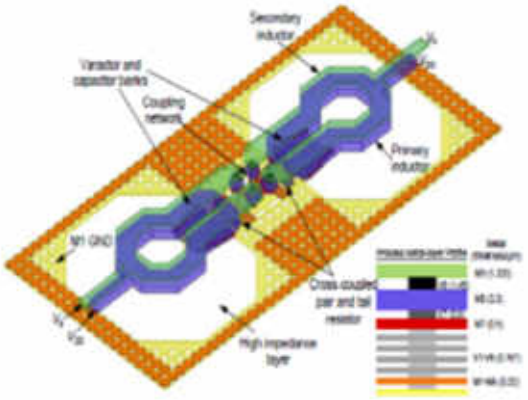
60GHz Quadrature PLL Comparison								
Ref.	Tech. (nm)	V_{DD} (V)	f_{ref} (MHz)	Operating Range (GHz)	P.N.@1MHz (dBc/Hz)	Reference Spur (dBc)	Topology	Power (mW)
[5]	90 CMOS	0.7/ 1.2	117	59.6~64.0 (7.1%)	-72.5	-23	30GHz PLL + 60GHz Hybrid	76.3
[6]	65 CMOS	1.0/ 1.2	36	54~61 (12.2%)	-94.2	n.a.	20GHz PLL + 60GHz QILO	80.9
[4]	45 CMOS	1.1	100	57~66 (14.6%)	-75	-42	60GHz QPLL	78
[7]	40 CMOS	1.1	20000	55~66 (18.2%)	<-96	n.a.	60GHz QILO	112
This work	65 CMOS	1.2	135	57.9~68.3 (16.5%)	-91	<-45	60GHz QPLL	24.6

6G & Beyond: World First 100GHz Fractional-N PLL in CMOS



Ultra-compact PLL
Overcoming frequency resolution, fast settling, signal purity trade-off.
X. Yi, C. C. Boon, TMTT 2019.

Ref.	Tech. (nm)	Operating Range (GHz)	P.N.@1MHz /10MHz (dBc/Hz)	FOM(1)@1MHz /10MHz (dBc/Hz)	FOM$_T$(2)@1MHz /10MHz (dBc/Hz)	Output Phase	Power (mW)
[2]	65 CMOS	98~103.3 (5.2%)	-75(3) /-112.1	-164.49/ -181.59	-158.81 /-175.91	Differential	12~21
		91.7~95.5 (4.1%)	-80(3) /-118.8	-162.79/ -181.59	-155.04 /-173.84	Eight Phases	48~85
[3]	65 CMOS	100~110 (9.5%)	-92.83 /-100(3)	-175.9 /-163.1	-175.5 /-162.7	Quadrature	54
This work	**65 CMOS**	**93.24~105.02 (11.9%)**	**-93.80 /-112.67**	**-178.6 /-177.5**	**-180.2 /-179.0**	**Quadrature**	**30**



Ref.	Tech. (nm)	f_{ref} (MHz)	Operating Range (GHz)	P.N.@1MHz /10MHz (dBc/Hz)	Reference Spur (dBc)	Resolution (MHz)	Output Phase	Architecture	Power (mW)
[4]	65 CMOS	371.5 ~377.0	95.1~96.5 (1.5%)	-76 /-93(3)	-51.8	f_{REF}	Differential	Integer-*N*	43.7
[5]	65 CMOS	185.7 ~211.9	96.8~108.5 (11.4%)	-88 /-105(3)	-40	f_{REF}	Differential	Integer-*N* + Push-Push	14.1
[6]	65 CMOS	402.6 ~408.5	103.058~104.58 (1.5%)	-80.41 /-101.08	-63.8	f_{REF}	Differential	Integer-*N*	63
This work	**65 CMOS**	**100**	**93.4~104.8 (11.5%)**	**-86.07 -86.07(4) /-108.75 -103.53(4)**	**-44.69**	**0.000036f_{REF}(4)**	**Quadrature**	**Frac-*N* + Sub-Sampling**	**57**

(1) FOM = P.N. – 20log($f_0/\Delta f$) + 10log(Power/1mW).
(2) FOM$_T$ = FOM – 20log(% of Operating Range/10%).
(3) Estimated from figures.
(4) PLL is in fractional-*N* mode.

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VIRTUS IC Design Centre of Excellence

6G and beyond: 160GHz 3.7mW Output Power Signal Source

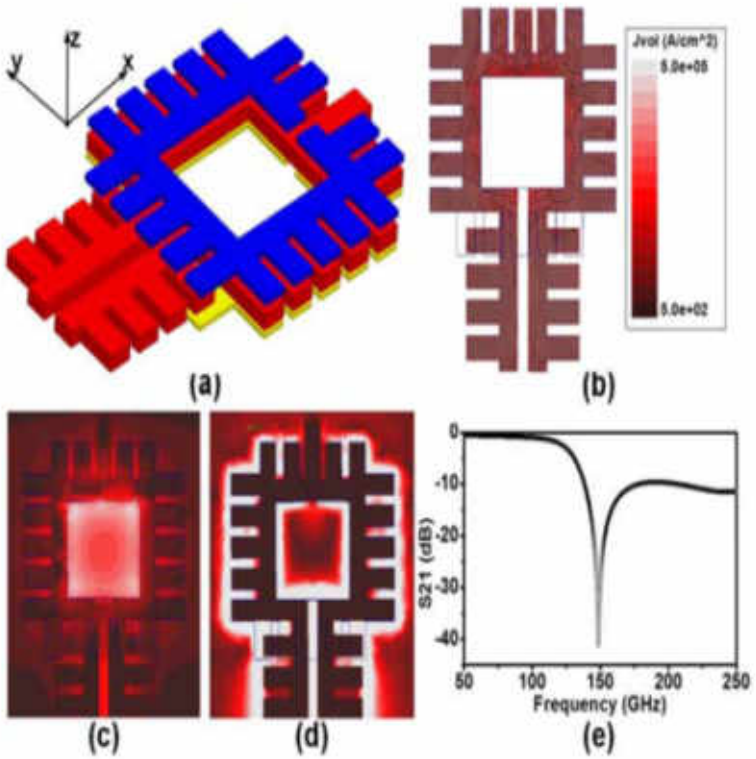


Fig. 3 (a) The proposed surface-wave resonator, the simulated (b) surface current distribution, (c) magnetic field distribution, (d) *E*-field distribution, and (e) S_{21} of surface-wave resonator.

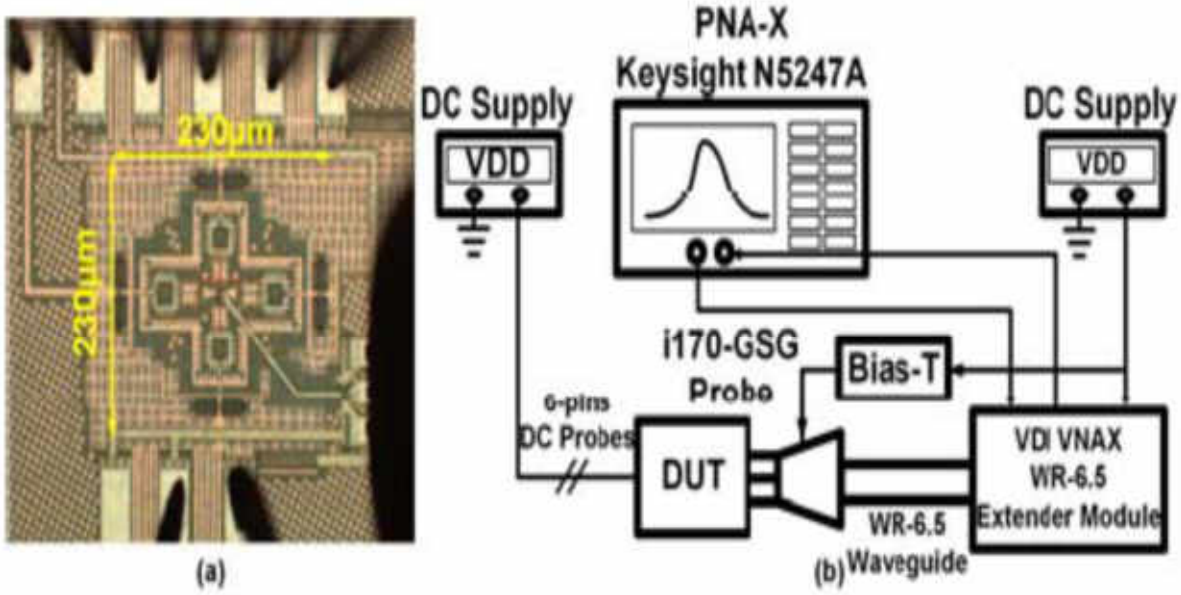


Fig. 5 (a) Die photo, and (b) the 110-170 GHz measurement setup

A 4-way surface-wave signal source is designed in 65nm CMOS at 160 GHz.
Low loss as signal source for sub-THz communication.
Measurement results 3.7 mW output power
5.5% DC-RF efficiency, 6.3% FTR and -105 dBc/Hz phase noise at 10 MHz offset, leading state-of-the-art FOM of -171 dBc/Hz and FOMT of -172.7 dBc/Hz in literature. (L. Yuan, C. C. Boon, ESSCIRC 2018)

6G & Beyond: A 311.6GHz PLL SiGe BiCMOS with -90 dBc/Hz in-band Phase Noise

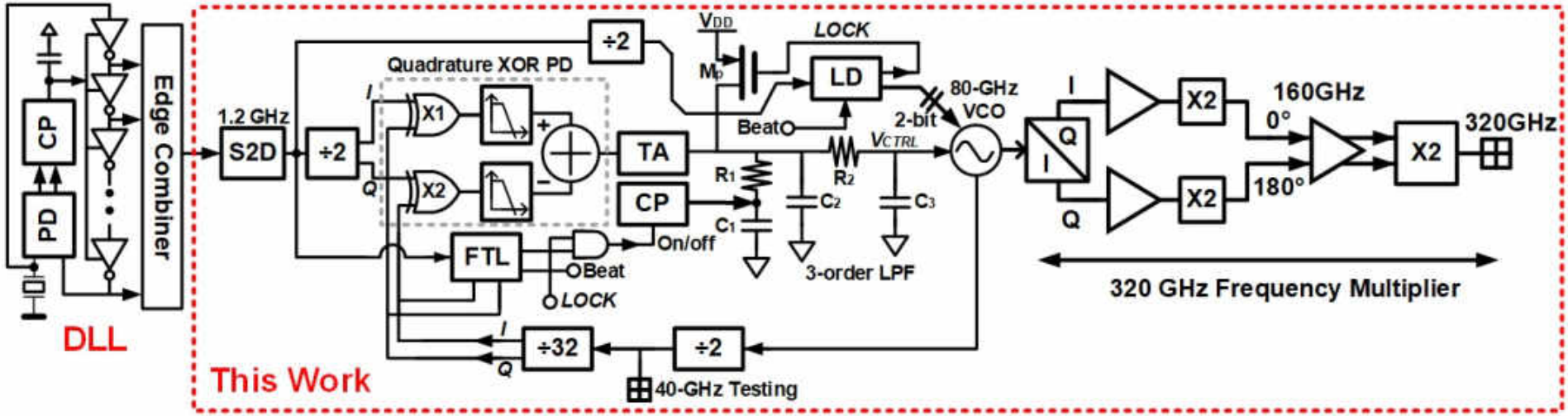


Fig. 1. Proposed 320 GHz PLL architecture involving an 80 GHz loop and a 320 GHz frequency quadrupler.

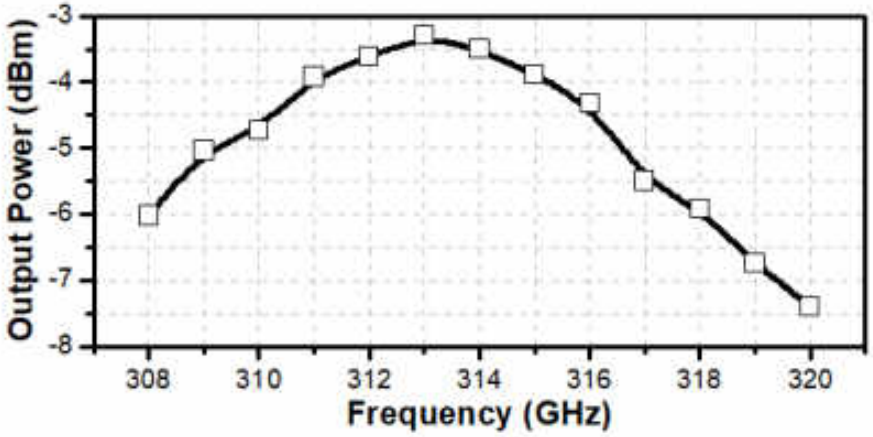
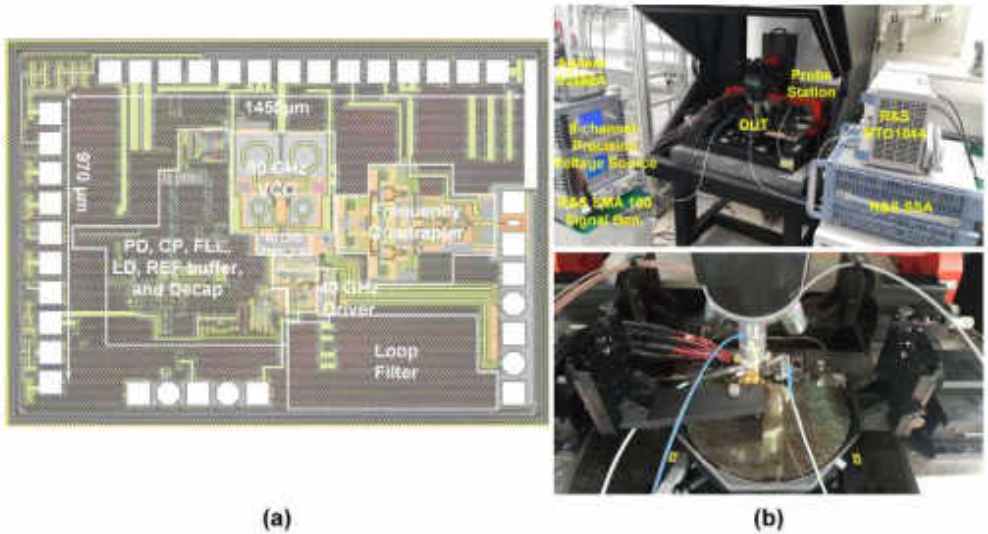


Fig. 10. Measured 320 GHz PLL probed output power.



(a) (b)

Fig. 4. Die photo of the proposed 320 GHz PLL, and (b) on-wafer testing with measurement setup.

Y. Liang, C. C. Boon, IMS 2020, USA

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Focused & Designed GaN+CMOS

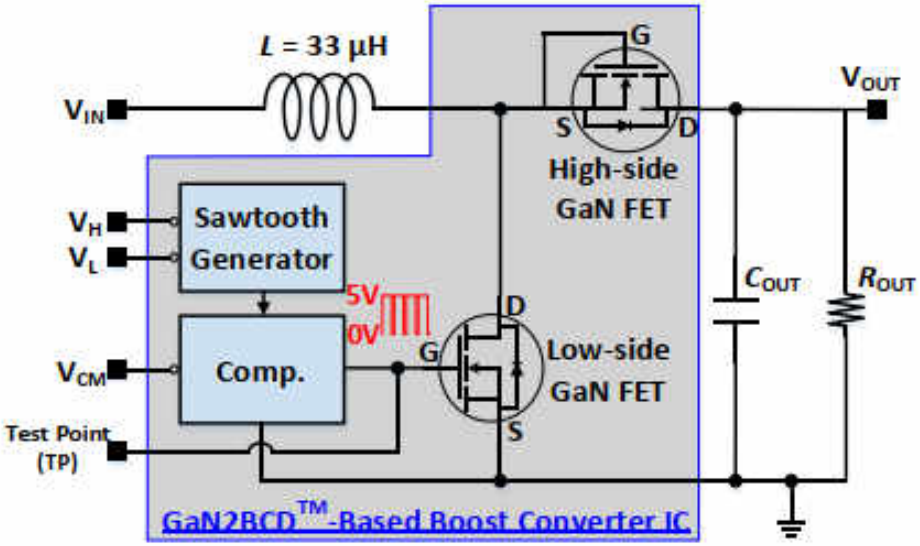
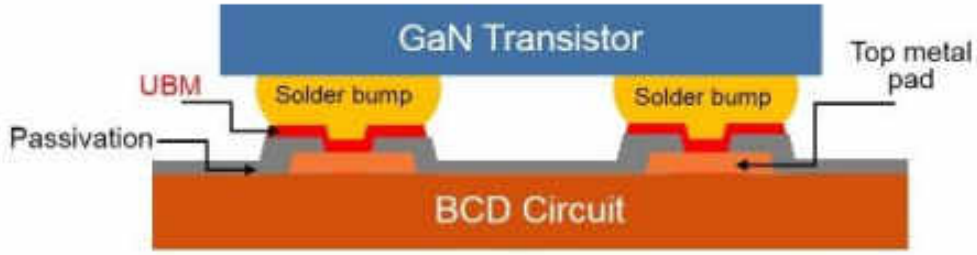


Fig. 5 Schematic of the 3.3-to-70 V boost converter prototype.



g. 1 Cross-section sketch view of the GaN2BCD™ technology.

Fig. 2 Design flow of the GaN2BCD™ technology.

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1. Donald DISNEY, **Fanyi MENG, *Xiang YI, Chirn Chye BOON, "Integrated DC-DC Boost Converter with Gallium Nitride Power Transistor, Publication number: 20190020272, Publication date: January 17, 2019. (GF).

CMOS + GaN Integrated in a Single Chip

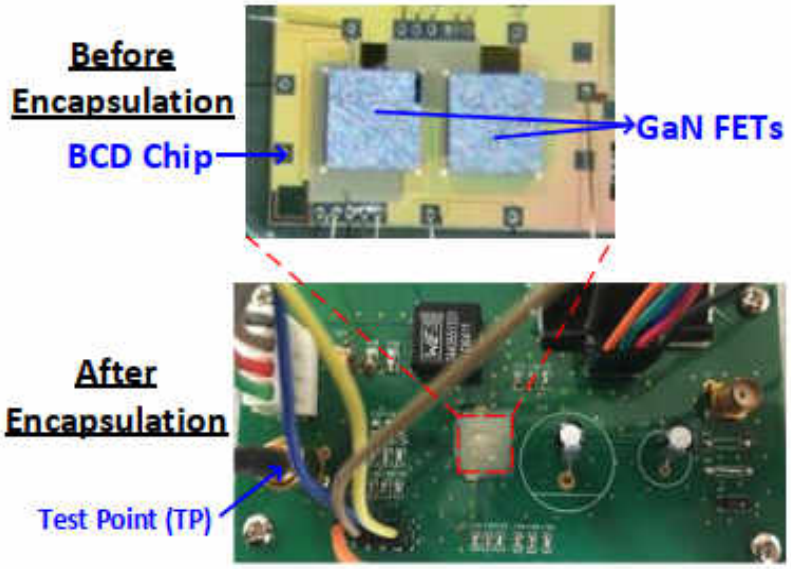

Fig. 6 Photographs of the boost converter prototype IC before encapsulation (top) and its evaluation board (bottom).

A DC-DC boost converter was designed and fabricated using the GLOBALFOUNDRIES GaN2BCDTM technology. It features direct integration of a silicon BCD control circuit with two GaN power transistors, high conversion ratio (3.3-to-70 V), large output power, high conversion efficiency, and compact size.

TABLE II
COMPARISON WITH OTHER INTEGRATED DC-DC BOOST CONVERTERS

Ref	Tech.	Boost Diode	V_{IN}/V_{OUT} (V/V)	$P_{OUT,MAX}$ (W)	η_{MAX} (%)	Area (cm×cm)
[1]	GaN + CMOS + IPD	Int. #	12/18	4.16	47.3	0.94× 0.98
[6]	80 V BCD	OTS *	3.3/80	0.35	53	0.1× 0.1
[7]	80 V BCD	OTS *	3.3/70	0.3	52	not mentioned
This Work	GaN + BCD	Int. #	3.3/70	1.68	70.3	0.32× 0.18

Integrated * Off-the-shelf

F. Meng, D. Disney,…C. C. Boon, IEEE Transactions on Power Electronics, vol. 34, no. 3, pp. 1993-1996, Mar. 2019. 2018. (I.F=6.008) DOI: 10.1109/TPEL.2018.2859419 (GF)

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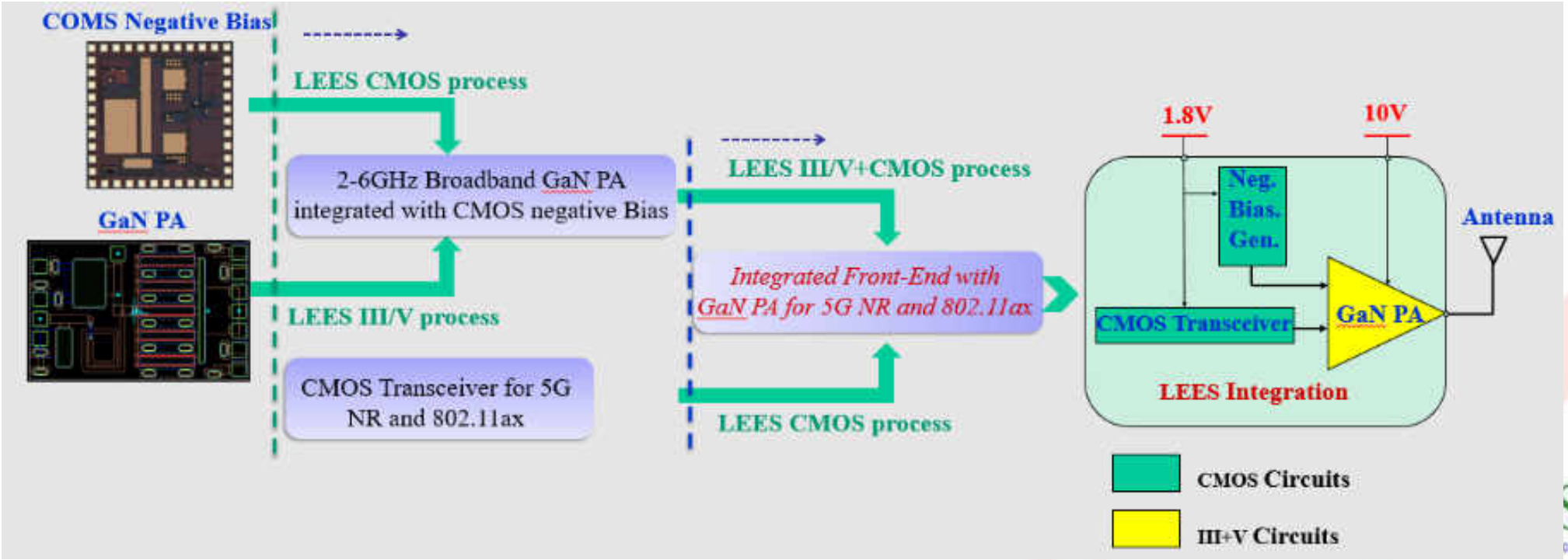
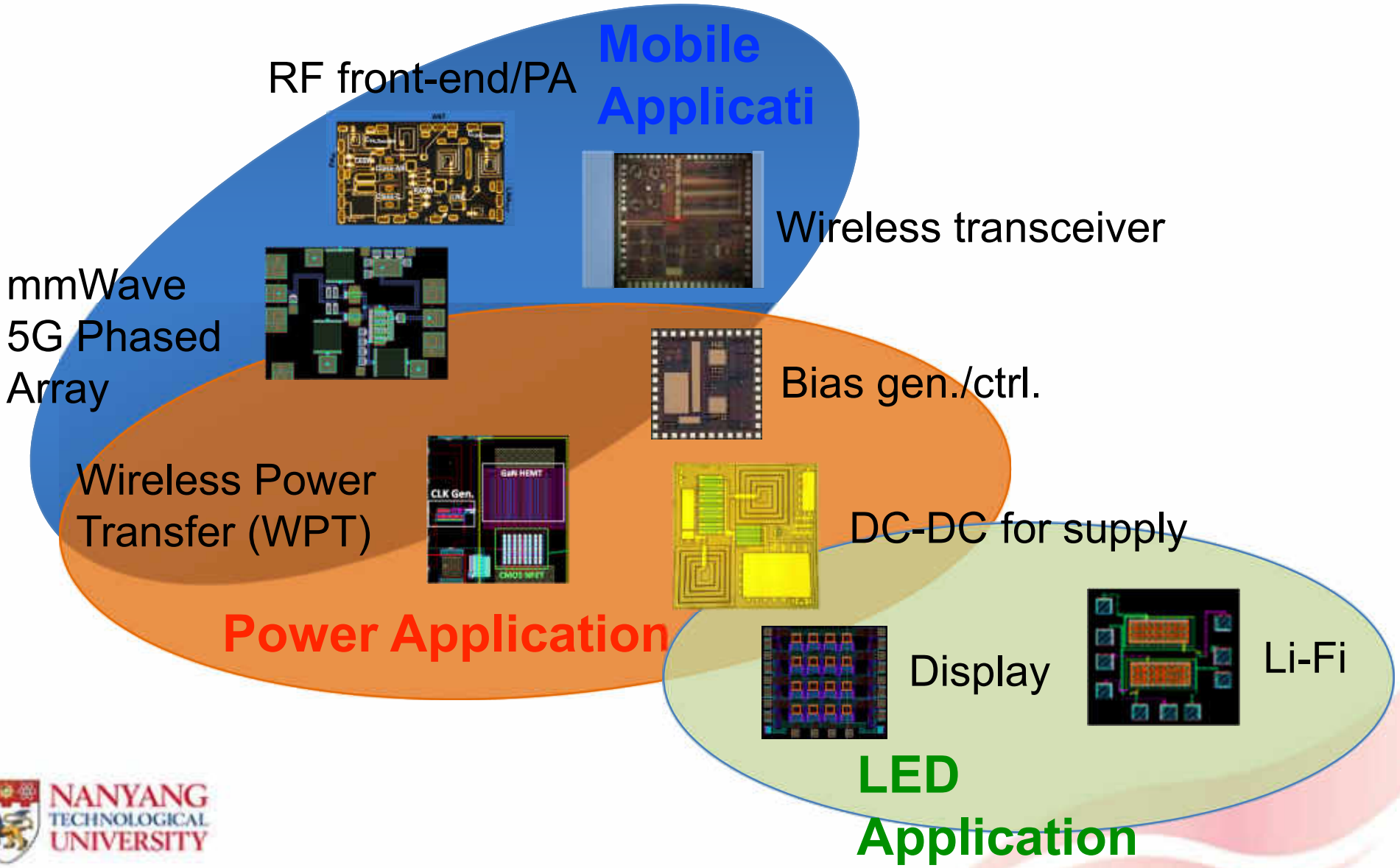
CMOS + GaN Integrated in a Single Chip

Research Direction:

- 5-6GHz CMOS transceiver for 802.11ax WLAN
- Sub-6GHz CMOS transceiver for **5G NR**
- 2-6GHz Broadband GaN Power Amplifier
- Integrated CMOS transceiver and GaN Power Amplifier in a single chip



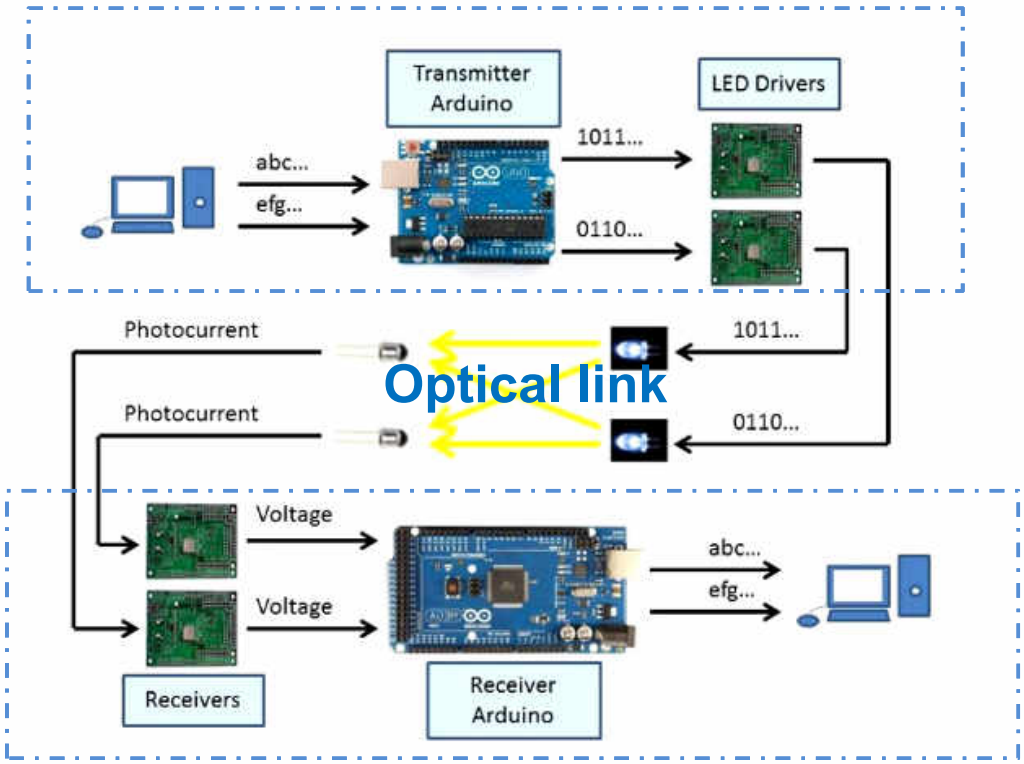
Focused & Designed GaN+CMOS



CMOS + GaN Integrated in a Single Chip

- **Recently – Work on using LEES LED in transmitter side**

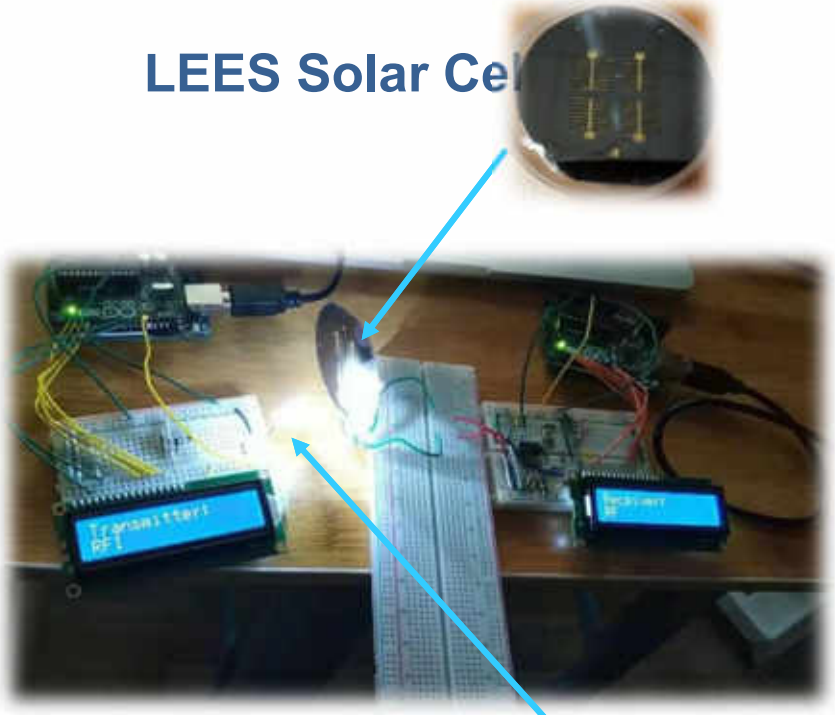
Optical Transmitter



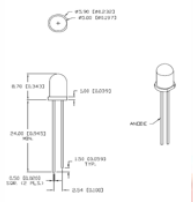
Optical Receiver

< System Level Diagram of Low Frequency Li-Fi >

LEES Solar Ce



<Previous demo using LEES solar cell>



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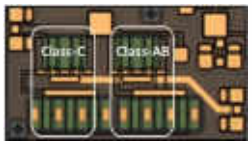
GaN Power Amplifier

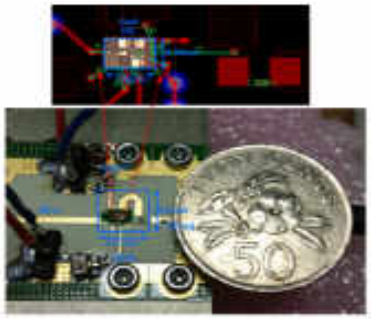
Previous Works

- Bulky module for high output power (>10W)
- Low efficiency @ low output power

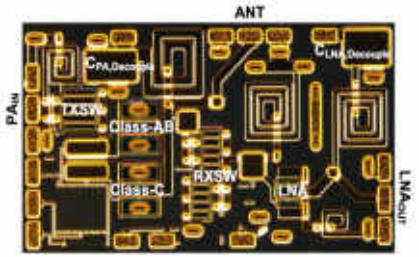
Our Works



New GaN PA topology

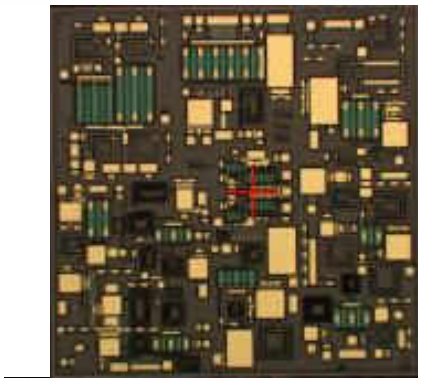


2~6GHz Wideband PA



2mm² RF front-end

Near Future



III-V+CMOS PA's for 5G

(High Power & Efficiency using LEES technology)

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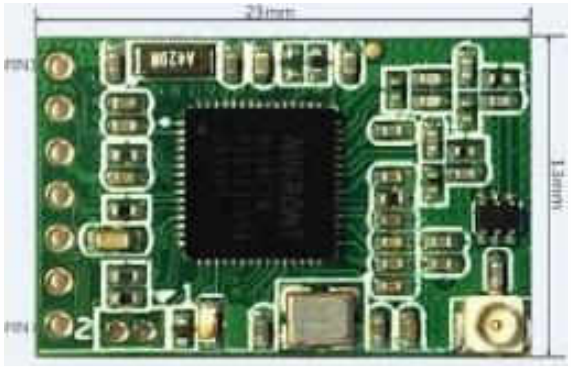
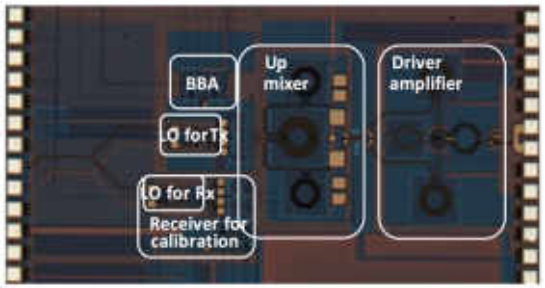
CMOS Transceiver

Previous Works

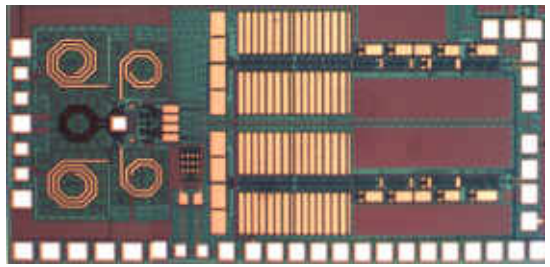


- CMOS single-chip for single RF or 2x2 MIMO
- Separate III-V for RF front-end (e.g. PA,LNA,SW)

Our Works

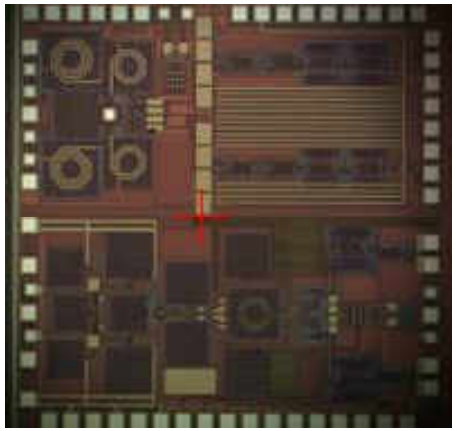


1.4mm^2 RF Tx in 0.18um GF CMOS



2.5mm^2 RF Rx in 0.18um GF CMOS

Near Future



Fully integrated 5G RF ‘array’

(High Level of Integration using LEES technology)

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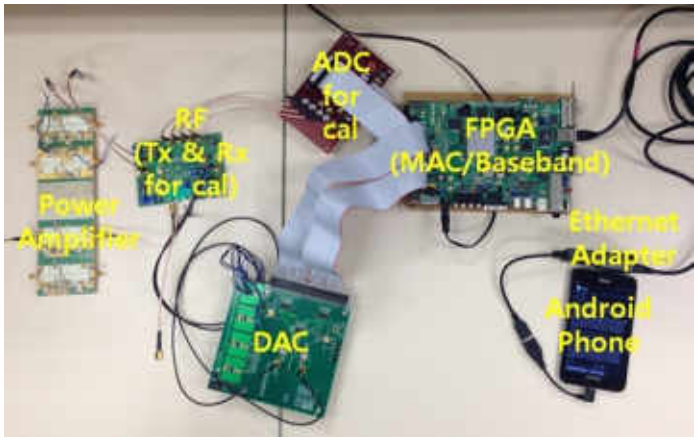
V2X Communication

Previous Works

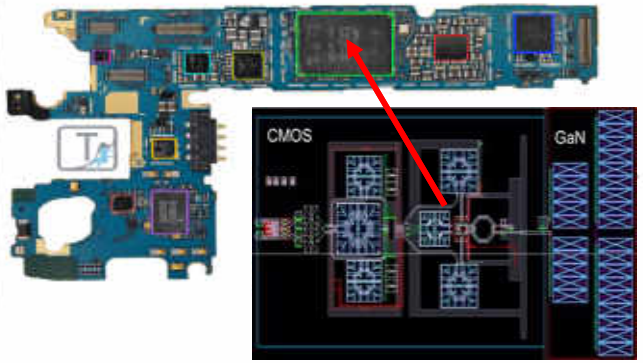
- Commercially available IEEE 802.11p radio
- Bulky & low output power

Our Works



Prototyping using our designed CMOS and GaN circuits (as well as an Android SW in a smartphone)

Near Future



Integration of GaN+CMOS single-chip radio in a smartphone (for direct phone-to-phone comm.)

(PCT published, US published)

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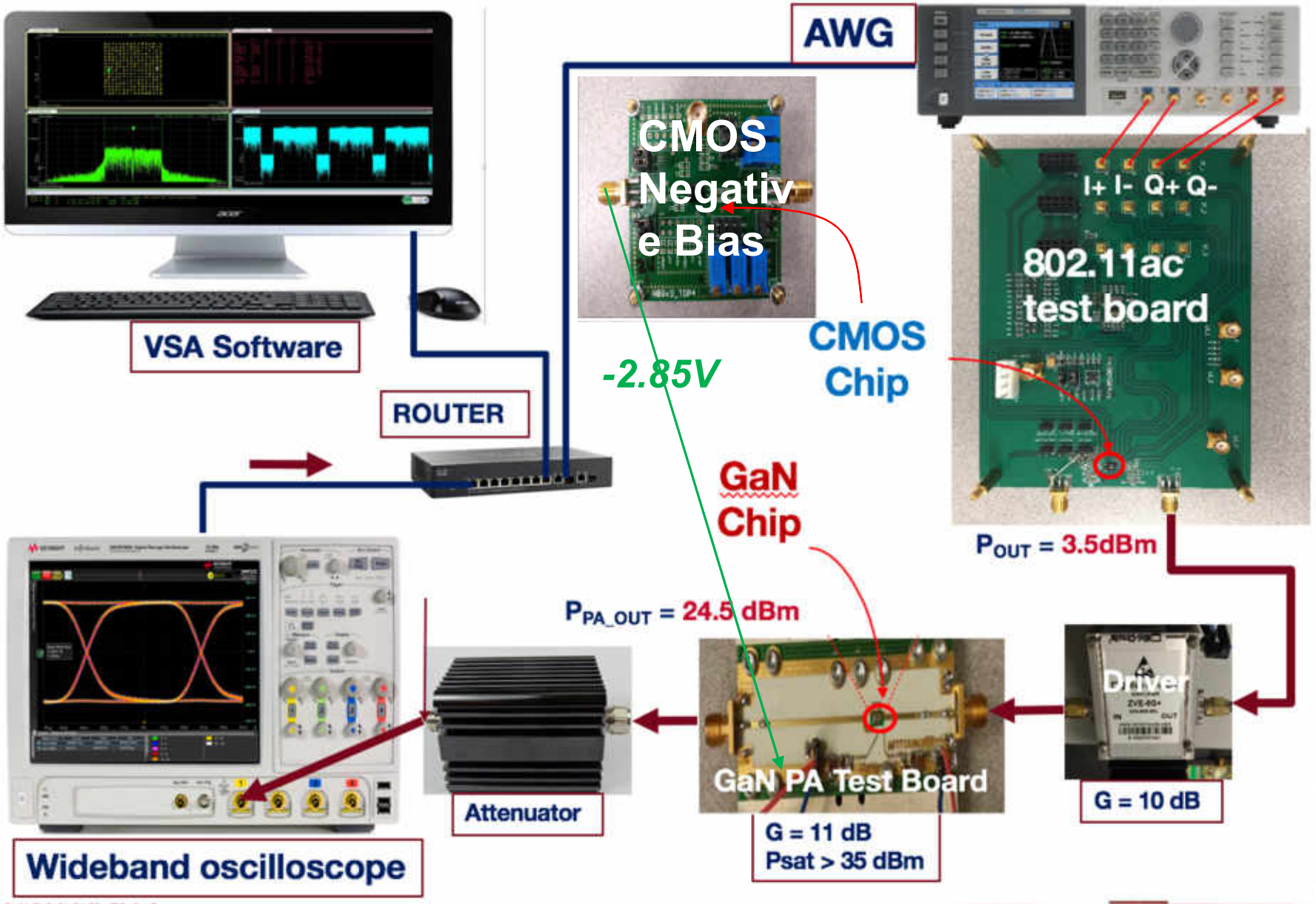
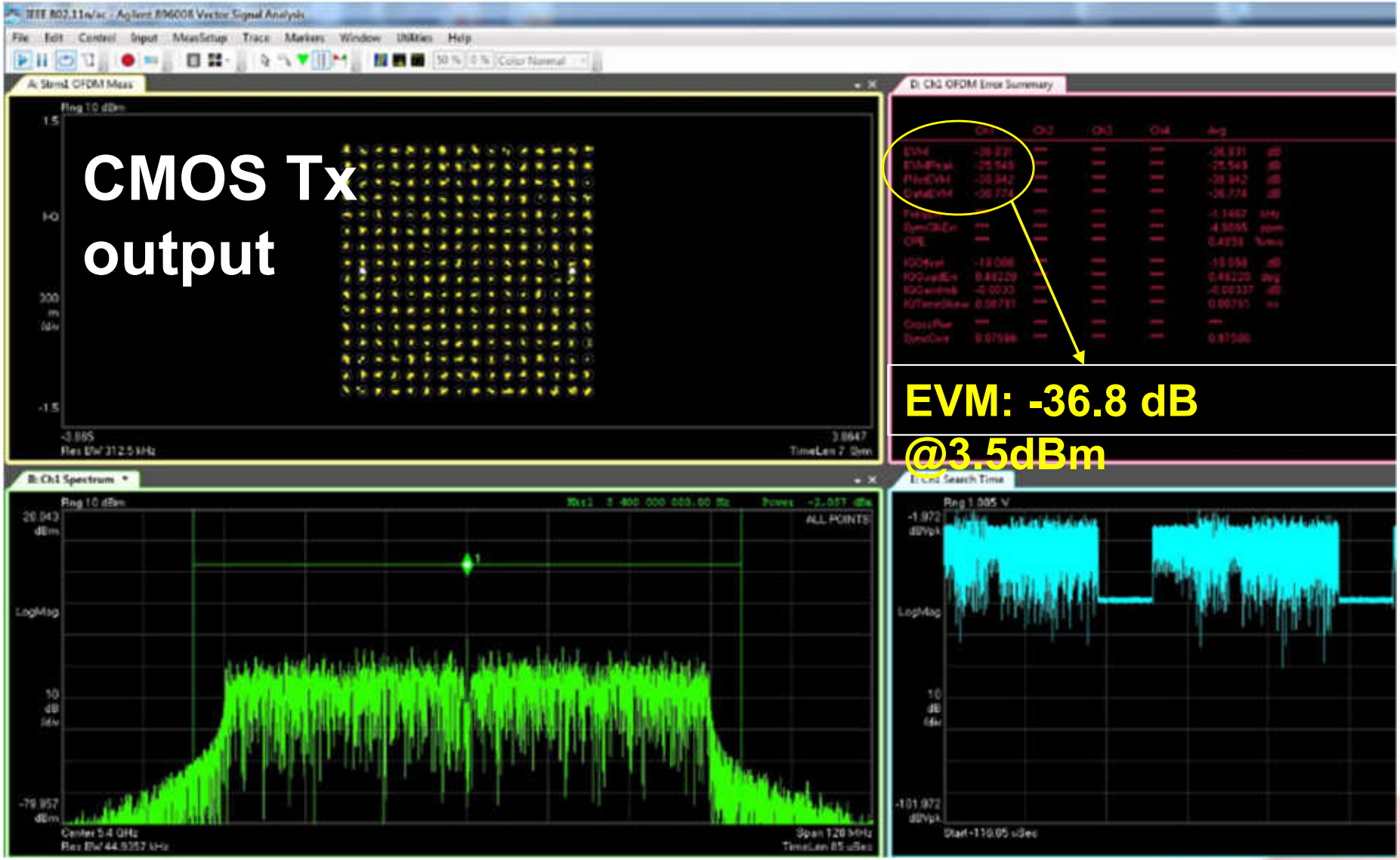
GaN+CMOS system integration (1/2)



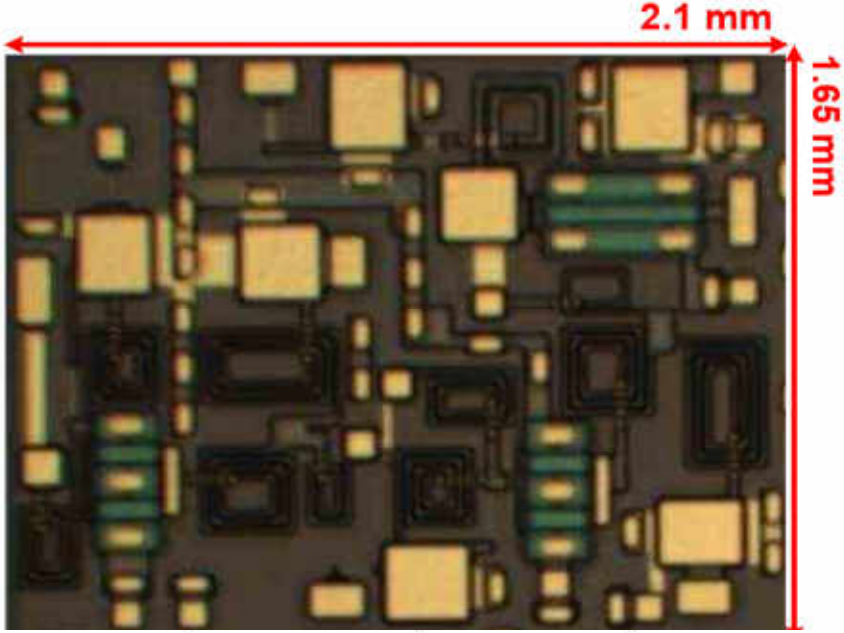
GaN+CMOS system integration (2/2)

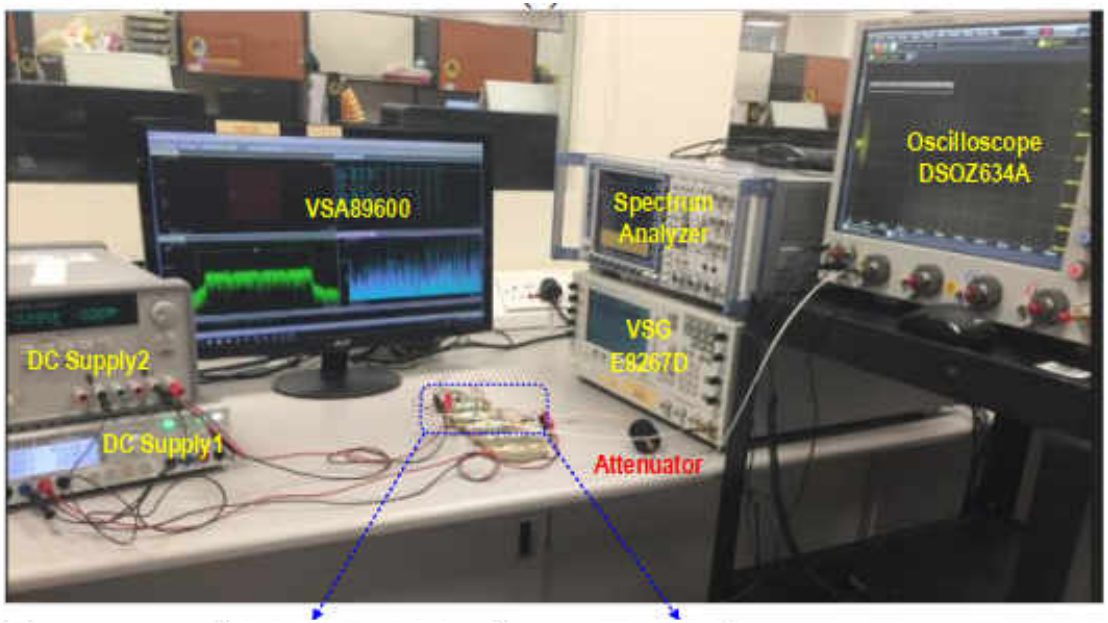


EVM: -36.8 dB for 80MHz 256 QAM Std. 802.11ac Signal at 5.4 GHz

Sub-6GHz 5G GaN PA:
2.4-6GHz (Fully Int. 2.1mm x 1.65mm)

B. Liu, C. C. Boon, IEEE TCAS-I, 2021





Ref.	Freq (GHz)	Gain (dB)	P_{sat} (dBm)	PAE (%)	DC Supply (V)	Area(mm^2)	Technology
[7]	2–6	12.8–13.7	40.9–41.5	27–34	28	7.6	0.25μm-GaN HEMT
[8]	0.5–6.5	10	33.45	38	15	4	0.5μm-GaN HEMT
[9]	1.5–10	12–16	30.7	44	7	4.6	0.25μm-GaAs pHEMT
[12]	3–7.5	19.6–21.6	21.4–22.9	20–30	3.5	1.9	0.15μm-InGaAs pHEMT
[15]	2-4	11.3-13.4	35.1-38.9	40-55	28	3.2	0.25μm-GaN HEMT
[29]	2–6.5	24–27	31–32	31.4–51.5	5	9.6	0.15μm-GaAs pHEMT
[30]	2–6	15	38.5–40	35–30	20	23	0.5μm-GaN HEMT
[31]	4–6	10–12.2	33.9–36.1	38–48	28	2.3	0.25μm-GaN HEMT
[32]	4.5–6.5	10.6–12.4	34.9–36.3	44–49	28	2.5	0.25μm-GaN HEMT
This work	**2.4–6**	**30.2–34.7**	**35.2–36.3**	**38–53**	**28**	**3.5#**	**0.25μm-GaN HEMT**

Sub-6GHz 5G GaN PA:
2.4-6GHz (Fully Int. 2.1mm x 1.65mm)

B. Liu, C. C. Boon, IEEE TCAS-I, 2021

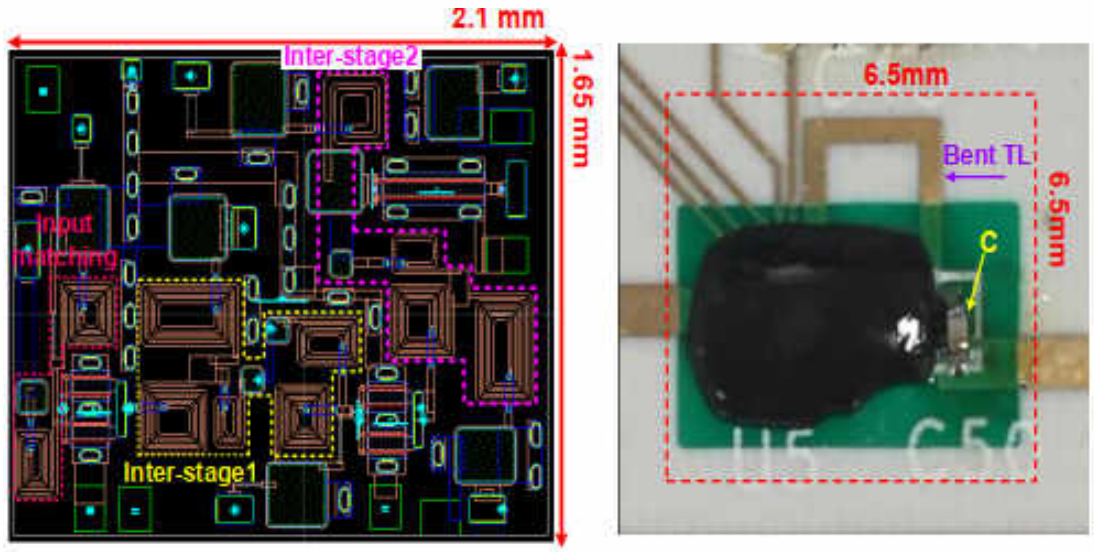


Fig.24. Photograph of GaN die and PCB.

The network using the proposed topology shows three complex poles. In contrast, there are two complex poles for all other kinds of the coupled resonators.

Intuitively, one more complex pole could provide the potential to increase bandwidth in the same in-band ripple level, without the reduction of transmission gain.

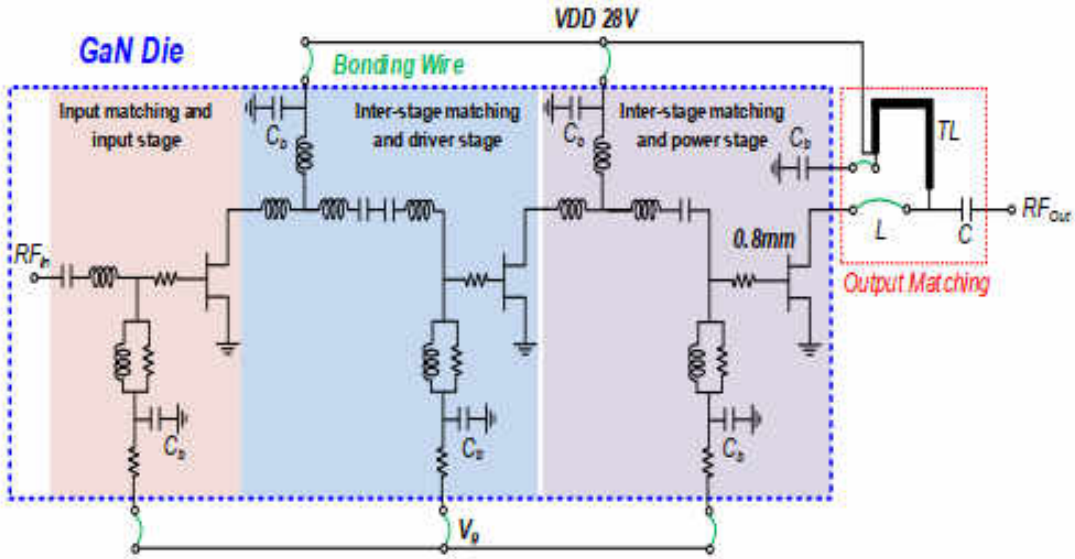


Fig.17. Schematic of the PA.

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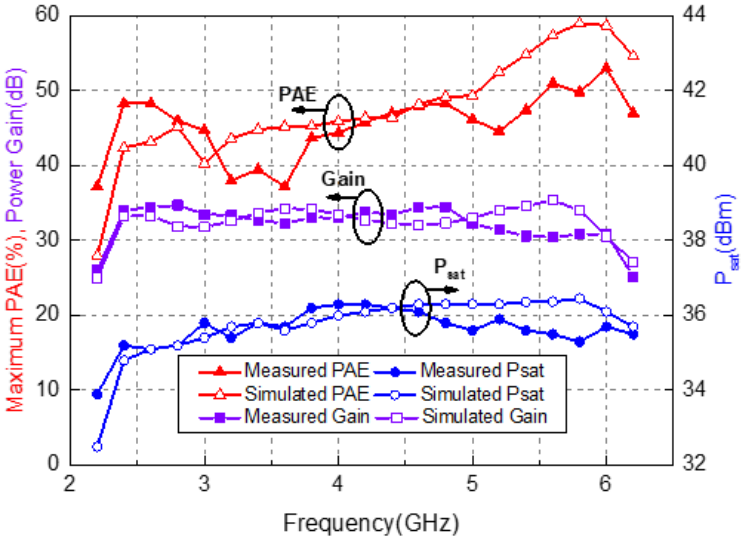
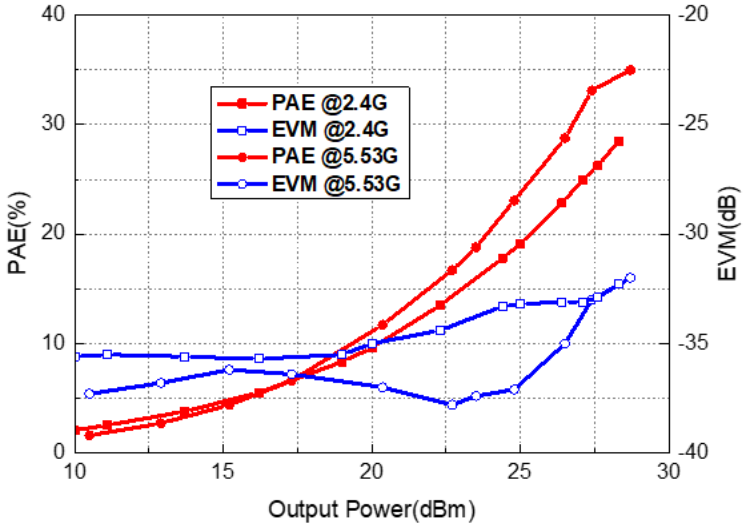
Sub-6GHz 5G GaN PA: 2.4-6GHz (Fully Int. 2.1mm x 1.65mm)

B. Liu, C. C. Boon, IEEE TCAS-I, 2021

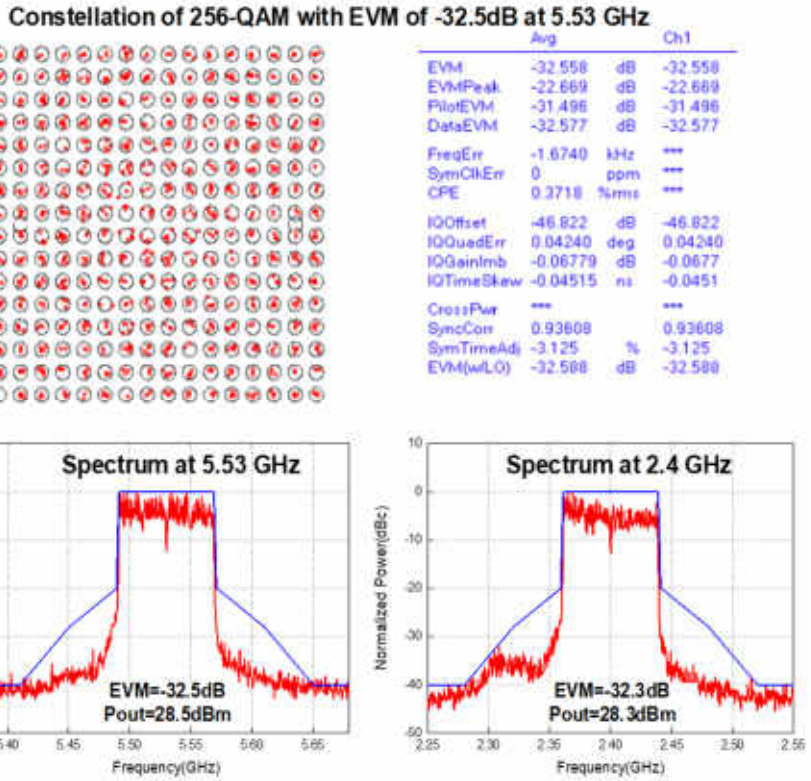
CW performance (**Broadband**)



PAE and EVM in different power level



Measured EVM and spectrum using 80-MHz 256-QAM signal



Measured CW performance:

- **Frequency: 2.4GHz-6GHz**
- **Output power: 35.2-36.3dBm**
- **Efficiency: 38-53%**
- **Gain: 30.5-34.7dB**

Sub-6GHz 5G GaN PA:
2.4-6GHz (Fully Int. 2.1mm x 1.65mm)

TABLE I
COMPARISON WITH OTHER BROADBAND PAS

Ref.	Freq (GHz)	Gain (dB)	P_{sat} (dBm)	PAE (%)	DC Supply (V)	Area(mm^2)	Technology
[7]	2–6	12.8–13.7	40.9–41.5	27–34	28	7.6	0.25μm-GaN HEMT
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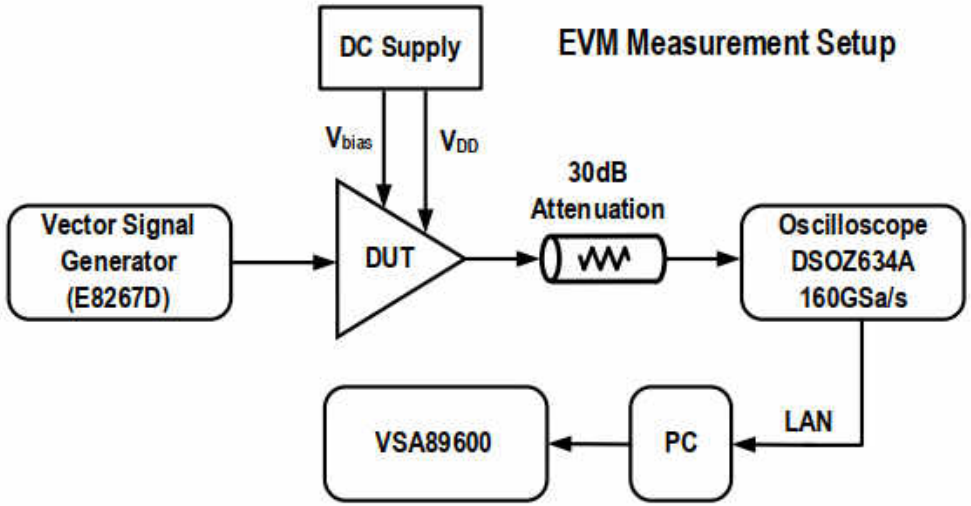
[9]	1.5–10	12–16	30.7	44	7	4.6	0.25μm-GaAs pHEMT
[12]	3–7.5	19.6–21.6	21.4–22.9	20–30	3.5	1.9	0.15μm-InGaAs pHEMT
[15]	2-4	11.3-13.4	35.1-38.9	40-55	28	3.2	0.25μm-GaN HEMT
[29]	2–6.5	24–27	31–32	31.4–51.5	5	9.6	0.15μm-GaAs pHEMT
[30]	2–6	15	38.5–40	35–30	20	23	0.5μm-GaN HEMT
[31]	4–6	10–12.2	33.9–36.1	38–48	28	2.3	0.25μm-GaN HEMT
[32]	4.5–6.5	10.6–12.4	34.9–36.3	44–49	28	2.5	0.25μm-GaN HEMT
This work	**2.4–6**	**30.2–34.7**	**35.2–36.3**	**38–53**	**28**	**3.5#**	**0.25μm-GaN HEMT**

Chip area is 3.5mm^2, and whole PA including external output matching network is within 6.5×6.5 mm^2.



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Dual-Band (2.4G/5G) Transmitter Design

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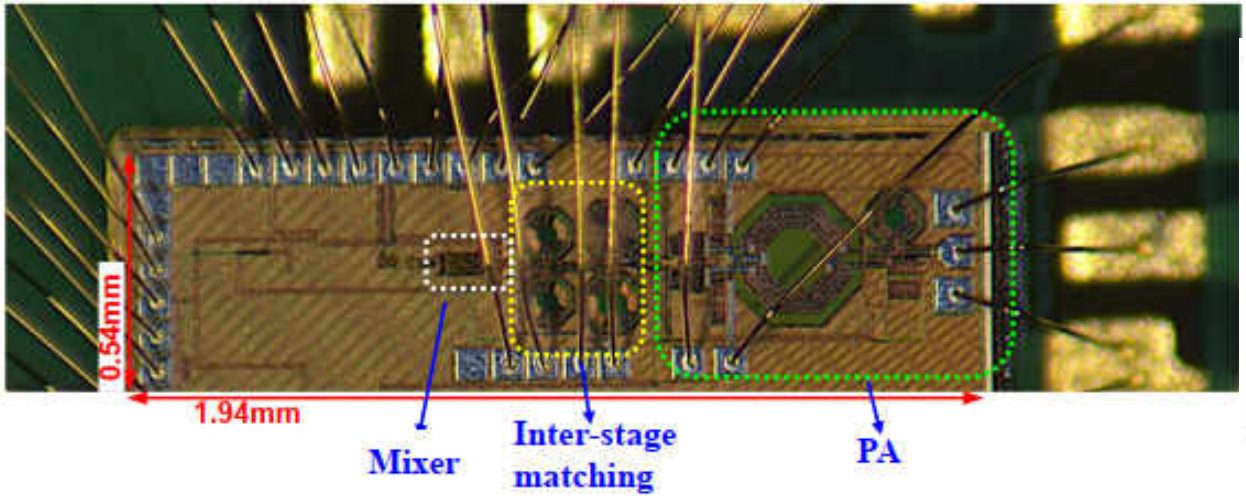
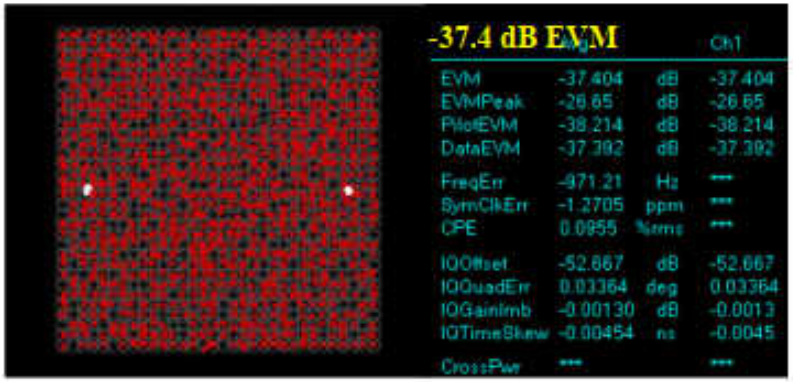
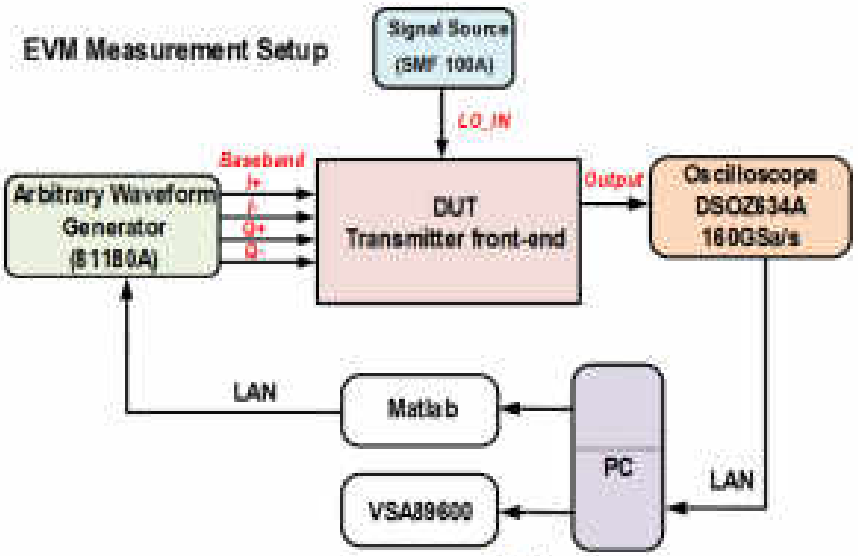




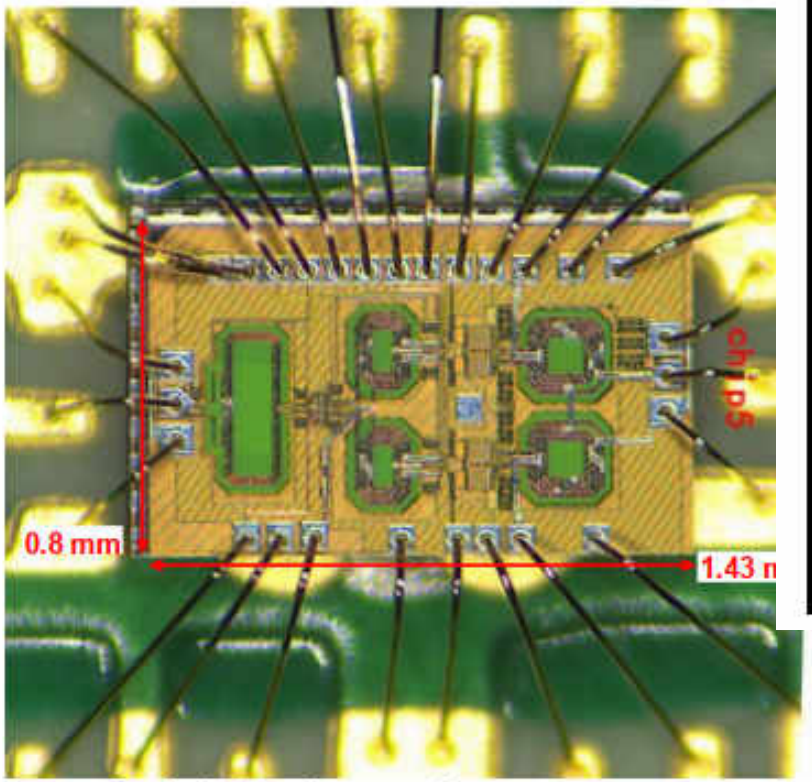


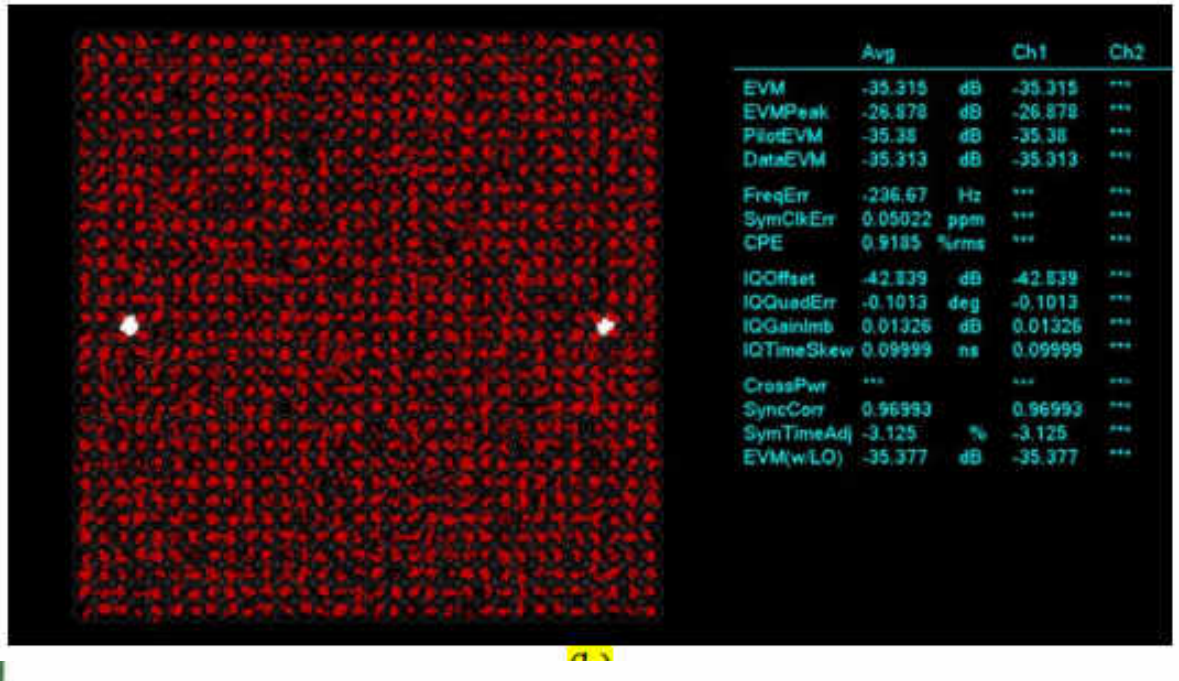
EVM measurement setup

Merits of the proposed dual-band transmitter

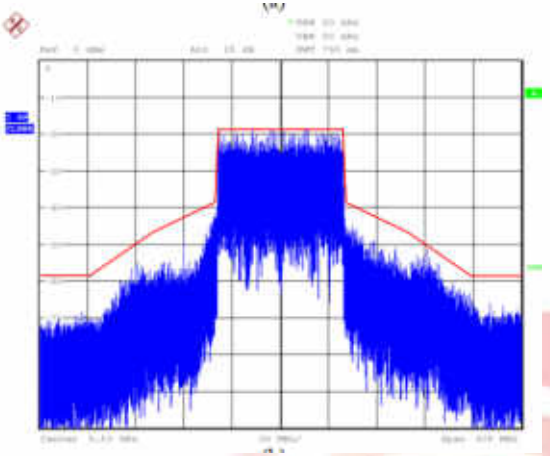
- Low cost: single transmitter
- High linearity: support 80MHz, 1024-QAM signal
- Advanced WLAN standard: 11ax
- The first Dual-band Transmitter using only one transmitter channel

RFIC for Wireless Communication
- CMOS 2.4/5GHz Dual-band PA for Sub-6GHz CA





- VHT80, MCS10 signal at 5.53 GHz 1024-QAM.



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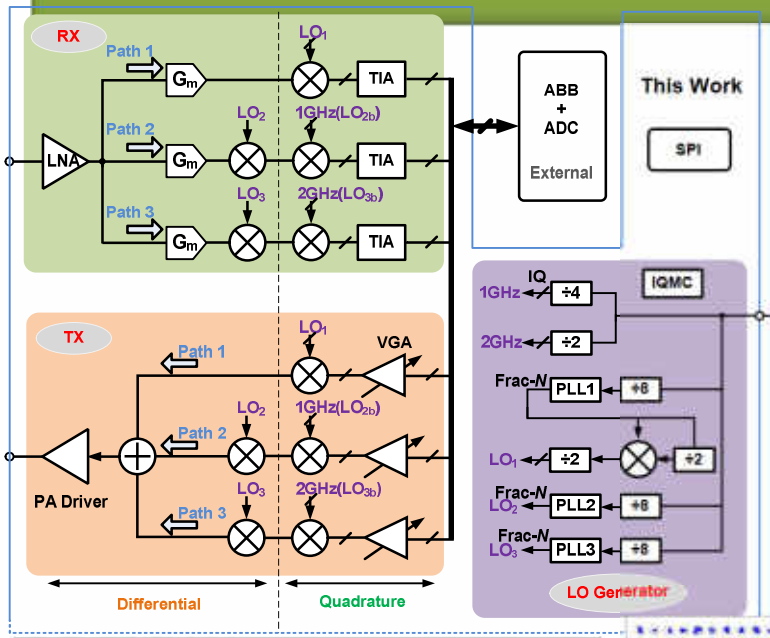
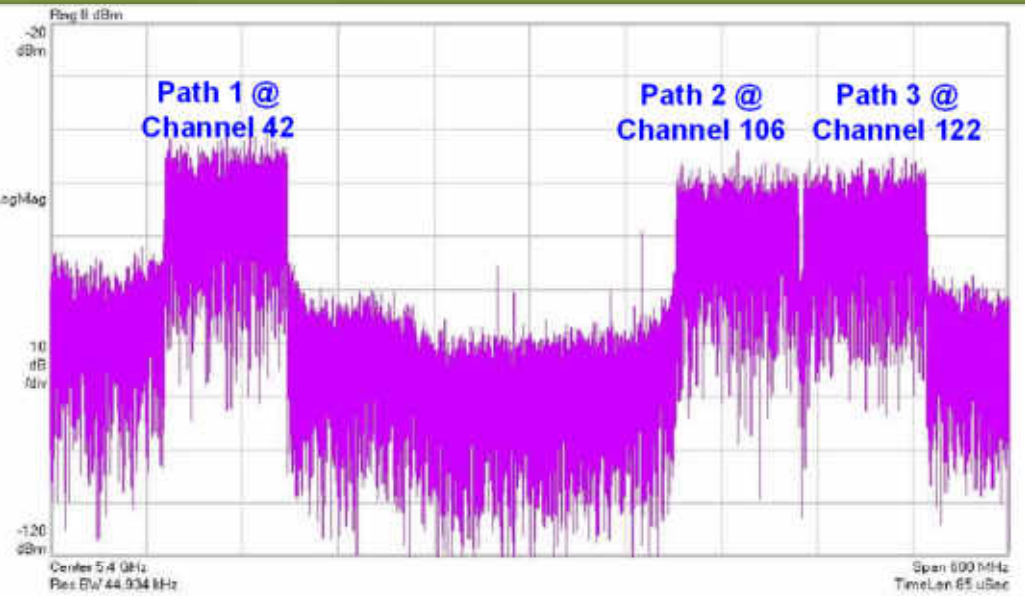
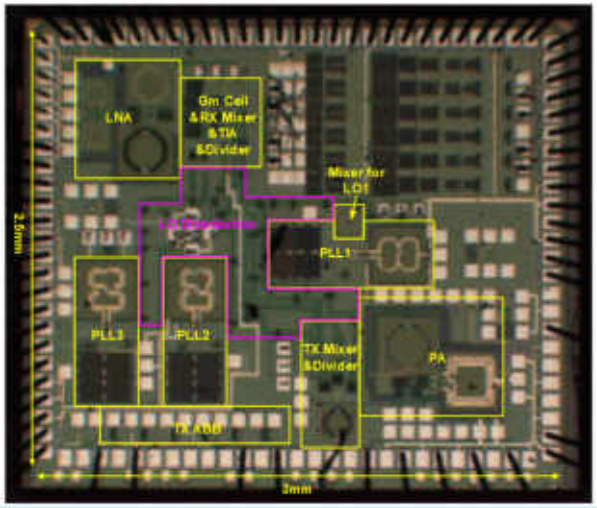
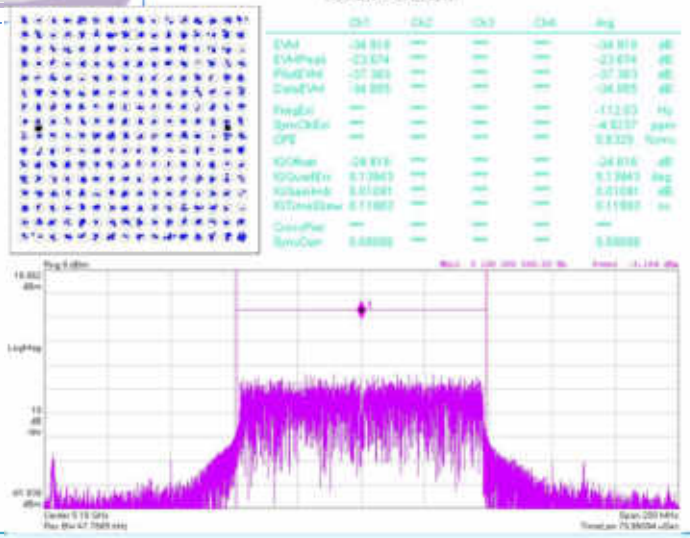
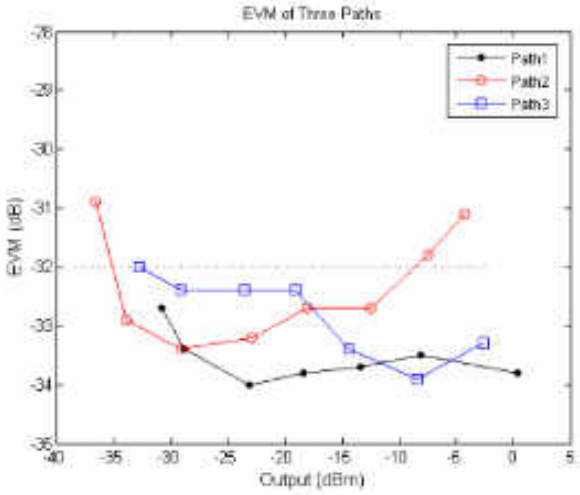
2 x 2 MIMO RFIC 3-Carrier Aggregation TRX for WiFi-6











1. Proposed transmitter can mitigate cross-talk and VCO pulling
2. Proposed transmitter can support inter-band and intra-band carrier aggregation

"Technology Cooperation Excellence Award" by Huawei. This award is for top 10% best research completion around the world. 2019.

Thank you for your time and effort to understand our work.

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