A 3.1-8 GHz CMOS UWB Front-End Receiver

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***Abstract*—A two-stage down-conversion architecture for 3.1−8 GHz ultra-wideband receiver front-end is designed which uses a local oscillator frequency equal to half the input frequency. The down-conversion technique is performed in two steps based on half-RF architecture to produce baseband signal. The proposed technique is implemented in 0.18 μm CMOS technology which achieves a conversion gain ranges from 36.1−32.4 dB and noise figure of 5.4−8.3 dB across the bandwidth.**

I. Introduction

The Ultra-wideband (UWB) front-end receiver can be designed either as direct conversion technique or double conversion technique. In the UWB receiver front-end a blocking signal can simply get down-converted with the desired RF band to the baseband frequency. This blocking signal appears as low-frequency second-order distortion, which is generated due to the non-ideality of the receiver stage such as device/load mismatch in the mixer stage and RF self-mixing. In [1] it is shown that if there is a blocker at $(2k-1)f_{LO}+f_{RF}$ in a zero intermediate-frequency (IF) UWB system, this mechanism will transfer the switch flicker noise to the baseband output. Apparently, this issue in a wideband receiver is one of the drawbacks, which can severely suppress the front-end performances.

In this paper unlike the conventional method, which employs the direct conversion technique, a two-stage down-conversion architecture is used to alleviate the even-order distortion and LO leakage issues appeared in the direct conversion receiver (DCR). This architecture, however, poses a number of drawbacks, which are described through the paper.

II. UWB Front-End Architecture

A simplified block diagram of the proposed receiver front-end is shown in Fig. 1. A single-to-differential low noise amplifier (SD LNA) circuit is designed to avoid the lossy and costly balun in front of the receiver. As shown, followed by the the LNA a two-stage down-conversion mixer is designed to down-convert the wideband RF frequency to the baseband. As a result a 3.1−8 GHz RF frequency is down converted to zero-IF at the baseband. The output buffers are integrated for the measurement purposes only. The differential output of the mixer is converted into a single I/Q, and drive an external 50 Ω load.

A. SD LNA with on-chip transformer

As shown in Fig. 2, a SD LNA is used with an output transformer load to provide differential output. The output transformer acts as AC-coupling (high-pass filter), which attenuates the IM2 harmonics generated by the LNA at low frequency. Coupling capacitors were placed between LNA and mixer to remove any DC offsets from LNA. A very low current is consumed in this design, since only one stage is used to generate differential output. More details on the principle of the LNA can be found in [2]. In the transformer, the appropriate number of turns $n = 1$ is chosen for two reasons; to provide high quality factor (Q) for better noise figure, and also avoiding to disturb the LNA performances. The transformer was measured separately from 1−10 GHz, which shows a maximum primary Q of 8 and secondary Q of 13 at 8 GHz frequency. The primary and secondary inductances are 0.58 nH and 0.68 nH, respectively. The designed on-chip transformer prevent the use of off-chip lossy balun.

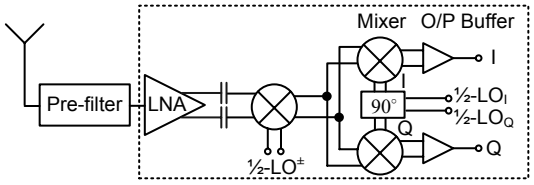

Fig. 1. Simplified block diagram of the UWB front-end receiver

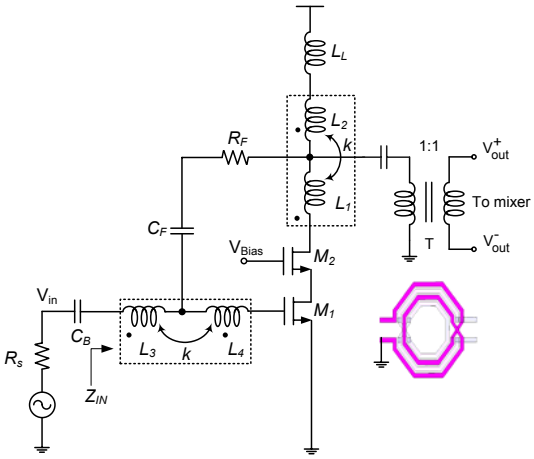

Fig. 2. Simplified schematic of the UWB SD LNA (biasing is not shown).

B. Down-Conversion Mixer Architecture

The proposed down-conversion mixer is shown in Fig. 3(a), which the down-conversion is performed in two-stage

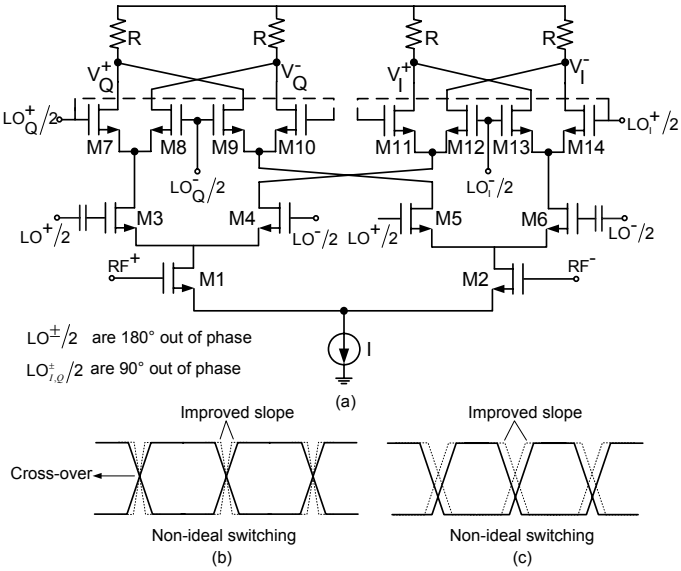

Fig. 3. (a) Simplified schematic of the double-balanced down-conversion mixer, (b), (c) Non-ideal LO switching and slope improvement

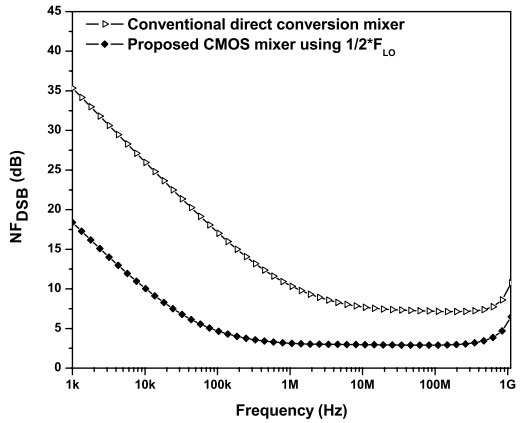

Fig. 4. Flicker noise comparison between different types of the mixers.

with $f_{LO} = f_{RF}/2$ for both switching stages. The first switching stage M_3-M_6 down-converts the RF frequency to an intermediate frequency, and the second stage is similar to a direct conversion technique. The second stage experiences the same issues as a conventional direct conversion receiver does, such as flicker noise. However, having a LO waveform with a large $S \times T$ product, that is, low frequency LO with sharp transition will lower flicker noise of the switching stage, where S is the slope of the LO waveform at cross-over point, and T_{LO} is the LO period [3]. The $1/2$-LO signal is applied to the gate of switching transistors stage to modulate the drain voltage of M_1-M_2. The RF frequency is down-converted into $1/2$-IF frequency at the drains of M_3-M_6. Therefore, the switching action of M_3-M_6 varies the drain-source voltage and transconductance (g_m) to provide frequency conversion gain. The down-converted signal is translated into the baseband frequency by another $1/2$-LO down-conversion stage using M_7-M_{14} transistors.

Fig. 3(b) plots non-ideal switching waveforms. As it is shown in solid line, the LO slope at cross-over is reduced due to the imperfect characteristics of the switches and asymmetric layout routing. One way to reduce the LO cross-over window is to increase the LO slope by increasing the LO-power, shown by dotted line in Fig. 3(b). However, if the high LO voltage driven the FET switches into deep triode region, the nonlinearity of the mixer deteriorates due to the nonlinear resistance of the switches. Another issue happens during the switching event, for instance when switch M_6 is ON at LO$^+$, and M_5 is supposed to be OFF at this period. However, the mismatch between two switches may cause M_5 to conduct for an interval time or vice versa. So ON-resistance R_{ON} of the switch M_5 drop the gate-source voltage of the transconductance stage, which reduces the conversion gain. As a result, during this time, flicker noise contribution increases.

Similarly in Fig. 3(c), the non-ideal LO switching property due to the mismatch between threshold voltages of the switches (biasing voltage and device size mismatch) varies the duty cycle of the switches. Therefore, the ON/OFF-time of each transistor, can be different from its OFF/ON-time. As a result, undesired signals are generated at the differential output, which can cause second-order intermodulation distortion (IM2). All the transistors were carefully laid out to reduce any possible mismatch. In here, an off-chip voltage regulator is used to further adjust the biasing voltage of the mixer at port V_{DD2} (shown later in Fig. 6). Since in the proposed architecture LO operates at $1/2$-RF, so LO to RF leakage is eliminated significantly.

Fig. 4, shows a flicker noise simulation comparison between two types of the mixer in the same simulation condition. The conventional direct-conversion mixer shows much higher corner frequency than the proposed mixer. Since the baseband bandwidth in this application is very wide compared to many other narrowband designs, practically the corner frequency is higher than other narrowband applications. A disadvantage of the proposed architecture is that I/Q mismatch causes the image of the signal to lie nearby zero. However, since the intermediate frequency of the first down-conversion is high enough ($1/2$-RF), preselect filter at the antenna can suppress the image. So the design of image rejection filter can be relaxed.

If we assume that the LO-power is large enough, and mixing function is observed by commutation of the RF transconductance with LO square-wave $sq(\omega_{LO})$, ignoring the effect up-converted terms, the output load current is derived

$$\begin{aligned} I_{out} &= g_{m1} V_{RF}(t)\, V_{LO}(t) \\ &= (I_{DC} + g_{m1} \sin \omega_{RF} t) \times (V_{LO}(t) + \Delta_{offset}) \\ &= \frac{2}{\pi} g_{m1} V_{RF}(t) \left(\cos(2\omega_{LO} - \omega_{RF})\right) (I_{DC} + \Delta_{offset}) \end{aligned}$$

$$V_{LO}(t) = \frac{4}{\pi} \sum_{n=1}^{\infty} \left(\frac{1}{n}\right) \cos(2n\omega_{LO} t). \quad (1)$$

where down-converted output frequency is shown as $2\omega_{LO} - \omega_{RF}$, I_{DC} is the DC current associated with RF

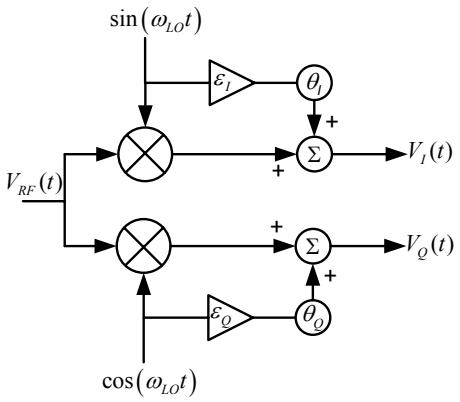

Fig. 5. I/Q receiver model including I/Q imbalance.

components and Δ_{offset} is the DC offset due to the changes in duty cycle over 2π period $\left(=\frac{\Delta T}{2\pi}\right)$. From above, the overall voltage gain of the mixer is

$$\text{Mixer Gain} = (2/\pi)\, g_{m1}\, (R \parallel R_{out,mixer}) \tag{2}$$

where R is determined by the load resistance and $R_{out,mixer}$ is the output impedance looking into drain of the switching stage when LO voltage is applied. The switching stage of the mixer is biased at $V_{GS} - V_t =$ 0.25 V to keep the switches in the saturation region, with total biasing current of 2 mA.

1) I/Q mismatch: In practice, there are always unavoidable mismatches in the phase and amplitude between I and Q signals in the mixer, as modeled in Fig. 5. The I/Q imbalance is introduced by the local oscillator as amplitude mismatch ε and phase mismatch θ. According to the model,

$$V_Q(t) = V_{RF}(t).\cos(\omega_{LO}t) + \varepsilon_Q.\cos(\omega_{LO}t + \theta_Q). \tag{3}$$

$$V_I(t) = V_{RF}(t).\sin(\omega_{LO}t) + \varepsilon_I.\sin(\omega_{LO}t + \theta_I). \tag{4}$$

we can rewrite (3) and (4) as

$$V_Q(t) = A\cos(\omega_{LO}t + \alpha), \quad V_I(t) = B\sin(\omega_{LO}t + \beta). \tag{5}$$

$$A = \sqrt{(V_{RF}(t) + \varepsilon_Q\cos(\theta_Q))^2 + (\varepsilon_Q\sin(\theta_Q))^2}. \tag{6}$$

$$\alpha = \tan^{-1}\left(\frac{\varepsilon_Q\sin(\theta_Q)}{V_{RF}(t) + \varepsilon_Q\cos(\theta_Q)}\right). \tag{7}$$

$$B = \sqrt{(V_{RF}(t) + \varepsilon_I\cos(\theta_I))^2 + (\varepsilon_I\sin(\theta_I))^2}. \tag{8}$$

$$\beta = \tan^{-1}\left(-\frac{V_{RF}(t) + \varepsilon_I.\cos(\theta_I)}{\varepsilon_I.\sin(\theta_I)}\right). \tag{9}$$

It should be noted that $\varepsilon_I/\varepsilon_Q$ and θ_I/θ_Q in I and Q branches are independent respectively. The first parts in (3) and (4) denote the down-converted signal and second terms are the frequency components created by the amplitude and phase mismatch. In order to eliminate the imbalance in phase and amplitude in two branches, the following equalities should be satisfied, $V_Q(t) + V_I(t) = 0$, $A = B$ and $\alpha - \beta = \pi/2$. Reduction in mismatch by balancing the LO signals would improve the performances especially second-order harmonic, which in here LO mismatch was trimmed off-chip.

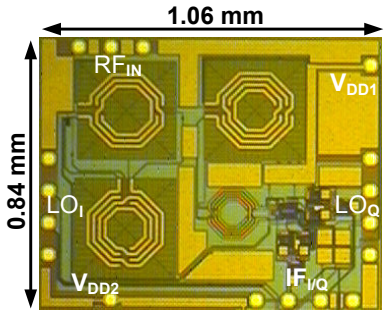

Fig. 6. Chip photograph of the wideband receiver.

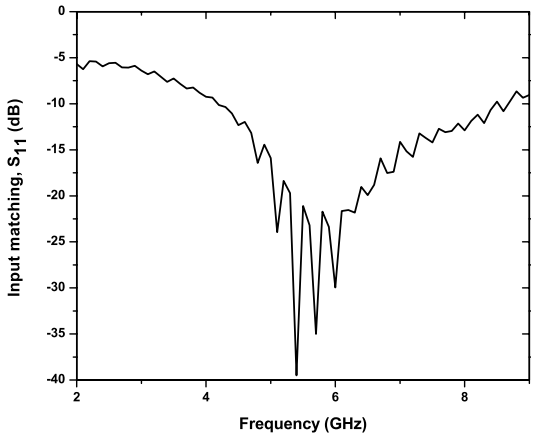

Fig. 7. Measured input reflection coefficient (S_{11}) of the receiver.

III. Measurement Results

Fig. 6 shows the chip photograph. A quadrature LO is applied off-chip using a signal-generator through a wideband balun and 90° hybrid coupler. From measurement results, the LNA and the mixer each consumes a total current of 2.45 mA and 2 mA from a 1.8 V supply voltage, respectively. The measured S_{11} is plotted in Fig. 7, showing a reasonable input matching from 3.1−8 GHz.

The conversion gain (CG) of the receiver is measured at the output of an on-chip unity-gain buffer, shown in Fig. 8. The peak gain is about 39.2 dB. The frequency response of the receiver can be improved with a wider-band test buffer. The CG's ripple from 3.1−8 GHz is about 2.5 dB. In Fig. 9 the graph of third-order intermodulation is shown at 3.05 GHz frequency, for instance. Two-tones are applied at 3.05 GHz and 3.06 GHz respectively, while LO is at 1.5 GHz frequency. The 1 dB difference between two fundamental tones at 49.96 $\approx$ 50 MHZ and 59.94 $\approx$ 60 MHz, in Fig. 9, is due to the unbalanced off-chip wideband balun at LO port. The phase and amplitude imbalance of the balun may cause distortion in the measurement, particularly at 1.5 GHz frequency, since the available wideband off-chip balun is calibrated from 2−4 GHz, which is used for LO signal. Table I summarizes the performances comparison of the references. The measured LO-RF and LO-IF isolation is plotted in Fig. 10. The LO-IF isolation may not be very high since the first

TABLE I
PERFORMANCES COMPARISON TABLE

Ref.	Bandwidth (GHz)	$Gain_{max}$ (dB)	IIP3 (dBm)	IIP2 (dBm)	NF (dB)	Power (mW)	Tech. (CMOS)	$FOM = \frac{\lvert Gain_{max}\rvert BW_{GHz}}{(NF-1)P_{mW}}$.
This work	3.1−8	36.1	$>$ -2.5^{+}	$<$ +33	5.4−8.3	8*	0.18 μm	16.2−7
[4]	3−10	15.5	$>$ -6.6	–	5.2−5.4	14.8	0.13 μm	3.7−3.5
[5]	3−10	29.1	-13.5	–	4.9−8.8	33	0.13 μm	2.8−0.92
[6]	3.1−8	23.2	$>$-3	$<$+46	5.2−7.3	18	0.18 μm	1.7−0.9
[7]	3−5	37	-22	–	3.6−4.1	51	0.13 μm	2.1−1.76

$^{+}$ The lowest IIP3 is -10 dB at 3 GHz. * The power consumption including output test buffer is 50.4 mW.

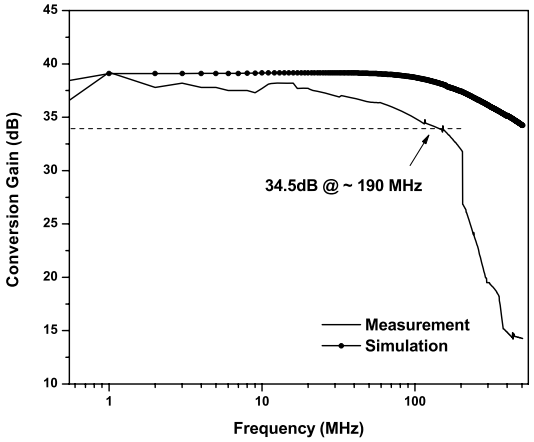

Fig. 8. Measured/Simulated conversion gain of the receiver at 8 GHz.

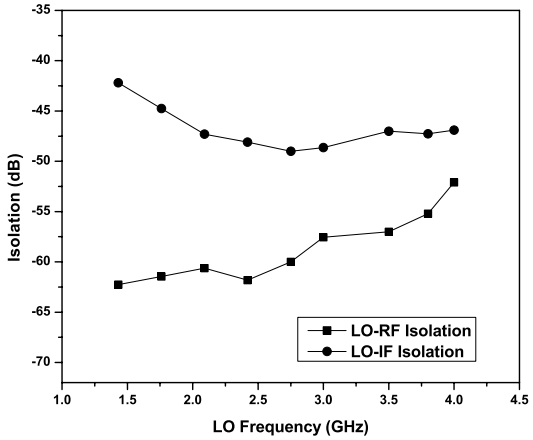

Fig. 10. Measured isolation of the LO and IF to the RF port (LNA input).

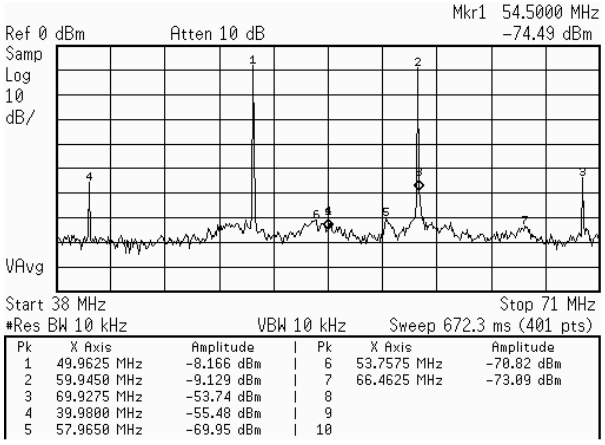

Fig. 9. An example of measured IIP3 which shows the third-order interferer.

stage of the mixer produces an IF equal to the LO frequency. With a low coupling voltage from LO-RF port, higher value of IIP2 is achievable and less unwanted signals are presented at the output. The measured corner frequency of the flicker noise is at 400 KHz which is higher than simulation.

IV. CONCLUSION

A two-stage down-conversion architecture was employed in the design of the 3.1−8 GHz receiver front-end. The single stage low power single-to-differential LNA eliminated the need for an off-chip balun and increases the integrity level of the front-end receiver. Using the proposed technique a good linearity and IIP2 was achieved from receiver front-end. The reduction in the flicker noise helps to improve the lower frequency noise figure. A good LO-RF isolation restricts the leakage of the unwanted signals to the RF port, which reduces the second-order harmonic distortion.

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