A Divide-by-Two Injection-Locked Frequency Divider with 13-GHz Locking Range in 0.18-μm CMOS Technology

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***Abstract*—In this paper, a new divide-by-two RC-oscillator-based injection-locked frequency divider is proposed. We present a symmetrical injection circuit, with only differential inputs, to realize multi-phase injection and hence the locking range is improved. Our proposed frequency divider can output quadrature signals which are useful for modern transceiver. Post-layout simulation results in a 0.18-μm CMOS Technology show that, the divider can be locked from 2 GHz to 15 GHz, draws a current less than 4 mA. The core area is only 30 μm by 30 μm.**

***Index Terms*—Frequency divider, injection locked, ring oscillator, multi-phase injection, quadrature.**

I. Introduction

Under the influence of ever-increasing demand for higher data rate communication, the required operation frequency of phase-locked loops (PLLs) keeps getting higher. In high frequency PLL or frequency synthesizer, frequency dividers are critical components [1], [2]. The challenges of high frequency divider design are wide locking range, low power and small area. True-single-phase-clock (TSPC) dividers are known for their low power consumption and wide locking range. However, TSPC divider suffers from frequency limitation due to RC delay. For example, the maximum operation frequency of TSPC divider is less than 6 GHz, in a standard 0.18-μm CMOS technology [3], [4]. Current-mode logic (CML) static frequency divider is also widely used in high speed application for its simple design and robustness. However, the power consumption increases rapidly with its operation frequency. Recently, injection-locked frequency divider (ILFD) has attracted much attention for its high frequency and low power [5]–[15]. But they still face some problems such as narrow locking range and multi-phase inputs.

Another issue is the phase of inputs and outputs in a divider. It is well-known that, the quadrature LO signals are necessary for a typical transceiver. There are many approaches to generate quadrature signals.The first one is to use quadrature voltage-controlled oscillator (VCO), but the power consumption will double and phase noise is generally worse compared with conventional LC VCO. Secondly, we can employ poly-phase filter to generate quadrature signals. However, its insertion loss is high, so additional buffers are needed to compensate the loss. The last choice is to adopt divider with quadrature outputs. Quadrature outputs are common in CML divider, but not common in TSPC divider or traditional ILFD.

In this paper, we present an ILFD with a new architecture. The ILFD implements a division ratio of two, with differential inputs and quadrature outputs. Furthermore, the proposed topology can realize multi-phase injection naturally, which greatly improves locking range. Section II presents the proposed ILFD structure after introduction of traditional ILFD, and analyzes its multi-phase injection concept. Post-layout simulation results will be discussed in section III. The paper is concluded in Section IV.

II. Circuit Architecture and Analysis

A. Traditional ILFDs

Generally, an ILFD is an oscillator synchronized by a reference signal at a frequency close to an integer multiple k of their free running frequency f_0. There are two types of ILFDs: one is based on LC oscillator, and the other is based on RC ring oscillator, as shown in Fig. 1. LC-oscillator-based ILFD can operate at high frequency, but its locking range is very narrow due to high-Q LC tank [6], mandating fine and frequent calibrations in PLL. In addition, The area-hungry LC tank also limits its utilization in low cost application. Thus, unless in very high frequency, such as millimeter wave application, LC-oscillator-based ILFD is not practical.

RC-oscillator-based ILFD has merits of wide locking range, compact area and low power. Both [8] and [9] have demonstrated that multi-phase injection technique can improve the locking range of ILFD. However, their proposed topologies need multi-phase inputs, which is not easy to obtain from conventional LC VCO. Furthermore, the locking range will become worse if the phase difference of inputs departs from the optimum value [8]. These defects prevent the application of multi-phase injection technology in ILFD.

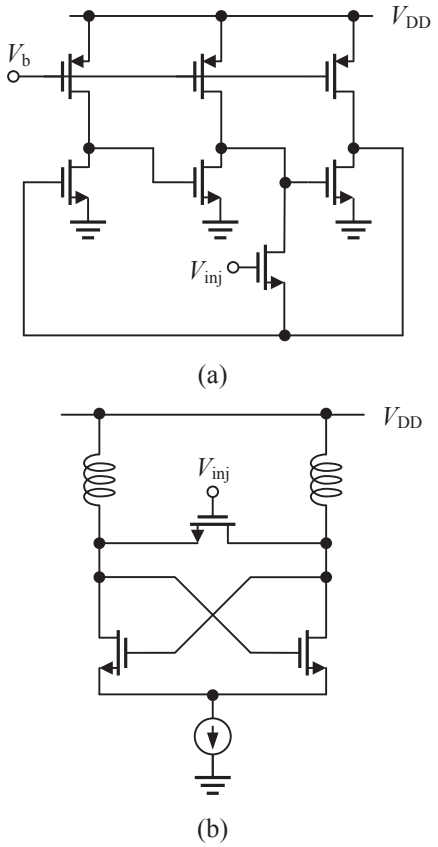

Fig. 1. Traditional ILFD (a) based on RC ring oscillator [7] and (b) LC oscillator [10].

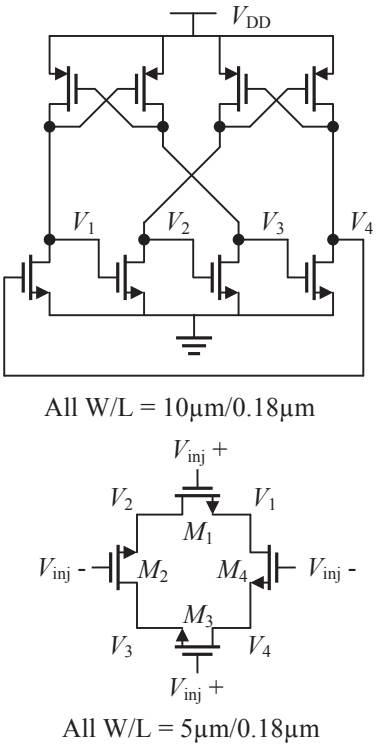

Fig. 2. Schematic of proposed ILFD.

B. Architecture of Proposed ILFD

Fig. 2 shows the schematic of proposed design. It is noted that two-stage differential RC ring oscillator, with cross-coupled pMOS load in each stage, is used to get high free running frequency and quadrature outputs. Four nMOS transistors are connected back-to-back between the drain and source of adjacent transistors to form a loop. The four connection points, V_1, V_2, V_3 and V_4, are connect to the oscillation nodes in ring oscillator. All the four nodes are loaded by identical CMOS inverters. $V_{inj}+$ is injected to the gates of M_1 and M_3, while $V_{inj}-$ is connected with the gates of M_2 and M_4. The size of all transistors in ring oscillator, including both nMOS and pMOS transistors, is the same (10 μm/0.18 μm). The size of all four injection transistors is 5 μm/0.18 μm. It seems that large injection transistors will result in larger injection currents and, consequently, larger locking range. However, the high average conductance of the injection transistors will damp the oscillation of ring oscillator, making locking range smaller [11].

C. Analysis of Proposed ILFD

To explain our proposed design, let us start with the conventional ring-oscillator-based ILFD. Assume that the gain of each stage is sufficiently large, so only the phase condition of Barkhausen criteria needs to be taken into account. Without injection, the ILFD operates at free running frequency f_0, and the load at each stage provides a $\pi/3$ phase shift to satisfy the phase condition. When the ILFD achieves locked, the phase shift provided by the load will change. Meanwhile, the frequency of ILFD will shift to a new value, that is $f_{inj}/2$ in divide-by-2 case. An extra phase shift must be generated by injection current to compensate the change of phase shift provided by the load, so as to meet the phase condition again. In the case of conventional single-phase injection, the locking range of the ILFD is narrow since the total extra phase shift around the loop is generated by only one injection current. In the case of multi-phase injection, the total extra phase shift can be provided by multiple injection currents. The locking range of this ILFD will be widened if the phase of the injections progress with the ring oscillator's intrinsic delays. However, as mentioned previously, the requirement of specific multi-phase inputs makes this technique impractical in low power application.

In our proposed ring-oscillator-based ILFD, this issue can be avoided. In fact, since the multi-phase always exists in ring oscillator inherently, the multi-phase injection can be generated in the symmetrical injection circuit by using differential inputs. For the qualitative analysis, we treat the injection transistor as a mixer, as shown in Fig. 3. The injection current of injection transistor M_i is $I_{inj,i}$ (i = 1, 2, 3, 4). The total current injected into the

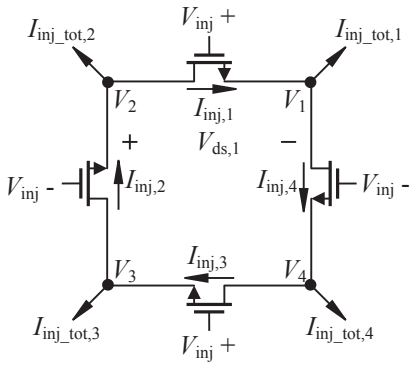

Fig. 3. Schametic of injection circuit for multi-phase injection analysis.

node V_i of the ring oscillator is $I_{\text{inj\_tot},i+1} = I_{\text{inj},i+1} - I_{\text{inj},i}$.[1] Without loss of generality, we assume the current $I_{\text{inj},i}$ flows from drain to source. The drain-source voltage of M_i is $V_{\text{ds},i} = V_{i+1} - V_i$. After injection-locked, the node voltage $V_i = \cos(\omega t + \varphi_i)$, so the drain-source voltage of M_i will be

$$V_{\text{ds},i} = \sqrt{2}\cos\left(\omega t + \varphi_i + \frac{3\pi}{4}\right), \quad \varphi_i = \frac{(i-1)\pi}{4}. \tag{1}$$

The voltage phasor relationship is shown in Fig. 4 (a). We can assume the differential injection voltages are

$$V_{\text{inj}}+ = V_{\text{cm}} + A_{\text{inj}}cos(\omega_{\text{inj}}t + \varphi_{\text{inj}}), \text{and} \tag{2}$$

$$V_{\text{inj}}- = V_{\text{cm}} + A_{\text{inj}}cos(\omega_{\text{inj}}t + \varphi_{\text{inj}} + \pi), \tag{3}$$

where ω_{inj} is equal to 2ω for divide-by-2 case, and V_{cm}, which can be tuned externally, is the common-mode voltage of differential input signals. After mixing, the injection current generated by M_i can be described as

$$I_{\text{inj},i} = \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} a_{mn}\cos(m\omega_{\text{inj}}t + m\varphi_{\text{inj}}) \cdot \cos(n\omega t + n\varphi_i + \frac{3n\pi}{4}), i = 1,3 \tag{4}$$

$$I_{\text{inj},i} = \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} a_{mn}\cos(m\omega_{\text{inj}}t + m\varphi_{\text{inj}} + m\pi) \cdot \cos(n\omega t + n\varphi_i + \frac{3n\pi}{4}), i = 2,4 \tag{5}$$

where a_{mn} is an intermodulation coefficient of the mixer. Here we pay more attention to the fundamental current because other harmonics will be suppressed by the intrinsic low-pass filter in the loop of the ring oscillator, that is, $|m\omega_{\text{inj}} \pm n\omega| = \omega$. For simplicity, only the terms with $m = 1$, and $n = 1$, are taken into consideration. Therefore, the injection currents can be simplified as

[1]Note that $i = 5$ is equal to $i = 1$ for expressing convenient.

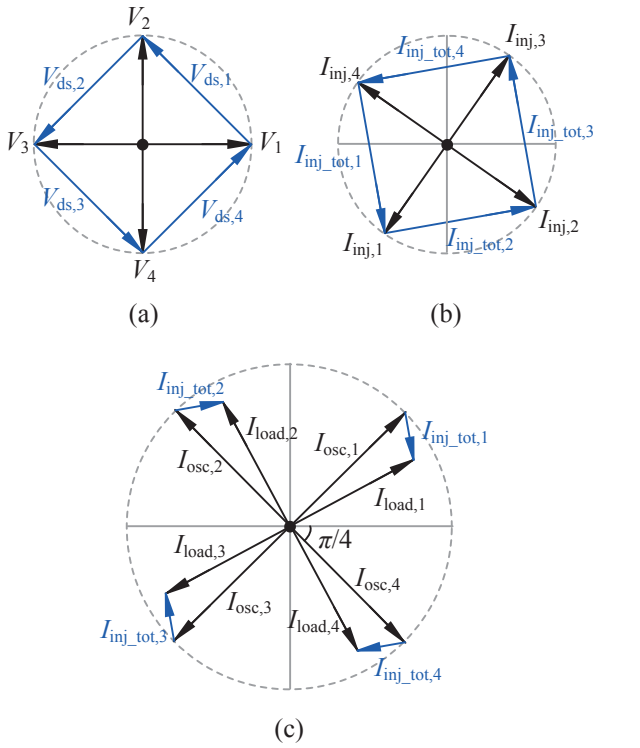

Fig. 4. Phase relationship of (a) voltage, (b) current and (c) multi-phase injection.

$$I_{\text{inj},1} = a_{11}\cos\left(\omega t + \varphi_{\text{inj}} - \frac{3\pi}{4}\right) \tag{6}$$

$$I_{\text{inj},2} = a_{11}\cos\left(\omega t + \varphi_{\text{inj}} - \frac{\pi}{4}\right) \tag{7}$$

$$I_{\text{inj},3} = a_{11}\cos\left(\omega t + \varphi_{\text{inj}} + \frac{\pi}{4}\right) \tag{8}$$

$$I_{\text{inj},4} = a_{11}\cos\left(\omega t + \varphi_{\text{inj}} + \frac{3\pi}{4}\right) \tag{9}$$

Four equations above show that the phases of four $I_{\text{inj},i}$ are in quadrature. It can be seen that, the phases of four total injection current $I_{\text{inj\_tot},i}$ are also in quadrature, as depicted in Fig. 4 (b). In other words, the injection can be considered as multi-phase injection, as depicted in Fig. 4 (c).

III. Post-Layout Simulation Results

Our proposed ILFD has been designed in Global-Foundries 0.18-μm CMOS technology. This work has already been sent for fabrication in May 2011, and the expected die delivery date is in September 2011. Self-resonance frequency of this ILFD f_0 is at about 4 GHz while supply voltage is 1.8 V. As mentioned previously, the common-mode voltage of differential inputs V_{cm} can be tuned externally. To realize a large modulation of conductance of injection transistors at the synchronization rate, we chose $V_{\text{cm}} = 1.5$ V as the optimized value [11]. Fig. 5 shows the waveforms of proposed ILFD

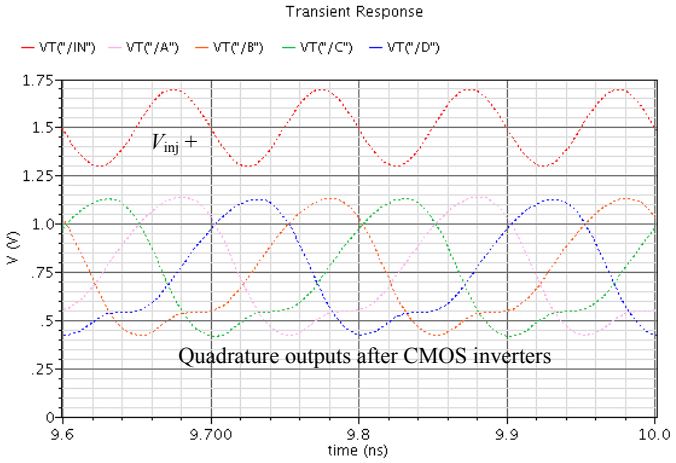

Fig. 5. Waveforms of proposed ILFD when reference input peak-to-peak voltage is 0.4 V and frequency is 10 GHz.

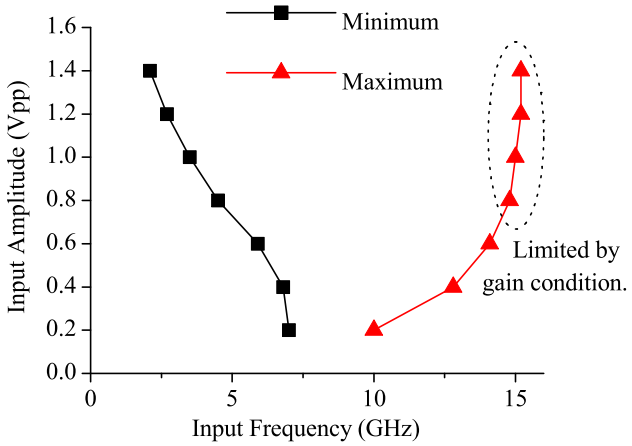

Fig. 6. Simulated input sensitivity of proposed ILFD at V_{cm} = 1.5 V.

when reference input peak-to-peak voltage is 0.4 V and frequency is 10 GHz.

A large locking range is achieved in our ILFD with divide-by-2 operation. Fig. 6 shows the simulated input sensitivity of the proposed ILFD at V_{cm} = 1.5 V. The locking range is from 2 GHz to 15 GHz, or 153% without tuning, when input peak-to-peak voltage is 1.4 V. One would expect that large injection voltages can result in larger locking range. However, the high average conductance of the injection transistors will cause gain condition of Barkhausen criteria failed in high frequency. Therefore, the maximum operation frequency is limited by gain condition.

Fig. 7 shows the power consumption, as well as output power of ILFD. Both power consumption and output power have similar curves because the ILFD operates in an almost class-A fashion [11]. The power dissipation is lower than 7.2 mW in any case. The output signals are obtained from CMOS inverters, and one of them is loaded by an AC-coupled open-drain 48 μm/0.18 μm

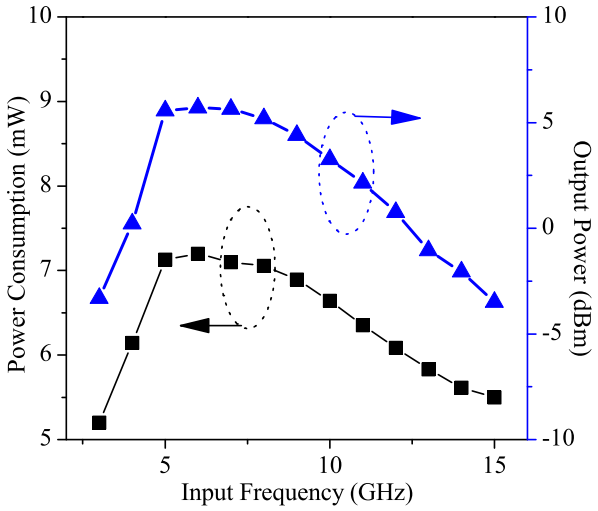

Fig. 7. Power consumption and output power of proposed ILFD when reference input peak-to-peak voltage is 1 V.

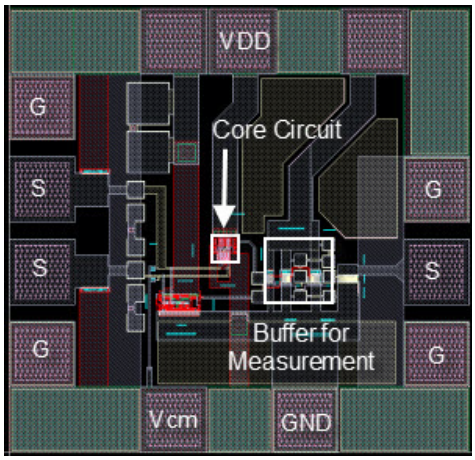

Fig. 8. Layout of proposed ILFD.

nMOS transistor for measurement.

Its core circuit occupies a small area of only 30 μm by 30 μm, as shown in Fig. 8. The performance of our ILFDs are compared with other works reported in similar CMOS technology, as summarized in Table I. Our proposed ILFD has best performance compared with dividers reported in 0.18-μm and 0.13-μm CMOS technology.

IV. Conclusion

A new divide-by-2 ILFD, with differential inputs and quadrature outputs, is proposed in 0.18-μm CMOS technology. This paper has demonstrated that our proposed topology can realize multi-phase injection by using symmetric injection circuits and only differential inputs. Post-layout simulation results show that our design can achieve a reasonable performance with very small area.

TABLE I
COMPARISON WITH OTHER WORKS IN SIMILAR CMOS TECHNOLOGY

Ref.	Tech. (nm)	V_{DD} (V)	Power (mW)	Area (μm^2)	Locking Range (GHz)	Locking Range (%)
[8]	180	1.8	24	3000	13–25*	63*
[12]	130	1.2	3.6	1944	11–15	31
[13]	180	1.8	17.6	N/A	1.95–5.5*	95*
[14]	130	2	10.4	N/A	4–6	40
[15]	180	1.8	6.8	6700	2.3–4.3	63
This work	180	1.8	7.2	900	2–15	153

* With tuning.

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