A Cascade-Parallel Based Noise De-Embedding Technique for RF Modeling of CMOS Device

X. S. Loo, K. S. Yeo, K. W. J. Chew, L. H. K. Chan, S. N. Ong, M. A. Do, and C. C. Boon

***Abstract*—In this letter, a unique cascade-parallel based noise de-embedding technique is presented for on-wafer device characterization and modeling. It utilizes two fully shielded THRU line structures and one OPEN structure that enable simultaneously de-embedding of series contact resistance, forward coupling and distributed parasitics of interconnect. Thus, it is more suitable for RF/millimeter wave noise characterization of lossy CMOS devices as compared to conventional lumped and cascade based de-embedding techniques. The proposed noise de-embedding technique is verified on both zero length THRU and OPEN devices. It demonstrates a better high frequency de-embedding performance than existing cascade based techniques by showing 1 dB improvement in predicted NFmin of 0.13 μm CMOS devices at 60 GHz. This is consistent with the further validation result on the de-embedded gain performance of the transistor.**

***Index Terms*—CMOSFETs, microwave measurements, modeling, semiconductor device noise.**

I. Introduction

HIGH frequency noise has become a dominant issue for RF IC designers due to continuous migration of operating frequency to a higher regime and escalating complexity of RF circuits. This directly prompts the need for accurate modeling and characterization of RF devices, which rely heavily on robust and correct noise de-embedding techniques to remove the impact of parasitics of a test fixture on device noise measurements.

One approach of noise de-embedding is implemented by modeling the test fixture as mixed parallel-series combinations of lumped parasitic elements [1], [2] and de-embed them in steps from the outer to inner part of a test fixture. However, such de-embedding technique would eventually fail as distributed parasitics of interconnect become prominent at high frequencies. In another approach, a test fixture is viewed as a single four port error adapter connected to two-port device. Such model was initially adopted in [3], [4] for VNA calibration, which is also popularly known as 15/16 error-terms model. The model covers most parasitic of the error adapter that includes leakage paths between ports since no assumption is made on its circuit topology. An attempt to apply this model for on-wafer noise de-embedding has been reported in [5]. Nevertheless, solving for the model error terms requires de-embedding/calibration standards to be ideal or known. Such on-wafer standards are impossible to realize on a practically lossy silicon substrate and are subjected to large process variations [6]. Therefore, this approach is not recommended for high frequency characterization of CMOS device. Instead, generalized cascade two-port networks are adopted in techniques [7], [8] to address the complexity in distributed circuit configuration of interconnect parasitics without a requirement of any precise standards. The transmission line based technique [8] moves one step further over [7] by reducing the number of de-embedding structures required by approximate interconnect of arbitrary length by equivalent transmission line model. However, both cascade based techniques [7], [8] ignore the forward coupling [9] between two test ports and the contact resistance [6] between probe and pad. Although the impact of forward coupling could be alleviated with shielded based design of test structure [2], still it could no longer be neglected at sufficiently high frequencies.

This letter presents a cascade-parallel based noise de-embedding technique that could account for both forward coupling effect and distributed parasitics of interconnect concurrently. It improves the lumped pad approximation of existing cascade based technique by taking consideration of series contact resistance without additional PAD-SHORT structure [2]. OPEN and THRU line structures are used to accurately characterize the test fixture parasitics without knowing their internal circuit configuration. The proposed de-embedding technique is verified and demonstrated on 0.13 μm CMOS device.

II. De-Embedding Theory

The proposed noise de-embedding technique is developed based on a set of shielded based structures (OPEN, THRU L and THRU LL) that enable effective removal of fixture parasitics from DUT (Device Under Test) measurements. A wide M1 ground shield is included in these structures to provide low resistive ground connections to all ports and improve the isolation performance [2]. As shown in Fig. 1(a), the two-port device to be extracted lies in the fixture gap of DUT structure and is surrounded by M1 ground shield. Note that only area within the fixture gap is vulnerable to forward coupling effect [2] at high frequencies since it is not shielded. It is filled by oxide (dielectric) which serves as the isolating material between metal layers. The OPEN structure (Fig. 1(b)) is a similar version of DUT structure but without the intrinsic device. Meanwhile, both THRU L and THRU LL structures (Fig. 1(c)) consist of a metal line connected in between bond pads and are fully shielded (no fixture gap). The line length of THRU LL structure (2L1) is twice of input metal lead (L1) and those of THRU L structure. Extraction of device

Manuscript received January 15, 2011; accepted May 14, 2011. Date of publication July 08, 2011; date of current version August 10, 2011.

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Digital Object Identifier 10.1109/LMWC.2011.2158533

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parameters from DUT measurements requires the fixture parasitics to be known. Here, the OPEN structure is used for characterization of forward coupling parasitics whereas the THRU line structures are used to determine the fixture parasitics that appear at both sides of the embedded device. These test structures could be described by equivalent two-port network models based on their physical layouts. Fig. 2(a) illustrates the network model of DUT structure in cascade-parallel form. Similar to existing cascade based de-embedding techniques, the G-S-G bond pads (PAD, PAD') and interconnect lines (Line L1, Line L2) are modeled as cascade connected networks that appear at both ports (IN, OUT) of the intrinsic device. However, the bond pad parasitic is separated into both series (PS) and parallel (PP) components to address the impact of series contact resistance and pad to ground admittance respectively. Also, additional parallel connected network, FC is used to model the forward coupling that exists in the fixture gap due to direct coupling to the lossy substrate. Note that the DUT model is simplified to OPEN model [Fig. 2(b)] when the embedded device is removed. Meanwhile, both THRU structures are simply cascade connections of bond pads and metal lines of different length [Fig. 2(c)]. Overall, the models provide relationship in between the test structures and parasitic networks. They could be converted into an equivalent form of two-port network matrix [Fig. 2(a)] for mathematical manipulations of noise de-embedding detailed in the following procedure:

1) Convert measured noise parameters ($\mathrm{NF_{min,DUT}}$, $\Gamma_{\mathrm{Opt,DUT}}$ and $\mathrm{R_{n,DUT}}$) of DUT structure to noise correlation matrix (in chain representation), $\mathrm{C_{A,DUT}}$ by method [10]. Measure S-parameters of all test structures ($\mathrm{S_{DUT}, S_{LL}, S_L}$ and $\mathrm{S_{OPEN}}$) and convert them into ABCD matrices ($\mathrm{A_{DUT}}$, $\mathrm{A_{LL}}$, $\mathrm{A_L}$ and $\mathrm{A_{OPEN}}$).
2) Compute ABCD matrix of input parasitic network

$$\mathrm{A_{IN}} = \begin{bmatrix} \frac{4\mathrm{Y_{12R}Y_{11R}A_{12LL}}}{\mathrm{A_{21LL}}-4\mathrm{Y_{11R}^2A_{12LL}}} & \frac{-1}{2\mathrm{Y_{21R}}} \\ \frac{8\mathrm{Y_{12R}Y_{11R}^2A_{12LL}}}{\mathrm{A_{21LL}}-4\mathrm{Y_{11R}^2A_{12LL}}}+2\mathrm{Y_{12R}} & \frac{-\mathrm{Y_{11R}}}{\mathrm{Y_{21R}}} \end{bmatrix}$$

Where, $\mathrm{Y_R} = (\mathrm{Z_L} - \mathrm{Z_M})^{-1}$ and $\mathrm{Z_M}$ is the Z-matrix form of $\mathrm{A_M} = \left(\mathrm{A_L^{-1}A_{LL}}\right)^{-1}$.
3) Compute ABCD matrix of output parasitic network by [11]

$$\mathrm{A_{OUT}} = \mathrm{I}\left(\mathrm{A_{IN}}\begin{bmatrix} \cosh\gamma(\mathrm{L2}-\mathrm{L1}) & \mathrm{Z_C}\sinh\gamma(\mathrm{L2}-\mathrm{L1}) \\ \frac{1}{\mathrm{Z_C}}\sinh\gamma(\mathrm{L2}-\mathrm{L1}) & \cosh\gamma(\mathrm{L2}-\mathrm{L1}) \end{bmatrix}\right)^{-1}\mathrm{I}$$

Where, permutation matrix, $I = \begin{bmatrix} -1 & 0 \\ 0 & 1 \end{bmatrix}$, propagation constant, $\gamma = \cosh^2\mathrm{A_{11L1}}/\mathrm{L1}$, characteristic impedance, $\mathrm{Z_c} = \sqrt{\mathrm{A_{12L1}}/\mathrm{A_{21L1}}}$ and ABCD matrix of Line L1, $\mathrm{A_{L1}} = \mathrm{IA_{IN}^{-1}A_LIA_{IN}}$.
4) Compute ABCD matrix of coupling network with $\mathrm{A_{IN}}$ and $\mathrm{A_{OUT}}$ determined, $\mathrm{A_{FC}} = \mathrm{A_{IN}^{-1}A_{OPEN}A_{OUT}^{-1}}$.
5) Calculate the resultant ABCD matrix, $\mathrm{A_{DEV''}}$ after de-embed the cascade parasitic networks: $\mathrm{A_{DEV''}} = \mathrm{A_{IN}^{-1}A_{DUT}A_{OUT}^{-1}}$.
6) Convert both $\mathrm{A_{DEV''}}$ and $\mathrm{A_{FC}}$ to Y-matrices ($\mathrm{Y_{DEV''}}$ and $\mathrm{Y_{FC}}$) and extract the admittance matrix of the intrinsic device, $\mathrm{Y_{DEV}}$: $\mathrm{Y_{DEV}} = \mathrm{Y_{DEV''}} - \mathrm{Y_{FC}}$.

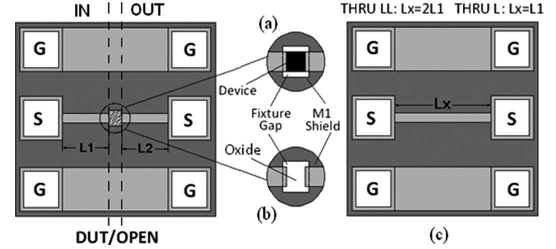

Fig. 1. (a) DUT structure consisting of device (e.g., NMOS) to be characterized. (b) OPEN structure is a shielded fixture frame (no device). (c) THRU L and THRU LL structures have metal lines of different lengths $(\mathrm{L1}, 2\mathrm{L1})$. (a) DUT. (b) OPEN. (c) THRU L/LL.

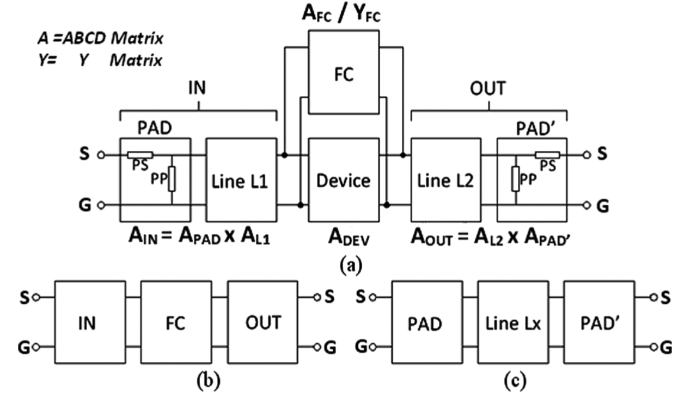

Fig. 2. (a) DUT structure modeled as cascade-parallel combinations of 2-port device and parasitic networks. (b) OPEN model is another version of DUT model with no device. (c) Cascade network model of THRU L and THRU LL structures includes pads and metals lines. (a) DUT. (b) OPEN. (c) THRU L/LL.

7) Calculate noise correlation matrices of parasitic networks in admittance form, $\mathrm{C_{Y,IN}}$, $\mathrm{C_{Y,OUT}}$ and $\mathrm{C_{Y,FC}}$ from their Y-matrices ($\mathrm{Y_{IN}}$, $\mathrm{Y_{OUT}}$ and $\mathrm{Y_{FC}}$) [12]. Then, convert both $\mathrm{C_{Y,IN}}$ and $\mathrm{C_{Y,OUT}}$ into equivalent cascade representation, $\mathrm{C_{A,IN}}$, $\mathrm{C_{A,OUT}}$: $\mathrm{C_{A,IN}} = \mathrm{T_{IN}C_{Y,IN}T_{IN}^H}$ and $\mathrm{C_{A,OUT}} = \mathrm{T_{OUT}C_{Y,OUT}T_{OUT}^H}$ where, $\mathrm{T_{IN}} = \begin{bmatrix} 0 & \mathrm{A_{12IN}} \\ 1 & \mathrm{A_{22IN}} \end{bmatrix}$, $\mathrm{T_{OUT}} = \begin{bmatrix} 0 & \mathrm{A_{12OUT}} \\ 1 & \mathrm{A_{22OUT}} \end{bmatrix}$ and superscript H denotes Hermitian complex conjugate transpose.
8) De-embed noise correlation matrix of cascade parasitic networks

$$\mathrm{C_{A,DEV''}} = \mathrm{A_{IN}^{-1}}(\mathrm{C_{A,DUT}} - \mathrm{C_{A,IN}})(\mathrm{A_{IN}^H})^{-1} - \mathrm{A_{DEV''}C_{A,OUT}A_{DEV''}^H}.$$

9) Convert $\mathrm{C_{A,DEV''}}$ to $\mathrm{C_{Y,DEV''}}$ and de-embed noise correlation matrix of parallel parasitic network, $\mathrm{C_{Y,FC}}$: $\mathrm{C_{Y,DEV}} = \mathrm{C_{Y,DEV''}} - \mathrm{C_{Y,FC}}$ where $\mathrm{C_{Y,DEV''}} = \mathrm{T_{DEV''}C_{A,DEV''}T_{DEV''}^H}$ and $\mathrm{T_{DEV''}} = \begin{bmatrix} -\mathrm{Y_{11DEV''}} & 1 \\ -\mathrm{Y_{21DEV''}} & 0 \end{bmatrix}$.
10) Lastly, convert $\mathrm{C_{Y,DEV}}$ to $\mathrm{C_{A,DEV}}$ and calculate the noise parameters of the intrinsic device ($\mathrm{NF_{min,DEV}}$, $\Gamma_{\mathrm{Opt,DEV}}$ and $\mathrm{R_{n,DEV}}$) by applying method [10]: $\mathrm{C_{A,DEV}} = \mathrm{T_{DEV}C_{Y,DEV}T_{DEV}^H}$ Where, $\mathrm{T_{DEV}} = \begin{bmatrix} 0 & \mathrm{A_{12DEV}} \\ 1 & \mathrm{A_{22DEV}} \end{bmatrix}$.

III. RESULTS AND DISCUSSION

Verification on zero-length THRU device provides an intuitive way to justify the accuracy of de-embedding technique due

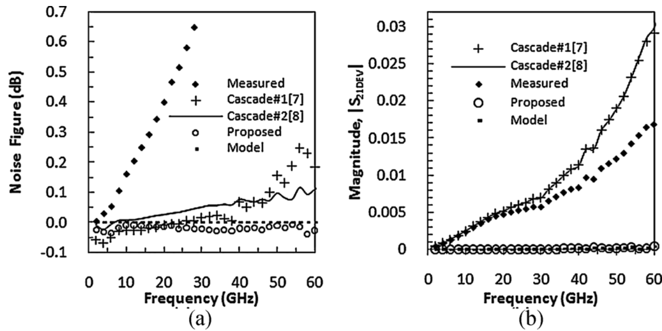

Fig. 3. Measured (before de-embedding) and de-embedded (a) noise figure of THRU device and (b) $|S_{21DEV}|$ (Magnitude of S-parameter, S_{21DEV}) of OPEN device versus frequency.

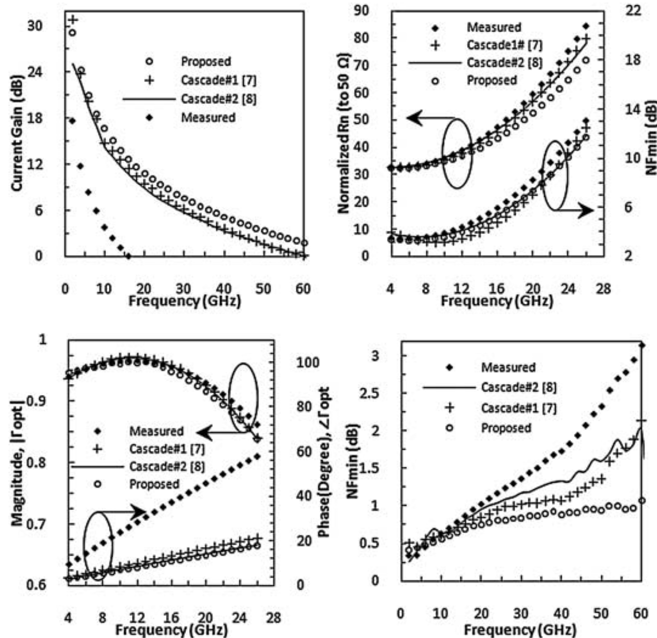

Fig. 4. Measured (before de-embedding) and de-embedded (a) current gain and noise parameters ((b) $\mathrm{NFmin}, \mathrm{Rn}$, (c) $\Gamma\mathrm{opt}$) of 0.13 $\mu\mathrm{m}$ NMOS device versus frequency for dc bias of $\mathrm{Vgs} = \mathrm{Vds} = 1.2\ \mathrm{V}$. (d) Measured and de-embedded NFmin of 0.13 $\mu\mathrm{m}$ NMOS device versus frequency at $\mathrm{Vgs} = \mathrm{Vds} = 0\ \mathrm{V}$.

to its simple defined characteristic. It could be de-embedded from THRU line structure that has the same total line length as the DUT structure (L1 + L2). The de-embedded THRU device should be ideal (0 dB noise figure) since it is parasitic free. As shown in Fig. 3(a), the proposed de-embedding technique shows better prediction in noise figure ($-20\log|S_{21DEV}|$) of the THRU device than [7], [8] and is thus more accurate. The de-embedding verification discussed is further extended to OPEN device. Note that the de-embedded OPEN by techniques [7], [8] shown in Fig. 3(b) are associated with forward coupling component that becomes dominant at high frequencies ($|S_{21DEV}| > -40\ \mathrm{dB}$ at 40 GHz). In contrast, the de-embedded OPEN by proposed technique is ideal ($|S_{21DEV}| \approx 0$) since the forward coupling effect is corrected. As shown in Fig. 4(a), the superiority of proposed de-embedding technique over [7], [8] has resulted in better prediction on current gain performance of 0.13 $\mu\mathrm{m}$ transistor by 1.5 dB at 60 GHz. Based on these verification results, the proposed de-embedding technique is further demonstrated for noise characterization of 0.13 $\mu\mathrm{m}$ NMOS device with ATN 2–26 GHz noise measurement system. As expected, the noise de-embedding performance of proposed technique agrees well with others [7], [8] for frequencies below 26 GHz [Fig. 4(b)–(c)] due to negligible impact of forward coupling and contact resistance. Validation on noise figure performance of transistor beyond 26 GHz is extracted directly from measured S-parameters [12] when it operates in passive mode ($\mathrm{Vgs} = \mathrm{Vds} = 0\ \mathrm{V}$). As shown in Fig. 4(d), the high frequency advantage of proposed de-embedding technique over others [7], [8] becomes obvious at frequencies beyond 25 GHz and approaches 1 dB at 60 GHz. Overall, the proposed noise de-embedding technique is more suitable than [7], [8] in noise characterization of RF devices at millimeter-wave frequencies.

IV. Conclusion

An accurate THRU-OPEN based noise de-embedding technique is presented. It is developed based on mix cascade-parallel configuration of the test fixture model which allows both distributed parasitics of interconnect and forward coupling effect to be taken into consideration concurrently. The proposed de-embedding technique is validated and has been shown to be more accurate than existing cascade based de-embedding techniques [7], [8]. This corresponds to 1 dB improvement in predicted NFmin of the 0.13 $\mu\mathrm{m}$ NMOS device at 60 GHz. Thus, it is recommendable for noise characterization of lossy devices at RF/millimeter-wave frequencies.

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