A CMOS W-band 4× Quasi-Subharmonic Mixer

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***Abstract*—This paper reports a 4× W-band quasi-subharmonic down-conversion mixer in a 65 nm CMOS technology. Developed from subharmonic mixers, this mixer saves trouble in designing phase-shifters and works well within W-band. Down-conversion is achieved by capturing the phase difference between two sine waves at every half cycle of the local oscillator. The power gain is above 3.5 dB over the entire W-band. The minimum noise figure is 12.5 dB, and the 1-dB compression point is -1.2 dBm.**

***Index Terms*—subharmonic, millimeter-wave, CMOS mixer**

I. Introduction

SYSTEMS operating in the millimeter-wave bands would prevail in daily life. Millimeter-wave radiometers are used in many applications, but unlike X-ray scanners, they pose no risk of harm to humans. Communication systems are also expanding their frontiers to the millimeter-wave range, as evidenced by *IEEE 802.15.3c*, *IEEE 802.11ad* and the impending 5G cellular networks [1], [2]. In these systems, the receiver plays an important role. It demodulates the received millimeter-wave frequency to a lower frequency, Δω, by using a mixer driven by a local oscillator (LO). In practice, however, it is difficult to build an LO at the extremes of frequency, especially for CMOS technologies. To address such an issue, a subharmonic mixer could be used in lieu of conventional mixers. Compared with conventional mixers driven at an LO frequency, ω_{LO}, the subharmonic mixer only needs one-half or even less of that LO frequency. [3] explains the working principle of a conventional 4× CMOS subharmonic mixer. The mixer in [3] is driven by LO signals with quadrature-phases. The quadrature-phases are generated by phase-shifters. However, the phase-shifter, typically a coupler, becomes a new burden for designers, because it occupies a large chip area and requires many EM simulation iterations [4]. Another issue associated with some subharmonic mixers is their low conversion gain [5], because the enhanced amplitudes of higher harmonics are normally smaller than the fundamental's. The subsampling mixer [6] could be used to relax the requirement on the LO side as well. Its scheme is based on the observation that the information bandwidth of modulation is necessarily lower than the carrier frequency. One may satisfy the Nyquist criterion with a sampling rate that is lower than the carrier frequency to down-convert the input signal. However, a train of impulses is created in the frequency domain as well, which simultaneously folds the noise at the multiples of the sampling rate into the baseband during the sampling process.

This paper reports a W-band 4× CMOS quasi-subharmonic mixer. The design method is based on the general description for subharmonic mixers. The topology and LO driving signals are similar to conventional ones. However, the down-conversion process is completed by trimming the input signal rather than by superposing or pumping the higher order of harmonics, wherein lies the reason for the prefix, "quasi-". Section II describes the design method. Section III exhibits the experimental results. A conclusion is drawn in Section IV.

II. Circuit Design

From a mathematical view, a 4× subharmonic mixer could be described as:

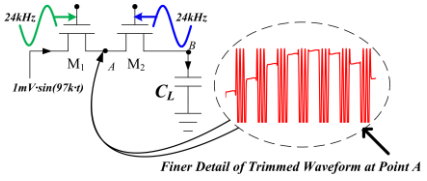
$$v_{out} = A_{out}\, sin[(\omega_{in} - 4 \cdot \omega_{LO}) \cdot t] = A_{out}\, sin(\Delta\omega \cdot t), \quad (1)$$

where v_{out} is the output voltage, and A_{out} is its amplitude.

Similarly, the input voltage can be expressed as:

$$v_{in} = A_{in} sin\left(4 \cdot \frac{2\pi}{T_{LO}} \cdot t + \Delta\omega \cdot t\right), \quad (2)$$

where T_{LO} is the time-period of the local oscillator. Equation (2) carries useful information, from which the design inspiration is derived. Assuming that A_{in} is a constant, the value of v_{in} at each time t is determined by its phase change. The phase change is due to two parts, i.e. $4 \cdot \frac{2\pi}{T_{LO}} \cdot t$ and $\Delta\omega \cdot t$. Interestingly, once t is a multiple of $\frac{T_{LO}}{2}$, the value of v_{in} is only decided by the latter part, because $4 \cdot \frac{2\pi}{T_{LO}} \cdot t$, at that time, is just a multiple of 2π. In other words, the value of v_{in} is modulated by $sin(\Delta\omega \cdot t$ at every half LO-cycle. Therefore, if v_{in} can be properly trimmed, a loss-less mixer becomes possible by tracking the values of v_{in} at the moment when t is a multiple of $\frac{T_{LO}}{2}$. A circuit consisting of two NMOS transistors in tandem could meet such an expectation. For the sake of developing an intuitive feel, a specific example from the simulation is given in Fig. 1.



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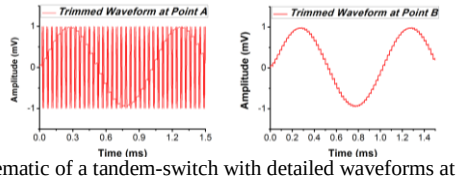


Fig. 1. Schematic of a tandem-switch with detailed waveforms at A and B.

In the particular case shown in Fig. 1, the tandem-switch trims a 1-mV sinusoid alternately, which yields a 1-mV demodulated-sinusoid at the output. Its working principle can be analyzed as follows. As shown on the left side in Fig. 2, the differential LO applied to each gate creates a time-interval, ΔT. ΔT repeats itself by every half LO-cycle. Within ΔT, both switches are "on". The current can charge the capacitor. Outside ΔT, the current stops charging, because at least one of the switches is turned off. The capacitor will hold the stored charge for a period of T_{hold}. The T_{hold} and ΔT depend on the bias voltage, V_{bias}. As shown on the right side of Fig. 2, a high bias voltage reduces T_{hold} but increases ΔT.

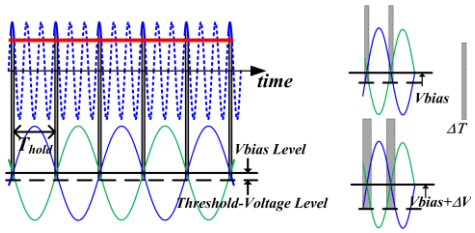


Fig. 2. Snapshot captured when ω_{in} is a multiple of ω_{LO}, with details on LO.

If the frequency of ω_{in} is a multiple of ω_{LO}, charges stored by the capacitor remain the same. The voltage on the capacitor is the area of the shadowed region divided by ΔT, as represented in Fig. 2 by a straight line in red. When ω_{in} is no longer a multiple of ω_{LO}, the charge stored by the capacitor starts to vary in a sinusoidal form, as shown in Fig. 3.

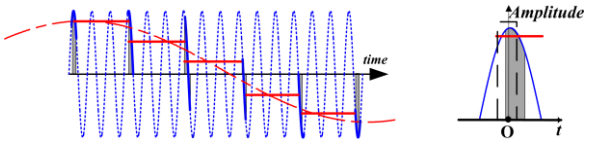


Fig. 3. Time domain waveforms used to explain the output waveform.

An intuitive way to think about this is as follows. Imagine that one is at point B in Fig. 1 and starts to record the values of v_{in}, which are on the other side of the tandem-switch. The value change of v_{in} can be monitored only at every half LO-cycle, when both switches are turned on. Otherwise, nothing could be recorded, since at least one switch is placed in the "off" state, which cuts off the path from the input to the output. Therefore, referring to (2), the recorded points belong to $sin(\Delta\omega \cdot t)$ only. The principle can be analyzed in the frequency domain as well. The repeating pattern of ΔT is similar to a Dirac comb. The Fourier transform of ditto is also a Dirac comb, spaced at intervals of $\frac{2}{T_{LO}}$ in the frequency domain. The down-conversion process is accomplished by utilizing its second harmonic component at the frequency of $4\omega_{LO}$. Fig. 3 helps with estimating the amplitude of the demodulated signal, A_{out}. Neglecting the frequency-offset and assuming that the center of ΔT is at the origin, one can have,

$$A_{out} \approx \frac{\int_{-\frac{\Delta T}{2}}^{\frac{\Delta T}{2}} A_{in} sin(\omega_{in} \cdot t + \frac{\pi}{2}) dt}{\Delta T} = \frac{\int_{-\frac{\Delta T}{2}}^{\frac{\Delta T}{2}} A_{in} sin\,(\frac{2\pi}{T_{in}} \cdot t + \frac{\pi}{2}) dt}{\Delta T}, \quad (3)$$

where T_{in} is the time-period of the input. Fig. 4 plots (3) as a function of $\Delta T/T_{in}$. As one may notice, in the extreme cases where ΔT is just a few instants of T_{in}, there is almost no difference between A_{out} and A_{in}. However, synchronization suffers at the same time.

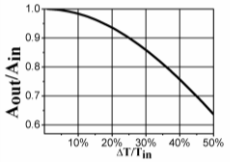


Fig. 4. Plot of A_{out}/A_{in} versus $\Delta T/T_{in}$.

Fig. 5 shows the schematic of the proposed mixer. A balanced topology is adopted in order to cancel the leakage current from LO at point B in Fig. 5. To relieve the issue of unequal threshold-voltages caused by body-effect, triple-well transistors are used. Conductance for a 20x1 µm-gate-width is about 1/20-Siemens. An IF amplifier, also used as a buffer, matches the output to 50 Ω. Its -3-dB bandwidth is from DC to 12 GHz. The AC gain-level falls below 10 dB thereafter. The LO power is chosen to be 10 dBm.

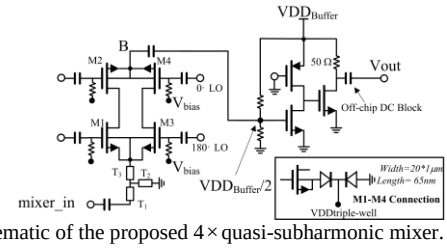


Fig. 5. Schematic of the proposed 4× quasi-subharmonic mixer.

The values of ΔT and T_{hold} are controlled by the bias condition. As mentioned earlier, a small ΔT yields a high average value. Additionally, T_{hold} also has effects on gain. Practically, the capacitor can only hold the charge for a limited duration, since the amount of stored charges would decrease exponentially within T_{hold}. As sketched on the left side of Fig. 6, a small ΔT averages a high value for (3) but increases T_{hold}, aiding the leakage. A large ΔT reduces T_{hold} but lowers the average value of (3). An optimized point for biasing thereby exists. As can be seen on the right side of Fig. 6, referring to the circuit in Fig. 5, when V_{bias} is 750 mV, for a 1 mV, 97 GHz input at the input node "mixer_in", v_B at 1 GHz is 615 µV. In other words, the loss from point B to the input node "mixer_in" is 4.2 dB.

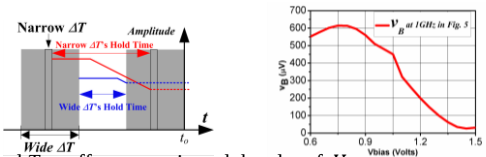
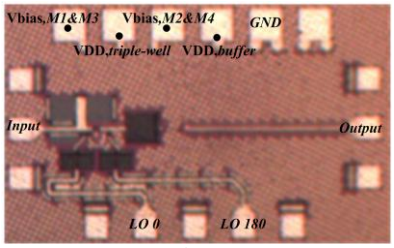


Fig. 6. ΔT and T_{hold} effects on gain and the plot of V_{bias} versus v_B-at-1-GHz.

III. Measurement Results

Fig. 7 shows the micrograph of the proposed mixer using the GLOBAL-FOUNDRIES 65 nm CMOS technology. The area

including the pads is 0.78 x 0.48 mm^2. We assign the DC pads conservatively, in order to fine-tune the mixer. However, based on the results assorted in Fig. 7, two DC pads are already enough. The W-band signal fed into the mixer comes from an R&S SMF100A signal generator. It is connected by a 6x frequency multiplier and an attenuator. An R&S ZVA67 network analyzer is used to generate the differential LO drive. The noise source is an ELVA ISSN-10, which covers the entire W-band. The passive mixer consumes a DC-power of 17 mW to drive the buffer stage.



Vbias, *M1&M3*	**0.75V**
Vbias, *M2&M4*	**0.75V**
VDD-triple well	**1.5V**
VDD-buffer	**1.5V**

Fig. 7. Micrograph of the proposed mixer and its corresponding DC bias.

The measured results agree well with the simulated. As shown in Fig. 8, the mixer can operate over a wide frequency range. The -3-dB bandwidth is from 79 GHz to 110 GHz. The mixer keeps its gain-level above 3.75 dB over the entire W-band. The peak gain is 8.1 dB at 93 GHz. Its noise performance is satisfactory as well. As shown in Fig. 9(a), the minimum double-sideband (DSB) noise figure (NF) is 12.5 dB at IF=2 GHz. Noise could be further suppressed, if a gain stage is applied at the input [6]. Fig. 9(a) also plots the effect of the frequency offset when it is applied to the mixer. In reality, a fading channel or an LO mismatch between the transmitter and the receiver may cause such a problem. To evaluate this effect, the LO frequency is fixed at 24 GHz, and the input frequency is swept from 97 GHz to 110 GHz. As plotted in Fig. 9(a), the gain of the mixer stays above 0 dB when the frequency offset is increased to 5.5 GHz. The measured output power-compression-point (OP1dB) is -1.2 dBm when the input frequency is 97 GHz, as shown in Fig. 9(b). The measured LO-to-RF/LO-to-IF/RF-to-IF isolations are 55/63/34 dB when the frequency of LO/RF is 24/97 GHz. The proposed mixer is not intended to strengthen the fourth harmonic at the LO-port. Moreover, its passive nature suppresses the current-growth at the frequency of 2LO or 4LO. Therefore, 2LO-RF and 4LO-RF are not considered as measures to judge the mixer performance. Taken as a supplement, the measured power, at 48 GHz (2LO) and 96 GHz (4LO), at the RF-port, is -31 dBm and -53 dBm, respectively. This weak power, far beyond the baseband, could neither radiate from the antenna nor affect following stages at the baseband. Table I summarizes and compares the designed mixer's performance with other CMOS mixers in W-band.

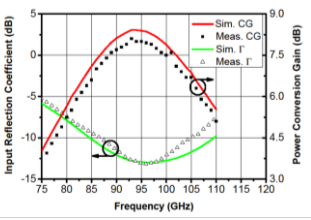
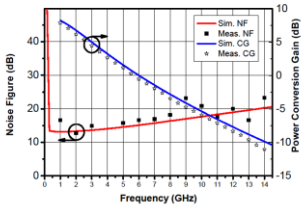
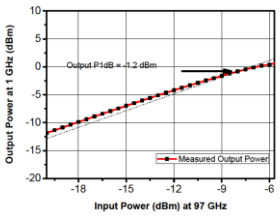


Fig. 8. Measured power conversion gain (CG) and input reflection coefficient (Γ) versus RF frequency with LO power set to 10 dBm.



(a)



(b)

Fig. 9. Measured (a) NF (DSB), CG vs. frequency offset, and (b) P1dB, with the LO power set to 10dBm.

TABLE I
PERFORMANCE COMPARISON OF W-BAND MIXERS

Ref.	Process	Freq. (GHz)	Gain (dB)	NF (dB)	OP1dB (dBm)	Power (mW)
[4]	CMOS 65 nm	5-75	>3	14.6	N/A	3
[7]	CMOS 65 nm	74-98	6	8	-16.5	N/A
[8]	CMOS 90 nm	40-108	-1.5	11	-14.5	2
[9]	CMOS 90 nm	35-83	0.5	N/A	-0.5	6.5
This Work	CMOS 65 nm	79-110	8	12.5	-1.2	17

IV. Conclusion

A W-band mixer in a CMOS 65 nm technology has been presented. It is of low loss, high linearity, and has a moderate noise figure. The principle is simple and straightforward, and it saves trouble in designing the phase-shifters. Moreover, by expanding the proposed method, it is possible to design a subharmonic mixer of higher orders, which could be a potential solution for down-converting Terahertz frequencies.

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