A 71 dB 150 μW Variable-Gain Amplifier in 0.18 μm CMOS Technology

Hang Liu, Xi Zhu, Chirn Chye Boon, Xiang Yi and Lingshan Kong

***Abstract*— This letter presents a simple approach for ultra-low-power and high-frequency variable gain amplifier (VGA) design, which requires no additional circuitry to generate the exponential-like function. Thus, the power consumption and chip area of the designed VGA can be drastically reduced without deterioration of other performance. The inverse exponential-like dB-linear characteristic is achieved by utilizing a pair of complementary transistors as the load. The p-MOS transistor is self-biased in the saturation region, while the n-MOS transistor is biased in the sub-threshold region. To prove the concept, a five-cell VGA is fabricated in a standard 0.18 μm CMOS technology. The measurements show that the power consumption of the VGA is less than 150 μW and achieves a total gain range of 71 dB, out of which 45 dB is dB-linear with less than 1 dB gain error, as well as bandwidth of more than 50 MHz. The output P_{1dB} is better than 0 dBm and the minimum input-referred noise is 7.5 $nV/\sqrt{Hz}$.**

***Index Terms*— CMOS variable-gain amplifier, dB-linear, ultra-low power.**

I. Introduction

A variable-gain amplifier (VGA) is one of the critical components in modern wireless transceiver designs [1-9]. Based on different gain switching/tuning mechanisms, VGA can be categorized as digital controlled (DVGA) and analog controlled (AVGA). Although the specifications of a VGA can vary significantly in terms of bandwidth, power consumption, noise and linearity for different applications, common specifications of the VGA are to provide a reasonable gain range with an accurate dB-linear characteristic. Although the DVGA can have a relatively larger gain range with smaller gain error [2, 3], it is difficult to achieve small gain steps due to the limited number of control bits. In contrast, the AVGA can provide continuous gain tuning, although the gain error may be larger than its DVGA counterpart. In this letter, VGA refers to AVGA. To minimize the gain error, extensive attention is given to the implementation of an exponential function [4-9].

Our previous work in [9] has demonstrated that a "cell-based" approach can be used to design a VGA with an accurate dB-linear characteristic. A novel "cell" structure has been presented to demonstrate the capability of the "cell-based" approach. To achieve an accurate dB-linear characteristic, the body-biased mechanism is employed. In this letter, another novel "cell" structure is presented, which uses the gate-biased mechanism. Consequently, the proposed VGA consumes much less power than many other state-of-the-art designs in the literature, while the other characteristics are not significantly deteriorated. The rest of the letter is organized in the following way. In Section II, the principle of the proposed approach is introduced. To prove the concept, a unit cell and a cascaded 5-cell VGA are fabricated and the measurement results are shown in Section III. In Section IV, conclusions are drawn.

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II. The Principle of the Proposed VGA Approach

A. Design of the Low-Power Unit Cell

Both the block diagram of the cascaded VGA and the schematic of the proposed unit cell are shown in Fig. 1. In contrast to conventional designs, a combination of p-MOS and n-MOS transistors are used as the active load. To compensate the gain error, the n-MOS transistors, M_1 and M_2, are biased in the sub-threshold region while the diode-connected p-MOS transistors, M_3 and M_4, are self-biased in the saturation region. M_5 and M_6 are a differential pair with input signal applied at their gate nodes and output signal taken from their drain nodes. M_7 is the current source providing the bias conditions.

By inspection, the gain is derived as:

$$A_v = \frac{v_{out}}{v_{in}} = \frac{g_{m,5,6}}{g_{m,1,2} + g_{m,3,4}}, \quad (1)$$

where g_m is the transconductance of the respective transistor. If the bias condition of the input differential pair is fixed, then the relationship between $I_{DS,1,2}$ and $I_{DS,3,4}$ can be expressed as:

$$I_{DS,5,6} = I_{DS,1,2} + I_{DS,3,4}. \quad (2)$$

If the n-MOS transistors, M_1 and M_2, are biased in the sub-threshold region, then $g_{m,1,2}$ can be expressed as:

$$g_{m,1,2} = \frac{2I_{DS,1,2}}{nV_T}. \quad (3)$$

Meanwhile, if the p-MOS transistors, M_3 and M_4, are biased in the saturation region, then $g_{m,3,4}$ can be expressed as:

$$g_{m,3,4} = \frac{2I_{DS,3,4}}{V_{OV,3,4}}. \quad (4)$$

where $V_{OV,3,4}$ is the overdrive voltage of M_3 and M_4. As the current flowing through M_5 and M_6 is constant, $g_{m,5,6}$ should be constant regardless of the condition of $I_{DS,1,2}$ and $I_{DS,3,4}$. If a

control voltage, V_{CTRL}, is applied to the gate terminal of the transistors M_1 and M_2, then the overall voltage gain A_v with the change in g_m represented as Δg_m can be rewritten as:

$$A_v = \frac{g_{m,5,6}}{g_{m,1,2} + g_{m,3,4} + \Delta}, \quad (5)$$

where $\Delta = \Delta g_{m,1,2} + \Delta g_{m,3,4}$. Substituting (3) and (4) into Δ leads to:

$$\Delta = \frac{2\Delta I_{DS,1,2}}{nV_T} + \frac{2I_{DS,3,4}}{V_{OV,3,4} + \Delta V_{OV,3,4}} \left(\frac{\Delta I_{DS,3,4}}{I_{DS,3,4}} - \frac{\Delta V_{OV,3,4}}{V_{OV,3,4}} \right). \quad (6)$$

The basic p-MOS I-V equations for M_3 and M_4 with channel-length modulation neglected can be written as:

$$I_{DS,3,4} = \frac{1}{2} \mu_P C_{ox} \left(\frac{W}{L} \right)_{3,4} V_{OV,3,4}^2. \quad (7)$$

As the total current remains unchanged, $\Delta I_{DS,1,2} = -\Delta I_{DS,3,4}$. The percentage change in $I_{DS,3,4}$ is larger than the percentage change in $V_{OV,3,4}$ due to their quadratic relationship as shown in (7) and of the same polarity, and since $V_{OV,3,4} + \Delta V_{OV,3,4}$ is always much larger than nV_T due to their different operation region, the following inequality is established:

$$\left| \frac{2I_{DS,3,4}}{V_{OV,3,4} + \Delta V_{OV,3,4}} \left(\frac{\Delta I_{DS,3,4}}{I_{DS,3,4}} - \frac{\Delta V_{OV,3,4}}{V_{OV,3,4}} \right) \right| < \left| \frac{2\Delta I_{DS,3,4}}{V_{OV,3,4} + \Delta V_{OV,3,4}} \right| \ll \left| \frac{2\Delta I_{DS,1,2}}{nV_T} \right| \quad (8)$$

Thus the second term in Δ can be ignored and the gain can be approximated as:

$$A_v \approx \frac{g_{m,5,6}}{g_{m,1,2} + g_{m,3,4} + \frac{2\Delta I_{DS,1,2}}{nV_T}}. \quad (9)$$

$\Delta I_{DS,1,2}$ can be expressed as:

$$\Delta I_{DS,1,2} = \frac{\kappa}{nV_T} I_{O,1,2} \left(\frac{W}{L} \right)_{1,2} exp \left(\frac{\kappa V_{G,1,2} - V_{S,1,2}}{nV_T} \right) \Delta V_{G,1,2}. \quad (10)$$

where $I_{O,1,2}$ is the sub-threshold current constant, κ is the gate coupling coefficient and can be treated as 0.7 throughout the sub-threshold region. The control voltage, V_{CTRL}, is applied at $V_{G,1,2}$ and the overall gain A_v is close to an inverse exponential function for an appropriate V_{CTRL} range. The design procedure of the unit cell can be summarized as follows. First of all, according to the required power consumption, the sizes of the input transistors, M_5 and M_6, can be chosen. Secondly, the selection of the size of M_3 and M_4 can be made based on the required gain of the unit cell. Finally, the size of M_1 and M_2 can be optimized accordingly. As illustrated in Fig. 2, the dB-linear gain range and gain error are dependent on the size of M_1 and M_2. Simulation results show that the unit cell only consumes 16 µA from a 1.8 V power supply, while a gain error of 0.2 dB over a dB-linear voltage gain range of 9 dB is achieved.

B. Design of the Cascaded VGA with the Unit Cell

The number of unit cells to be cascaded is determined according to the system specification. From a practical design point of view, a DC-coupled VGA can be designed for compactness and simplicity. However, the frequency response of such a VGA may suffer from the DC-offset issue. On the other hand, an AC-coupled VGA with common-mode bias voltage applied at each stage can handle much larger DC-offset even with a high gain setting, although it occupies a relatively larger area than the DC-coupled one. Thus, it guarantees the final yield. To demonstrate the usefulness of the cascaded VGA, an AC-coupled 5-cell VGA is presented.

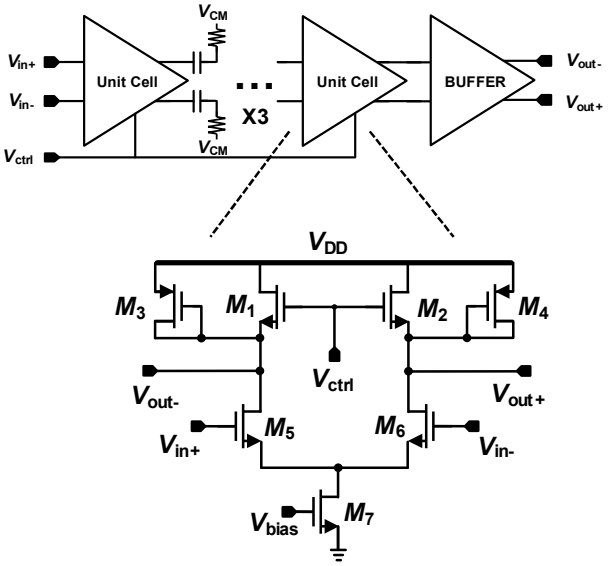

Fig. 1. Block diagram of the 5-cell VGA with the proposed unit cell, size in µm: $M_{1,2} = 5/0.36, M_{3,4} = 1/1, M_{5,6} = 4/0.36, M_7 = 3/0.36$.

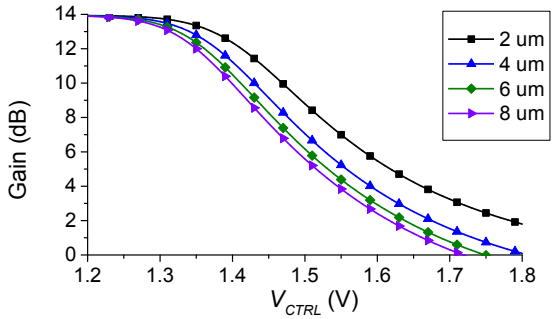

Fig. 2. Simulated gain of the unit cell vs. width of M_1 and M_2.

III. Fabrication and Measurement

To verify the performance, the VGA presented in Fig. 1 is fabricated in Globalfoundries' 0.18 µm CMOS technology. The on-wafer measurement was performed using an Agilent E8364B vector network analyzer, which operates from 10 MHz to 50 GHz. In order to drive the 50 Ω vector network analyzer, a differential buffer was included after the VGA and was fabricated separately. The buffer is measured to have 16 dB of attenuation. In the following discussion, the attenuation of the buffer is always de-embedded from the measurement, so that the performance of the "core" circuit can be effectively reflected. Moreover, a fixed 20 MHz signal is used for all of the dB-linear gain characterization, output 1-dB compression (OP_{1dB}) and input-referred noise (IRN) measurements.

Fig. 3 shows the measured and simulated dB-linear gain characteristics of the cascaded VGA. A voltage gain range of

71 dB is measured, of which 45 dB is dB-linear with less than 1 dB gain error. The power consumption of the cascaded 5-cell VGA is only 81 µA under a 1.8 V power supply. Moreover, the measured frequency responses of the designed VGA against V_{CTRL} are shown in Fig. 4. The bandwidth varies from 50 MHz to 209 MHz while the gain setting is varied from the highest to the lowest.

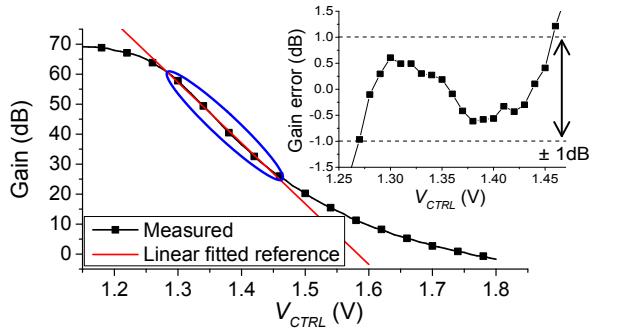

Fig. 3. Measured gain characteristics and gain error for the 5-cell VGA.

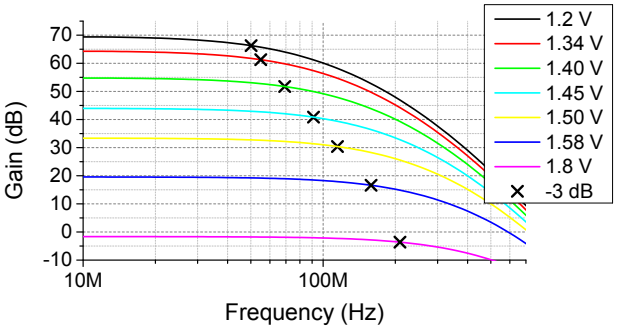

Fig. 4. Measured frequency response for the 5-cell VGA.

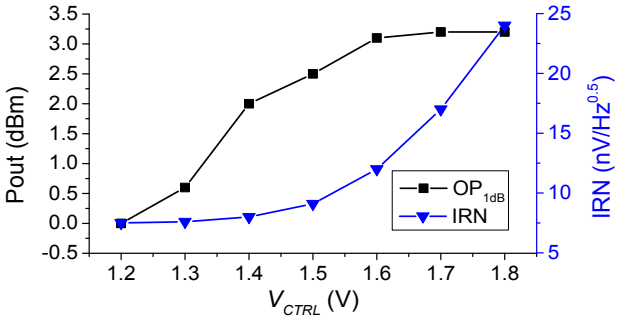

Fig. 5. Measured OP_{1dB} and IRN vs. V_{CTRL} for the 5-cell VGA.

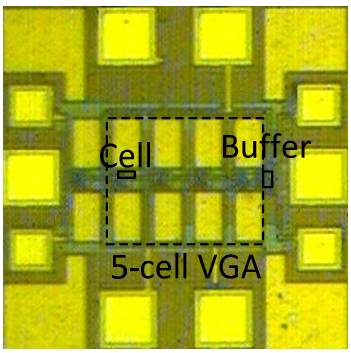

Fig. 6. Die photo of the fabricated 5-cell VGA, size in µm^2: VGA 200×170, unit cell 24×7, buffer 43×30.

Moreover, both the measured OP_{1dB} and IRN vs. V_{CTRL} are presented in Fig. 5. As can be seen from Fig. 5, the OP_{1dB} is around 0 dBm, while the minimum IRN is 7.5 $nV/\sqrt{Hz}$ at the highest gain setting. Fig. 6 shows die photo of the fabricated VGA. It can be seen that the unit cell is very compact and the main area-consuming block is the AC-coupling capacitors. Even with the AC-coupling circuitry, the size is still comparable to other published VGAs. A comparison of the proposed VGA with recently published work is summarized in Table I.

TABLE I
COMPARISONS WITH OTHER STATE-OF-THE-ART DESIGNS

	[5]	[6]	[7]	[8]	[9]	**This work**
DC power (mW)	2.2	5	6.5	2.2	0.74	**0.15**
f_{-3dB} (MHz)	40	76	32	15	149	**50**
Gain range (dB)	65	65	95	76	39	**71**
dB-lin. gain (dB)	40	40	95	50	39	**45**
Gain error (dB)	0.8	1	1	0.5	0.2	**1**
OP_{1dB} (dBm)	12*	2.3	-7	2*	-3	**0**
IRN ($\mathbf{nV/\sqrt{Hz}}$)	11	n/a	n/a	3.5	10.6	**7.5**
Technology (nm)	65	180	180	65	180	**180**

*Estimated from IP3 result

IV. CONCLUSIONS

In this letter, a simple approach is presented for the design of ultra-low power and high frequency VGA. To illustrate the proposed approach, the design and analysis of a unique unit cell has been presented, utilizing complementary devices as the load. Since this unit cell requires no extra circuit to generate an exponential-like function, it drastically reduces the power consumption. Therefore, the presented approach is suitable for many applications where ultra-low power, high frequency and an accurate dB-linear characteristic are required.

REFERENCES

[1] B. Razavi, *RF Microelectronics,* 2nd ed., Upper Saddle River, NJ: Prentice-Hall, 2013.

[2] S. Y. Kang , Y. Jang , I. Y. Oh and C. S. Park, "A 2.16 mW low power digitially-controlled variable gain amplifier", *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 3, pp.172 -174, 2010.

[3] S. Y. Kang, S. T. Ryu and C. S. Park "A precise decibel-linear programmable gain amplifier using a constant current-density function," *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 9, pp. 2843-2850, Sep. 2012.

[4] C. Garcia-Alberdi *et al,* "Micro-power class-AB VGA with gain-independent bandwidth," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 60, no. 7, pp. 397-401, Jul. 2013.

[5] H. Elwan, A. Tekin and K. Pedrotti, "A differential-ramp based 65 dB-linear VGA technique in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2503–2514, Sep. 2009.

[6] Z. Chen, Y. Zheng, F. C. Choong and M. Je, "A low-power variable gain amplifier with improved linearity: analysis and design," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 10, pp. 2176-2185, Oct. 2012.

[7] Q. H. Duong, L. Quan, C. W. Kim and S. G. Lee, "A 95-dB linear low-power variable gain amplifier," *IEEE Trans. Circuits Syst. I, Reg. Papers,* vol. 53, no. 8, pp. 1648-1658, Aug. 2006.

[8] I. Choi, H. Seo and B. Kim, "Accurate dB-linear variable gain amplifier with gain error compensation," *IEEE J. Solid-State Circuits*, vol. 48, no. 2, pp. 456–464, Feb. 2013.

[9] H. Liu, X. Zhu, C. C. Boon and X. F. He, "Cell-based variable gain amplifiers with accurate dB-linear characteristic in 0.18 um CMOS technology," *IEEE J. Solid-State Circuits*, vol. 50, no. 2, pp. 1–11, Feb. 2015.