

A 50–59 GHz CMOS Injection Locking Power Amplifier

Jiafu Lin, *Student Member, IEEE*, Chirn Chye Boon, *Senior Member, IEEE*, Xiang Yi, *Student Member, IEEE*, and Guanyin Feng, *Student Member, IEEE*

Abstract—The injection-locked power amplifier (ILPA) has demonstrated relatively high gain and high efficiency at millimeter-wave frequency. However, their application is still limited by its sensitivity to loading effect and narrow injection locking bandwidth. In this letter, a wide injection locking ILPA using buffered input and output has been proposed and implemented on 65 nm CMOS technology. The buffered input and output can improve the injection locking range and avoid load-to-tank pulling. The measured injection locking range is from 50 GHz to 59 GHz and the peak Power Added Efficiency (PAE) is 16.1% with a maximum output power of 11.39 dBm. Moreover, the die size is merely $260 \mu\text{m} \times 400 \mu\text{m}$ excluding pads.

Index Terms—CMOS power amplifier (PA), injection locking, low power, power added efficiency (PAE), V-band.

I. INTRODUCTION

DUE to the fast growing demand of wireless communication, the CMOS transceiver has been developed and becomes available for commercial market. However, there are still technical obstacles to achieve widespread application of millimeter-wave (mm-wave) CMOS application, especially in the design of Power Amplifier (PA). For example, the gain of CMOS transistor at 60 GHz is typically small, so multiple-stage design is usually employed in order to obtain higher gain. In addition, power combining technology can be a solution to CMOS's low output power. However, the efficiency of CMOS PA is usually low due to the poor RF performance of transistor. Technique like multi-stage design would further reduce the overall efficiency. In [1], Zero Voltage Switching (ZVS) PA has been implemented at 60 GHz and demonstrated 20% efficiency. However, the power gain is only 5 dB and the peak output power is just -1.5 dBm. Alternatively, Injection Locking PA (ILPA) can also achieve high efficiency at 60 GHz [2], [3] in addition to provide high gain with a compact size (see Table I).

However, there are some major drawbacks of the ILPA. First of all, the ILPA is usually more suitable for narrow band application because of its intrinsic narrow injection locking bandwidth. Mm-wave communication standard like IEEE802.15.3c has a wide channel bandwidth of more than 2.16 GHz for each

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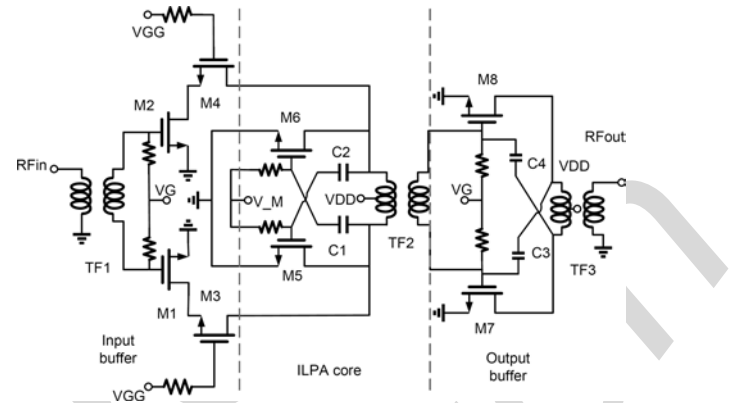


Fig. 1. Schematic of proposed ILPA.

TABLE I
DESIGN PARAMETERS OF THE PROPOSED ILPA

M1/M2*	M3/M4*	M5/M6*	M7/M8*	C1/C2
50 μm /65nm	50 μm /65nm	30 μm /65nm	90 μm /65nm	270fF
C3/C4	TF1	TF2	TF3	
12fF	Radius/Width	23 μm /5 μm	20 μm /6 μm	26 μm /6 μm

* All transistors have finger width of 2 μm

channel and the overall bandwidth is 9 GHz. In addition, direct transformer coupled output is employed in previous two works[2], [3] and this results in potential injection locking frequency shift when the ILPA is loaded with a real antenna that has a non-50 Ω input impedance. Moreover, in a multi-user environment, the interference can be regarded as another type of injection source [5] for the ILPA. Assume that the interference is much larger than the ILPA's input, the ILPA may lock to the interference instead of its input signal. Furthermore, the injection locking time is inversely proportional to the injection locking bandwidth, smaller injection bandwidth requires a longer time. The long injection locking time will cause large phase error that limits the Error Vector Magnitude (EVM) as the phase error between input and output is determined by the transient response of injection locking. Hence, a large injection locking bandwidth is preferred for the ILPA [4].

Conventional ILPA as shown in Fig. 2(a) normally generates a large output power from tank which has a large ratio of output power and input power therefore limits the injection locking bandwidth. This work presents a V-band CMOS ILPA that employs input and output buffer stages to enlarge its injection locking bandwidth as shown in Fig. 2(b).

II. DESIGN & ANALYSIS

The schematic of proposed wide-band ILPA is shown in Fig. 1. The ILPA consists of a cascode input buffer stage, a

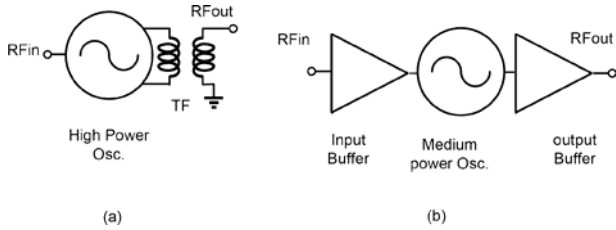


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cross-coupled differential pair with transformer load as ILPA core, and a capacitor neutralized common source stage as output buffer. The transistor size of the cross-coupled pair is $30 \mu\text{m}$, while the size of input driver and output buffer are $50 \mu\text{m}$ and $90 \mu\text{m}$ respectively. The bias voltage V_M is set to zero when the gain of input and output buffer are measured. The injection locking can be understood as synchronization process between the oscillator's high output power and its input injection signal. The synchronization is dependent on the oscillator's design parameters and the frequency difference between injected signal and oscillator's free-running frequency. In the proposed ILPA, the direct transformer coupled output has been avoided to improve the robustness to output pulling. Moreover, the output power from the tank has been reduced so a wide injection locking bandwidth can be achieved. Due to its smaller cross-coupled pair and gain of the input buffer, the input power to tank should be considered as large signal. Hence the analysis must take the large signal into consideration, as the conventional small signal analysis is invalid. Using the extended Adler's equation [6] the locking bandwidth of the proposed ILPA is

$$B = \frac{\omega_o}{2Q} \frac{1}{\sqrt{\left(\frac{P_{out}}{G1G2P_{in}}\right)^2 - 1}} \quad (1)$$

where B is the half injection-locking bandwidth, ω_o is the free-running frequency of oscillator, Q is the quality factor of tank, P_{out} is the output power, P_{in} is the input power, $G1$ is gain of input stage, and $G2$ is the gain of output buffer. As seen in (1), an increase of $G1 \cdot G2$ leads to improvement of injection locking bandwidth. The time domain response can be illustrated by the Adler's equation in differential form

$$\frac{d\phi}{dt} = -\frac{\omega_o}{2Q} \frac{P_{in}G1(P_{in}G1G2 + P_{out} \cos \phi_{ss})}{(P_{out} + P_{in}G1G2 \cos \phi_{ss})^2} \quad (2)$$

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where ω_{inj} is the injection frequency and the minimum settling time occurs when $\omega_{inj} - \omega_o$ equals to zero

$$\tau_{\min} = \left(\frac{\omega_o}{2Q} \frac{P_{in}G1G2}{P_{in}G1G2 + P_{out}}\right)^{-1} \approx \frac{1}{B}. \quad (5)$$

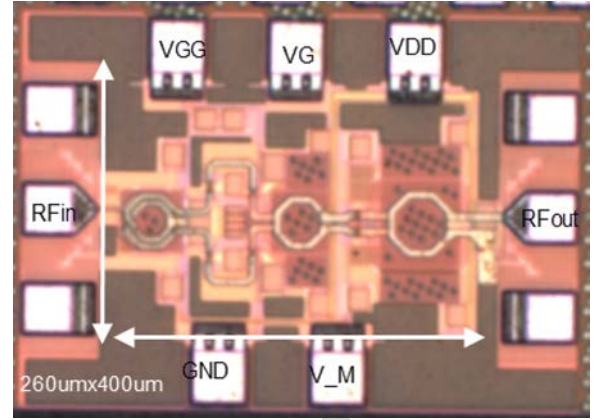


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From (5), the time constant is inversely proportional to the half injection locking bandwidth. Assuming $P_{out} = 100 \cdot P_{in}$, $G1 \cdot G2$ is 20 and a Q of 5, from (1), B will then be about 3.84 GHz for ω_o of 60 GHz. Therefore, the bandwidth of the ILPA would be 7.69 GHz, which has been improved significantly. Conventional ILPA has injection locking bandwidth around 2 GHz [3]. The linearity is also dependent on modulation schemes, a simulation has predicted that $\pi/4$ DQPSK resulted slightly better ACPR performance than QPSK.

In summary, to avoid aforementioned design challenges of conventional ILPA, the ILPA core is used as high voltage gain cell as shown in Fig. 1 to generate a moderate output power. The oscillator's tank consists of a transformer loaded with gates of next stage, which leads to a low tank Q thus improves the injection locking range as shown in (1). Due to the moderate output power from tank, a relatively smaller cross-coupled pair can be used to provide positive feedback. The input injection signal is firstly amplified by the input buffer before injected into the tank. Also it can provide reverse isolation from tank to the input.

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A prototype of the proposed wide-band PA has been implemented in GlobalFoundries 65 nm CMOS technology, the core circuit occupies a $260 \mu\text{m} \times 400 \mu\text{m}$ area excluding pads as shown in Fig. 3. Slot dummy cells metal are used to fulfill the required density rule except for transformer region where dummy filling excluded mask was employed. The proposed PA has been measured on wafer using Cascade Elite300 On-Wafer Probe Station with Agilent 8361A vector network analyzer calibrated using LRRM (load, reflect, reflect, match) using standard substrate at room temperature 27°C .

To characterize the $G1 \cdot G2$, the V_M bias voltage is set to zero, so the cross-coupled pair presents a high impedance. Under 1.2 V supply, 0.75 V gate bias with 53.6mW power consumption, a peak small-signal gain of 13 dB is achieved at 56 GHz, compared to peak gain of 13.5 dB at 58 GHz from post-layout simulation. The discrepancy is mainly due to the unaccounted parasitic at mm-wave.

The output power and PAE versus frequency has been investigated in Fig. 4. The peak output power of 10.5 dBm is shown at the free-running frequency of 55 GHz, while the simulation predicts a free-running frequency at 58 GHz with output power

TABLE II
MM-WAVE CMOS HIGH EFFICIENCY PA

Technology	Topology	Freq(GHz)	Max Gain (dB)	Pmax(dBm)	PAE(%)	Area(mm ²)
CMOS 65nm -This work	Buffered Input&Output	50-59	37.8	11.39	16.1	0.104
CMOS 65nm [3]	2 to 1 transformer	52.5-54.5	29	9.6	17.3	0.1
CMOS 65nm [1]	ZVS	57-65	5	-1.5	20*	NA

*Drain efficiency

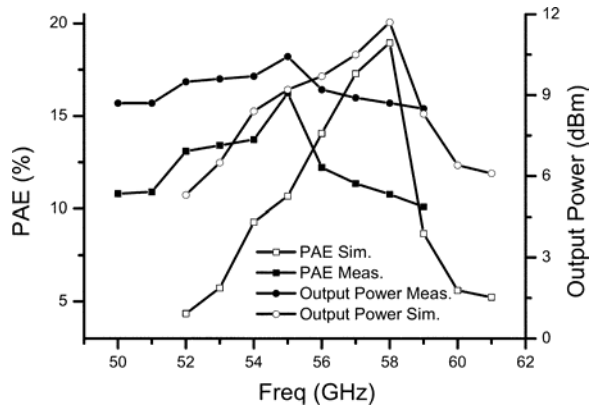


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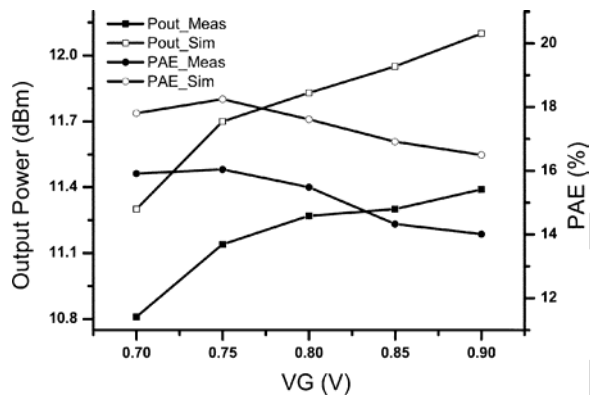


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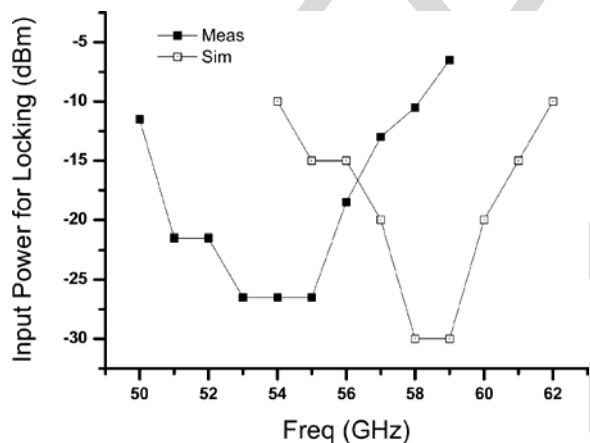


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of 11.7 dBm. The measurement has shown that from 54 GHz to 56 GHz the ILPA can delivery an output power and efficiency of more than 9 dBm and 10% respectively. The output

power and PAE versus gate bias is shown in Fig. 5. A maximum output power of 11.39 dBm has been obtained while the simulated output power is more than 12 dBm at 55 GHz. The output power increase slightly as the gate bias of common source stage increases. However, the best efficiency is achieved with gate bias of 0.75 V, because a low gate bias limits the linearity of common source buffer but a high gate bias increases the power consumption. The bias of crossed-coupled pair is set to 0.8 V to achieve large swing. A gate bias of larger than 0.9 V would cause the cross-coupled pair to enter triode region which leads to a reduction in output power.

The injection-locked operations is characterized when V_M control is set to 0.8 V. The free-running frequency of ILPA is at 55 GHz. The measured injection locking range is from 50 to 59 GHz as shown in Fig. 6. The maximum required injection power at 50 GHz is -11.5 dBm, while at 59 GHz is -6.5 dBm. At the free-running frequency, the minimum required input power is -26.5 dBm while the output is 11.39 dBm, which corresponds to a gain of 37.8 dB. The wide injection locking range is also due to the well designed input matching network and signal amplification from the first stage. Table II compares high efficiency mm-wave CMOS PA designs. The proposed ILPA has achieved the largest injection locking range, the achieved PAE is comparable to other works.

IV. CONCLUSION

This work demonstrates an ILPA with largest injection locking bandwidth, the fabricated PA has achieved a injection locking range from 50 to 59 GHz, and a maximum output power of 11.39 dBm has been obtained while the highest PAE is 16.1%. Moreover, the chip size is $260 \mu\text{m} \times 400 \mu\text{m}$ excluding pads. In summary, a compact size and high efficiency wide-band ILPA has been proposed.

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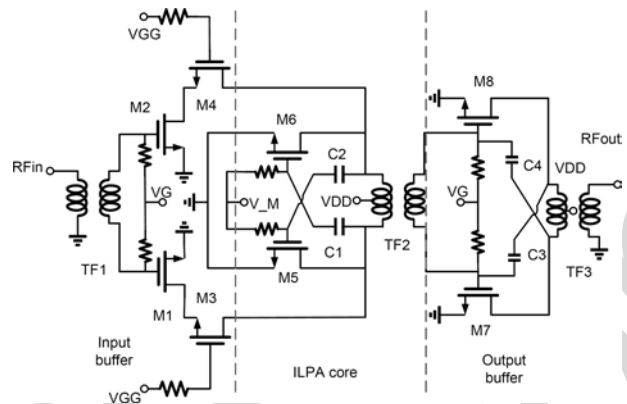


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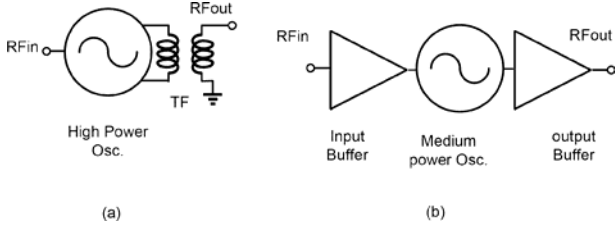


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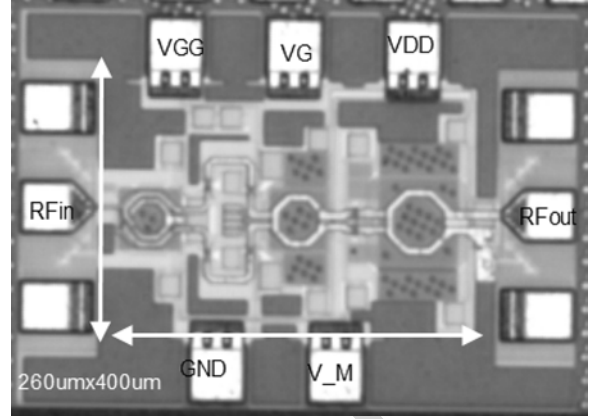


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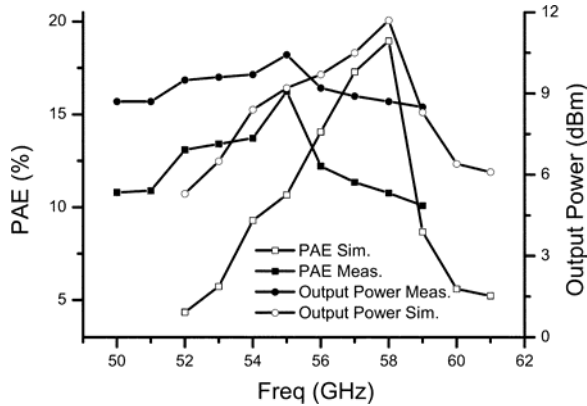


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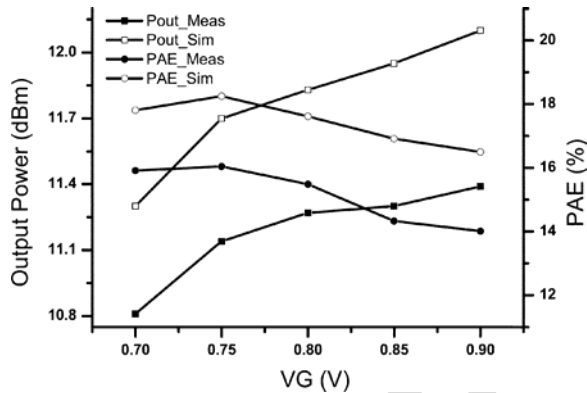


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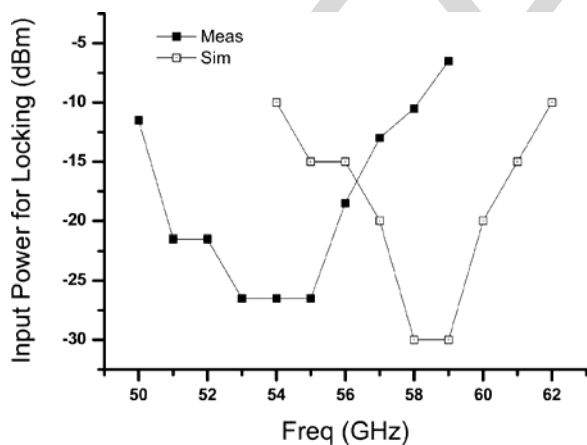


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