A 5.9 GHz Fully Integrated GaN Frontend Design With Physics-Based RF Compact Model

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***Abstract*—This work presents the design of a fully integrated high-efficiency and high-power RF frontend for the IEEE 802.11p standard in GaN HEMT technology. An embedded transmitter/receiver (Tx/Rx) switching scheme and a dual-bias power amplifier (PA) linearization technique are used to improve Tx efficiency and linearity. An accurate physics-based non-linear, large signal device model is developed and used for the design, providing insight into the impact of the behavioral nuances of the GaN HEMTs on RF circuit performance. The fully integrated RF frontend is fabricated in 0.25 µm GaN-on-SiC technology and occupies only 2 mm x 1.2 mm. The Tx branch achieves 48.5% drain efficiency at 33.9 dBm, Psat with 28 V supply. With orthogonal frequency division multiplexing (OFDM)-modulated signals, it achieves 30% average efficiency at 27.8 dBm output power while meeting the -25 dB error vector magnitude (EVM) limit without predistortion. The Rx branch achieves +22 dBm OIP3 with 3.7 dB noise figure at 12 V supply. The fully integrated high-efficiency and linear RF frontend designed with physics-based RF GaN compact models is demonstrated for the first time for future device-to-device applications.**

***Index Terms*—RF frontend, GaN HEMT, compact model, power amplifier, drain efficiency, antenna switch, low noise amplifier, IEEE 802.11p, and device-to-device communication**

I. Introduction

THE proliferation of mobile devices and moving objects (e.g. cars) that demand increasing wireless data communications is causing the capacity limit to be exceeded in cellular networks and low responsiveness between devices/objects and users. Besides, mobile devices tend to be working on in-situ computations by themselves for video/file sharing, multi-player games, or processing sensor data from nearby devices, and thus can leverage direct device-to-device (D2D) communications to off-load the base stations in cellular networks and improve response time. The emerging IEEE 802.11p-based dedicated short range communication (DSRC) standard [1] was originally targeted for car safety and congestion control, but it is actually a form of D2D communication with long range and fast response time. Since current D2D (e.g. WiFi Direct) cannot effectively handle the demands of D2D due to insufficient range and poor reliability, IEEE 802.11p can be harnessed as a viable D2D solution [2].

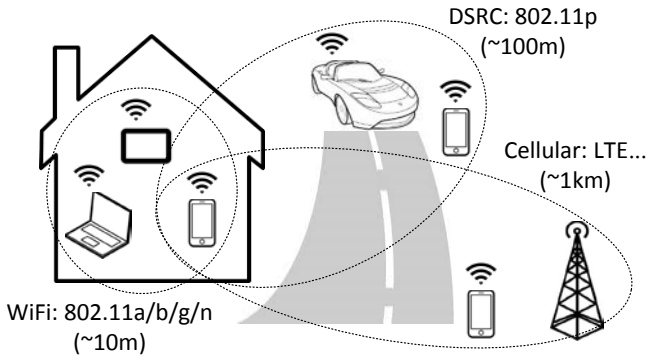

Fig. 1. Comparison between DSRC, WiFi, and Cellular networks.

Fig. 1 illustrates the co-existence of WiFi, DSRC, and Cellular networks with different coverage and the comparison between WiFi and DSRC is shown in Table. 1. To be suitable for highly mobile networks that change topologies very rapidly in multipath channel environments, the maximum allowed output power in the IEEE 802.11p standard is 28.8 dBm in the 5.9 GHz frequency band with the same orthogonal frequency division multiplexing (OFDM)-based modulation as in the IEEE 802.11a standard. However, CMOS circuits have not been able to achieve such high output power at 5 GHz while maintaining linearity or good error vector magnitude (EVM) even though much effort was put into increasing the efficiency and output power of a CMOS linear PA for 5 GHz wireless local area network (WLAN) applications [3], [4].

It is well known that GaN devices outperform CMOS devices for PAs in terms of output power and efficiency. In this paper, we leverage GaN for a high-power and high-efficiency

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TABLE I
COMPARISON BETWEEN 802.11A AND 802.11P

	802.11a (WiFi)	802.11p (DSRC)
Frequency (GHz)	5.15 – 5.825	5.85 – 5.925
Channel BW (MHz)	20	10
Max. output (dBm)	16 / 23	28.8
Data rate (Mbps)	6 – 54	3 – 27
Modulation	BPSK – 64QAM	BPSK – 64QAM
Symbol duration (μs)	4	8
Guard time (μs)	0.8	1.6
Preamble duration (μs)	16	32
Subcarrier space (kHz)	312	156

PA design for the IEEE 802.11p standard through an accurate RF compact model for GaN HEMTs. At the same time, a linear GaN-based low noise amplifier (LNA) can be employed in RF frontends since the receiver is also required to be highly linear to accommodate input signals with minimum sensitivity along with potential high-power interferers from nearby 802.11p transmitters. Due to the high power handling capability, small on-resistance, and high isolation characteristics of the GaN devices, on-chip antenna switches can also be taken into account to achieve high level of integration. Implementing GaN RF frontends including a PA, an LNA, and transmitter/receiver (Tx/Rx) antenna switches on a single die enables the reduction of packaging cost and system form factor since high-power RF frontends have traditionally relied on multi-chip modules or discrete designs. The fully integrated RF frontend can benefit from both architectural and circuit-level techniques to further improve efficiency. A new Tx/Rx switching scheme and a dual-bias linearization technique are proposed to design the RF frontend using GaN RF compact model, enhancing system energy efficiency.

This paper is an expanded version from the IEEE RFIC Symposium in 2014, providing more details on the circuit design and measurement as well as adding two more issues: a physics-based RF compact model used for the circuit design and discussion on a negative bias generation circuit for depletion mode GaN HEMT devices. Section II discusses frontend architectures and proposes a new transmitter/receiver (Tx/Rx) switching scheme for achieving high-efficiency Tx. Section III gives a detailed description of the RF frontend circuit designed with a physics-based GaN RF compact model described in Section VI. Implementation results for a prototype are presented in Section IV. The circuit performance is benchmarked against simulation with the calibrated model in Section V. Section VI describes the GaN RF compact model which is calibrated against measurements on fabricated test devices. Finally, to make a fully integrated 802.11p radio and to overcome the disadvantage of depletion mode GaN HEMTs, future direction for higher level of integration is discussed in Section VII, followed by a conclusion in Section VIII.

II. RF FRONTEND ARCHITECTURE

In a time division duplex (TDD) radio, an explicit antenna switch is usually employed in both the Tx and Rx branches in order to switch modes. This architecture is shown in Fig. 2(a). An integrated GaN switch typically exhibits an insertion loss of about 1 dB at 5.9 GHz [5], in addition to consuming significant

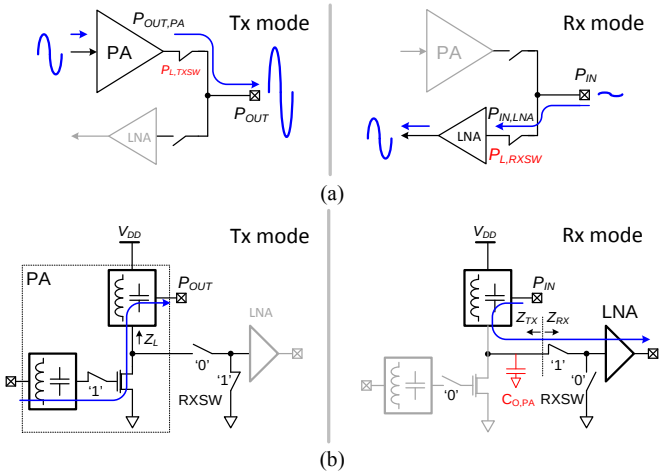


Fig. 2. RF frontend architecture. (a) Conventional Tx/Rx switching scheme. (b) Proposed Tx/Rx switching scheme.

additional die area. Switch insertion loss adversely impacts both Tx and Rx performance. In the Rx branch, it directly adds to the overall noise figure (NF) of the receiver chain. In the Tx branch, the switch is placed at the output of the PA. If the PA produces an output power of $P_{OUT,PA}$, and the Tx switch has a loss of $P_{L,TXSW}$, then the achievable Tx output power at the antenna port is:

$$P_{OUT} = P_{OUT,PA} - P_{L,TXSW} \quad (1)$$

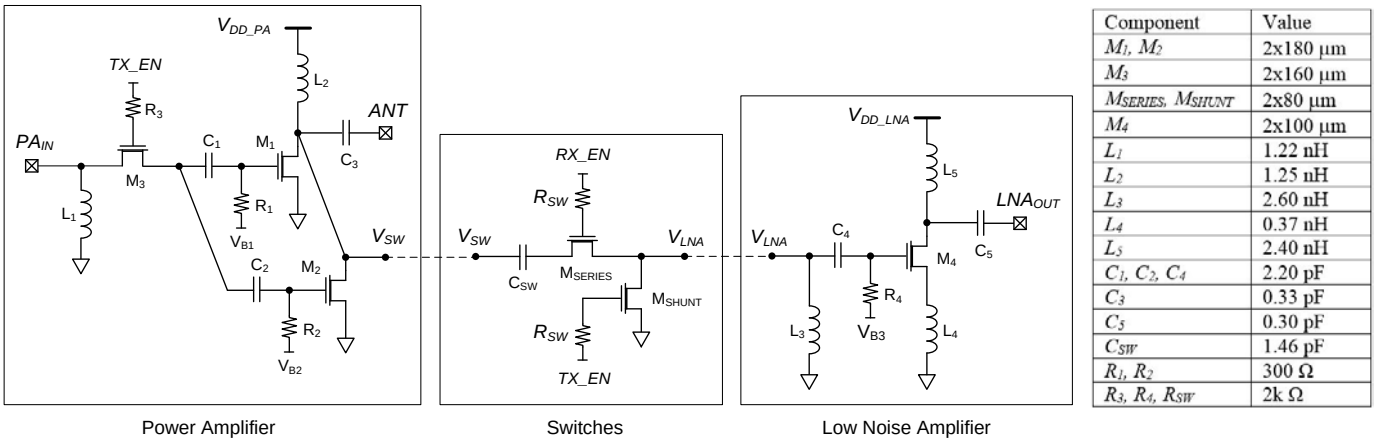
Similarly, if the PA efficiency is given by η_{PA}, then the overall Tx efficiency is:

$$\eta = \eta_{PA} \times 10^{-(P_{L,TXSW}/10)} \quad (2)$$

If a 1 W, 50% efficient PA is used with an antenna switch exhibiting 1 dB of loss, the overall TX output power and efficiency are degraded to 0.794 W and 39.7%, respectively, according to (1) and (2). To return to the desired power level of 1 W, the PA output power must be boosted to compensate, leading to more than 25% increase in overall TX power consumption because consumed dc power is not fully transformed to RF output power. Consequently, additional energy consumption is dramatically increased in a transmitter chain to compensate for the loss of the switch.

Fig. 2(b) shows the proposed architecture [6], which focuses on co-design of the Tx and Rx paths to essentially eliminate the Tx branch switch for efficiency enhancement. No explicit switch is placed at the output of the PA. The switch at the PA input prevents an undesirable Tx input signal from leaking into the receiver or the antenna port and its small on-resistance can be absorbed as a series gate resistor for PA stabilization, providing both isolation (when it is off) and stability (when it is on).

To maximize the energy efficiency of the system, the Tx is designed and optimized first. The PA output-matching network transforms the 50 Ω antenna to an optimum impedance Z_L, which maximizes the output power from the GaN HEMT



Component	Value
M_1, M_2	2x180 μm
M_3	2x160 μm
M_{SERIES}, M_{SHUNT}	2x80 μm
M_4	2x100 μm
L_1	1.22 nH
L_2	1.25 nH
L_3	2.60 nH
L_4	0.37 nH
L_5	2.40 nH
C_1, C_2, C_4	2.20 pF
C_3	0.33 pF
C_5	0.30 pF
C_{SW}	1.46 pF
R_1, R_2	300 Ω
R_3, R_4, R_{SW}	2k Ω

Fig. 3. RF frontend circuit schematic and component values.

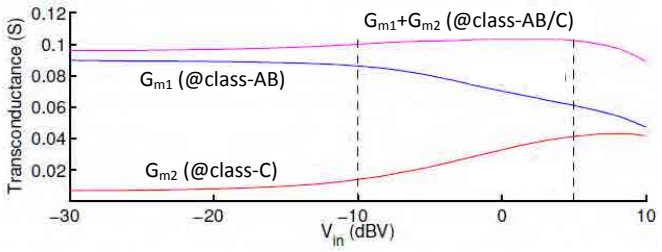


Fig. 4. Simulated dual-bias linearization of large-signal transconductance.

device. Under this condition, the drain of the PA device sees large voltage swings up to $2V_{DD}$. The series-shunt switch in the Rx branch isolates and protects the inactive LNA from this voltage stress. In the Rx mode, the PA transistor is isolated from the PA input by employing the PA input switch which is off. The PA transistor is also turned off with a sufficiently low gate bias and presents a small but finite parasitic capacitance $C_{O,PA}$ at the drain node. The LNA input is simply power-matched to the parallel combination of Z_L and $C_{O,PA}$ to maximize power gain and minimize noise figure, as defined below.

$$Z_{RX}(\omega) = Z_{TX}(\omega)^* = (Z_L(\omega) || \frac{1}{\omega C_{O,PA}})^* \quad (3)$$

The circuit details will be described in the following section.

III. Circuit Design

Fig. 3 illustrates the entire RF frontend circuit schematic including PA, antenna switch, and LNA, which are all integrated on a single die. All the circuits in this section are designed with a physics-based GaN RF compact model which is calibrated against device-level measurements, described in Section VI.

A. Tx design

Since the IEEE 802.11p standard employs OFDM modulation, a standard-compliant PA should satisfy the linearity requirement to accommodate the high peak-to-average power ratio (PAPR) of complex modulated signals, as well as high efficiency. Considering additional constraints of high level of integration and minimizing the die area, conventional PA techniques like a Doherty PA [7] or a switching PA with supply modulation [8] are not appropriate candidates due to the large size of the required passive components and circuit complexity. In this work, a Class-C GaN HEMT device with its input and output combined in phase with a Class-AB GaN HEMT device [9] is adopted for higher linearity with enhanced efficiency, without additional tail devices for more compact integration of the RF frontend.

Fig. 4 shows the simulated individual transconductances, G_{m1}/G_{m2} for Class-AB/C over a range of drive voltages, as well as the linearized composite transconductance, $G_{m1}+G_{m2}$. Since Class-AB amplifiers have to be backed-off from their P_{1dB} point to meet system linearity and EVM requirements, a low P_{1dB} point corresponds to lower average efficiency. However, with help of the combined in-phase Class-C device, the P_{1dB} point of the PA increases through cancellation of the compressive nonlinearity, enhancing the average efficiency.

The optimal impedance vectors were found through large-signal load-pull simulation for the dual-biased GaN HEMT devices, with up to the third harmonics. Initially, the source impedance is set to Z_0 to determine Z_L with load-pull, and then a source-pull is performed to find Z_S. Since efficiency is more sensitive to load impedance, the optimal Z_L is used, while a somewhat non-optimal Z_S is chosen in order to improve stability. Small on-resistance of the PA input switch in the Tx mode acts as a series stabilization resistance, absorbing the switch loss. The final load and source impedances at 5.9 GHz used in the design are presented in (4) and (5). Based on those impedance vectors, the input and output *LC* matching networks are designed.

$$Z_L = Z_0(0.57 + j1.33) \quad (4)$$
$$Z_S = Z_0(0.66 + j0.36) \quad (5)$$

The corresponding passive component values adjusted after rigorous post-layout electromagnetic (EM) simulations, are also listed in Fig. 3. At the drain, the shunt-L/series-C provides impedance matching from Z_0 to Z_L, dc biasing, and RF signal

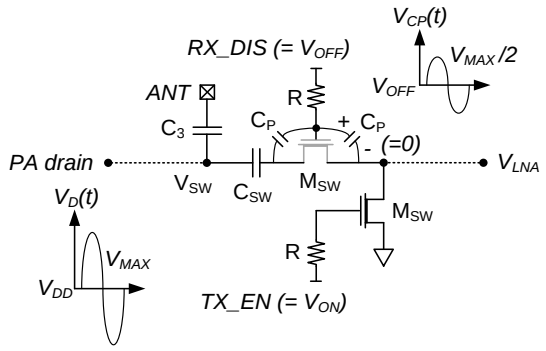


Fig. 5. Rx switch design considering the Tx mode waveform.

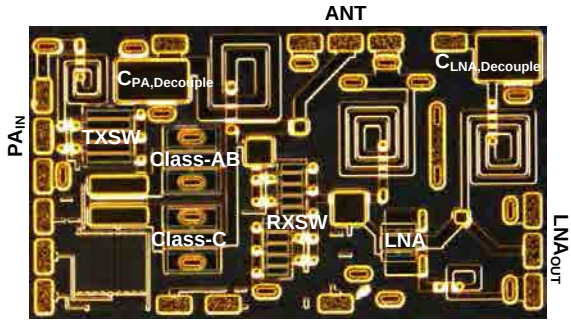


Fig. 6. Die micrograph of the fully integrated RF frontend.

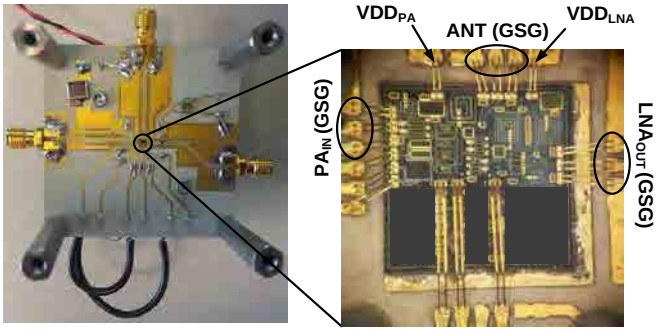


Fig. 7. PCB and Chip-On-Board (COB) Implementation

coupling, with only two elements. A series-C/shunt-L is chosen for the gate as it performs the transformation from Z_0 to Z_S and splits the RF signal into the two gates in phase for the dual-bias Class-AB + Class-C topology.

The small signal and large signal simulation results with the GaN RF compact model will be shown and compared with measurement data in Section V.

B. Rx design

In Fig. 3, the series-shunt switches are placed in the Rx path, which protect the LNA from the high-power PA in the Tx mode while providing low insertion loss in the Rx mode. In the Tx mode, the LNA input, V_{LNA}, is grounded through the shunt switch, as shown in Fig. 5. Since the series switch is directly connected to the drain of the PA, the voltage stress is shared equally in the capacitive divider formed by the parasitic capacitors C_P of the series switch which is off. The control voltage, V_{OFF}, should be chosen such that the RF voltage stress does not accidentally turn on the series switch, satisfying the condition in (6).

$$V_{CP,max} = V_{OFF} + \frac{V_{max}}{2} \ll V_{TH} \tag{6}$$

Considering the maximum expected V_{DD} used, V_{OFF} = -25 V is chosen with margin because the depletion mode GaN device has a negative threshold voltage and the supply voltage is supposed to be up to 37 V in measurement. The switches are sized to keep loss under 0.5 dB and provide more than 30 dB of isolation which is adequate to protect the LNA.

The LNA's input matching network is co-optimized with a small resistance, R_{ON}, in the series switch, which forms the conjugate power match with Z_{TX} as follows.

$$Z_{RX}(\omega) = Re\big(Z_{LNA}(\omega)\big) + R_{ON} + Im(Z_{LNA}(\omega)) = Z_{TX}(\omega)^* \tag{7}$$

An inductively degenerated topology is for independent control of real and imaginary parts of the input impedance as well as obtaining good NF. Fig. 3 shows the complete LNA schematic with the corresponding component values. 12 V supply is used for the LNA whereas the high-power PA is designed with more than 28 V.

The Rx simulation results including small/large signal and 3rd order intermodulation performance with the GaN RF compact model will also be shown and compared with measurement data in Section V.

IV. Implementation

Three test devices (i.e. 2 x 180 μm, 2 x 100 μm, and 2 x 30 μm) with open and short de-embedding patterns were fabricated in Cree 0.25 μm GaN-on-SiC technology to generate the RF compact models. A prototype of the proposed fully integrated RF frontend was also fabricated. The die micrograph is shown in Fig. 6. The RF frontend circuit occupies 2.0 mm x 1.2 mm die area including all passive matching components and decoupling capacitors at the supply nodes for both the PA and LNA. Spiral inductors designed with a thick metal layer and high-voltage metal-insulator-metal capacitors were used for all matching networks. The process also offers through-wafer-vias which were used extensively for low-inductance and stable grounding. Co-simulation with foundry supplied device models and EM simulation-based models (mostly for passives and interconnect metals) was conducted for final verification of the design and layout. Benchmarking the circuit simulation performances with the MIT Virtual Source GaNFET-RF (MVS-G-RF) model against measurement results will be demonstrated in the next section.

For good thermal and electrical performance, eutectic die attachment is performed directly to the printed circuit board (PCB) through chip-on-board (COB) technology. Fig. 7 shows the prototype board implementation with only a few decoupling capacitors on the PCB. To minimize the inductance value,

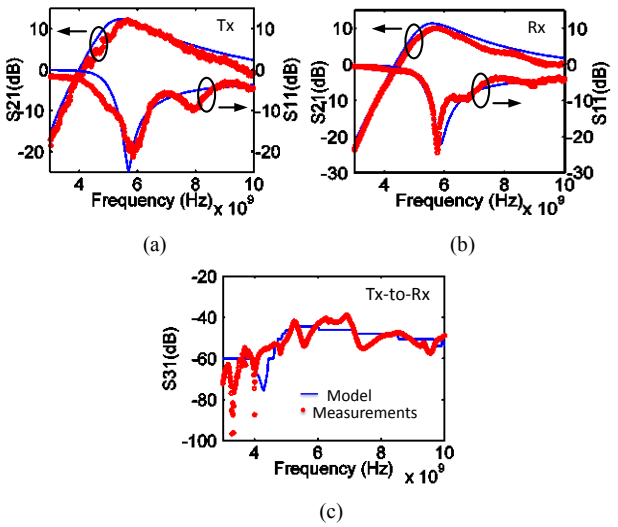


Fig. 8. Small signal frequency response of the RF frontend (the model is benchmarked against measurements in circuit level). (a) Tx mode. (b) Rx mode. (c) Isolation between Tx and Rx.

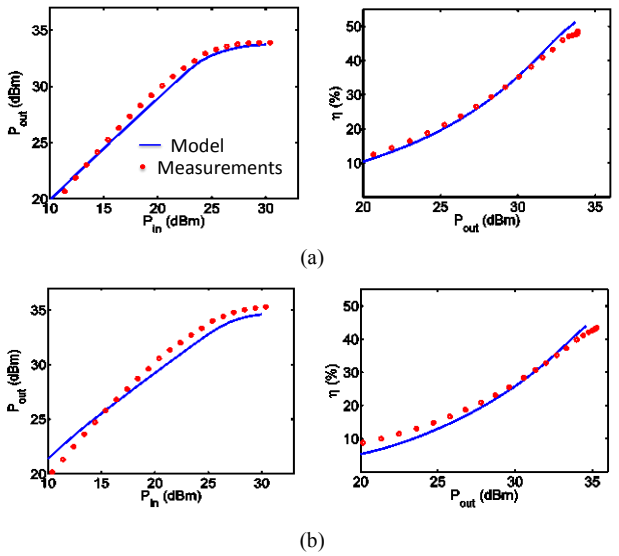


Fig. 10. Tx linearity and efficiency measurements are compared against simulation with the compact model, at (a) V_{DD} = 28 V and (b) V_{DD} = 37 V.

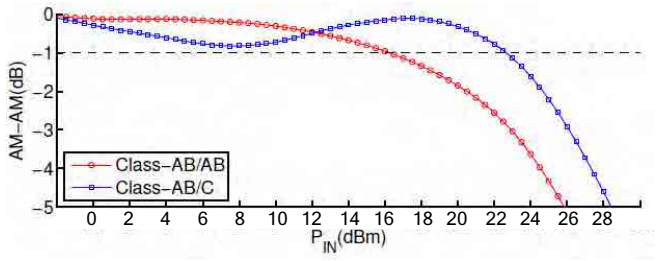


Fig. 9. Measured dual-bias linearization.

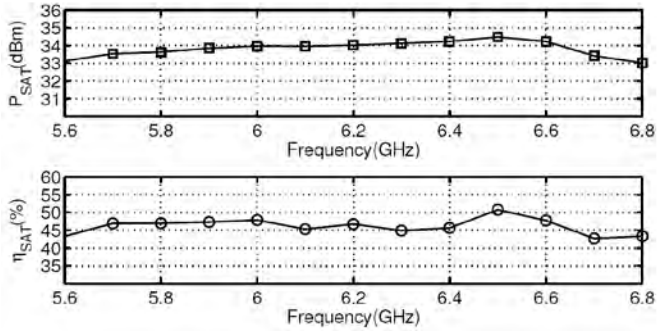


Fig. 11. TX saturated power and efficiency measurements over frequency.

double bond wires are used for all pads. In particular, bond wire length of important RF and supply pads is designed to be less than 0.4 nH. Double bonding along with the on-chip decoupling capacitors at the supply nodes is helpful to minimize the wire bonding effects at 5.9 GHz. The PCB is designed on a high dielectric constant, low-loss Rogers-3010 material.

V. Measurement Results

The small signal responses of the RF frontend are measured and compared with the simulation results. Fig. 8 (a) shows the small signal response in the Tx mode, with the Rx port terminated. S11 is better than -20 dB while S21 is around 10 dB for the band of interest (i.e. 5.850 GHz - 5.925 GHz). The small-signal response of the Rx mode is also shown in Fig. 8 (b). The input matching of the LNA combined together with the Rx series-shunt switches are measured at the antenna port, which shows S11 of -13 dB and S21 of 8 dB at 5.9GHz. Tx-Rx path isolation, shown in Fig. 8 (c), is better than -45 dB in the band of interest. All small signal measurements in Fig. 8 are well matched with the simulation results using the RF compact model extracted from the discrete devices for modeling.

The measured amplitude-to-amplitude (AM-AM) response for two bias configurations consuming the same total quiescent current of 9 mA demonstrates the advantage of the dual bias linearization, as depicted in Fig. 9. For the Class-AB/C case, one transistor carries most of 9 mA while the other transistor is biased below threshold, yielding a more linearized response with P1dB improving dramatically by over 6 dB, thereby validating the linearization scheme introduced in Section III.

Fig. 10 shows TX power sweeps with the optimized Class-AB/C bias. The efficiency of 48.5% is achieved at 33.9 dBm P_{SAT} with 28 V supply voltage in Fig. 10 (a), while the 43.8% efficiency at 35.3 dBm P_{SAT} with 37 V supply voltage is shown in Fig. 10 (b). Good agreement between the measurement and simulation data with the RF compact model in both cases proves that the RF compact model is quite scalable with a wide range of drain voltages (there is also a good agreement in the LNA with 12 V supply, which is validated below). 37 V supply voltage provides a bit higher saturation output with lower efficiency due to the increased dc power consumption. Measured P_{SAT} and efficiency at P_{SAT} is almost maintained across 1 GHz bandwidth with 28 V supply, as shown in Fig. 11.

To evaluate performance with real communication signals, the Tx is tested with 20 MHz bandwidth 802.11a waveforms with 7 dB PAPR instead of 802.11p signals with 10 MHz

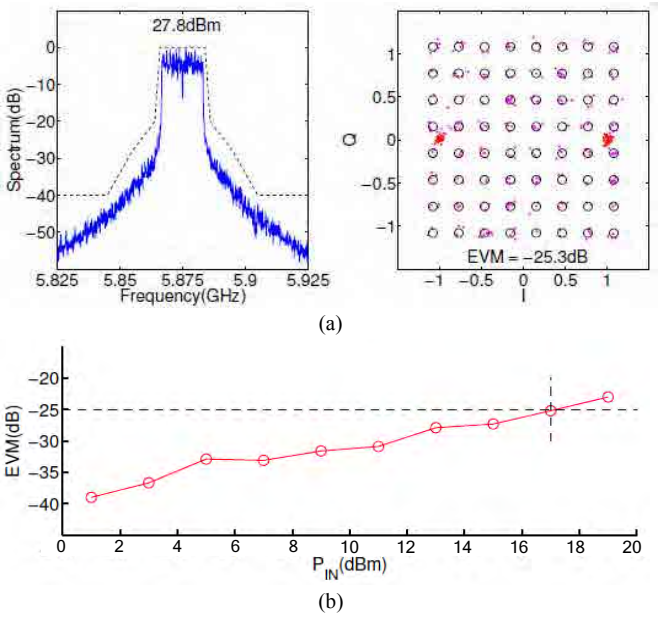


Fig. 12. Measured Tx performance with 20MHz bandwidth OFDM signal. (a) Output spectrum at 5.875 GHz and EVM. (b) EVM across the input power level.

TABLE II
COMPARISON OF FULLY INTEGRATED RF PA

	[3]	[4]	[10]	**This work**
Application	802.11a	802.11a	Generic	**802.11p**
Technology	45 nm CMOS	65 nm CMOS	0.2 µm GaN	**0.25 µm GaN**
PA topology	Class-AB	Class-AB	Switch	**Class-AB/C**
Freq. (GHz)	4.9 – 5.9	4.9 – 5.9	7	**5.7 – 6.7**
V_{DD} (V)	-	6.35	28	**28**
P_{SAT} (dBm)	26.0	30.3	37.0	**33.9**
η_{SAT} (%)	32.1	19.4	-	**48.5**
P_{OUT} (dBm)	18.7	-	33.2	**27.8**
η (%)	-	-	19.1	**30.0**
EVM (dB)	-25.0	-	-28.0	**-25.3**
Integrated switch	No	No	No	**Yes**
Pre-distortion	Yes	No	Yes	**No**

bandwidth to compare with other fully integrated PAs [3], [4], [10] in a high frequency band. As shown in TABLE I, 802.11p adopts the same OFDM modulation as 802.11a except that its time domain parameters are double those of 802.11a and it occupies half the bandwidth of 802.11a accordingly. In fact, the transmitted spectrum for 802.11a (802.11p with the Class A or B transmit power classifications) shall have a 0 dBr bandwidth not exceeding 18 MHz (9 MHz), –20 dBr at 11 MHz (5.5 MHz) frequency offset, –28 dBr at 20 MHz (10 MHz) frequency offset and –40 dBr at 30 MHz (15 MHz) frequency offset and above, respectively. Thus, we can assume that the 802.11a and 802.11p signals are similar enough. Although more stringent spectrum mask is applied to higher transmit power classifications of 802.11p (i.e. Class C and D) [1], the 802.11a

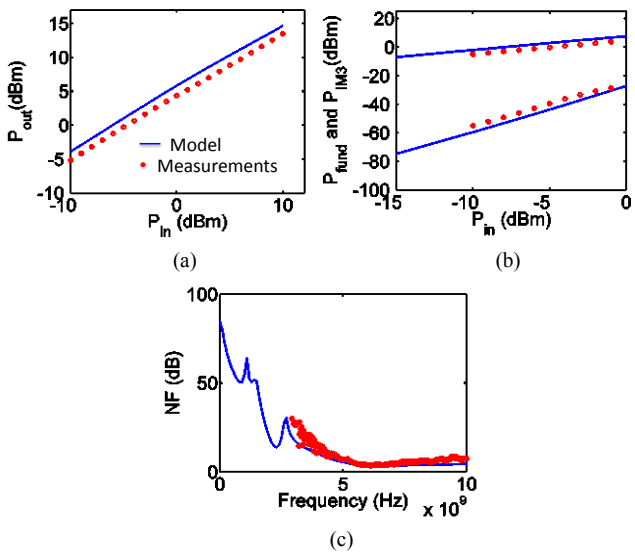


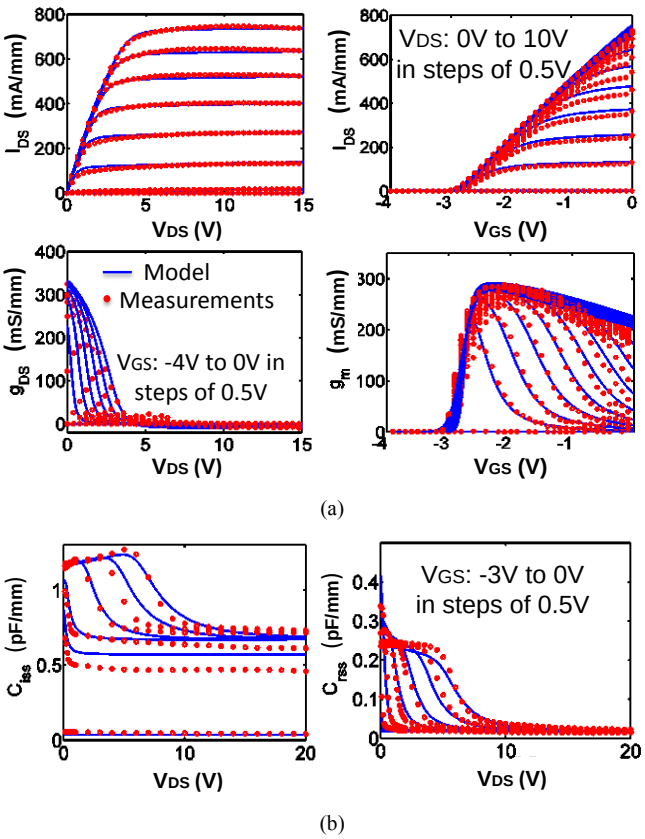
Fig. 13. LNA performance comparison between the model and measurements. (a) P_{out} vs. P_{in}. (b) Third-order intermodulation with two-tone input. (c) Noise figure.

spectrum mask for the 20MHz bandwidth signal is appropriate for a fair comparison with the other PAs in TABLE II. As shown in Fig. 12 (a), the Tx complies with the general WLAN spectral mask, achieving an average efficiency of 30% at 27.8 dBm output power with -25.3 dB EVM without applying any digital predistortion. Fig. 12 (b) demonstrates the EVM change across the input power levels. Table II summarizes the performance comparison with other fully integrated PAs for WLAN applications in the 5 GHz band. Compared to the other publications, the results of this work include the Tx switch.

The Rx nonlinearity is also tested and compared with the simulation data. The large-signal one-tone and two-tone responses with 5.5 mA currents at 12 V supply are depicted in Fig. 13 (a) and (b), showing that the OP1dB of the Rx is 10.8 dBm and OIP3 lies at 22.0 dBm. As shown in Fig. 13 (c), 3.7 dB NF is also predicted by the simulation with the RF compact model. NF is measured with a calibrated noise source and found to be 3.7 - 4.0 dB in band, which is reasonable considering 2.0 dB NF_{min} of the GaN HEMT device in Section VI, an inductive degeneration LNA topology, and additional input switch loss in the Rx branch. Since the LNA active device is not downsized aggressively to maintain high linearity, it partially affects noise performance, as well.

VI. RF COMPACT MODEL FOR GAN HEMTS

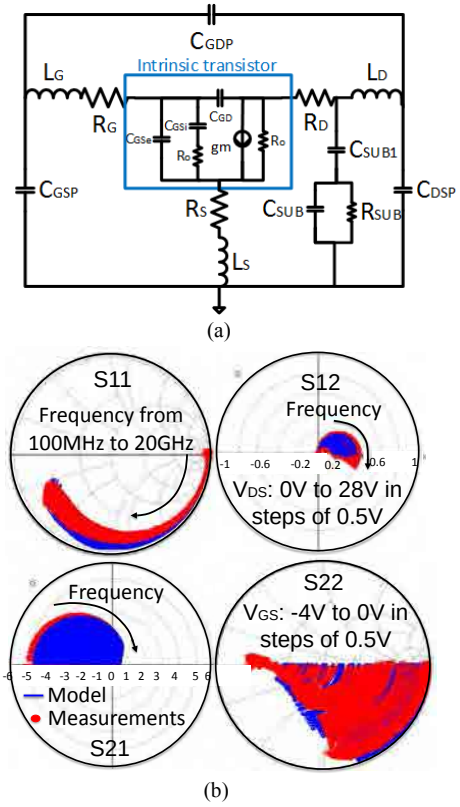
Accurate RF compact models for GaN HEMTs are crucial for designing the IEEE 802.11p RF frontend circuits described in this paper. Compact models for RF circuit design particularly need to consider accurate non-linear device behavior suitable for high-frequency and high-power operation regimes, which is a stricter requirement than for digital-logic design. It is also desirable that these compact models be grounded on appropriate device physics in order to gain insight into the impact of the behavioral nuances of the GaN HEMTs on RF



(a)

(b)

Fig. 14. Dc modeling. (a) Terminal currents and output/trans-conductance. (b) C-V plots of L_g=0.25 µm GaN HEMT comparing MVS-G-RF model against measurements.



(a)

(b)

Fig. 15. Small signal modeling. (a) Small signal equivalent circuit with parasitics added to the core model of the device. (b) The global-S-parameter fits of the model in the region of interest for circuit design are compared against measurements. The 4 S-parameters that are shown on smith charts and polar plots are derived at frequencies from 100 MHz to 20 GHz, V_{DS} ranging from linear-to-saturation and V_{GS} spanning on-to-off state of the device.

circuit performance, which is not the case with most of the available models such as EEHEMT, Curtice, and Angelov models [11].

In this work, the physics-based MIT Virtual Source GaNFET-RF (MVS-G-RF) model was used to characterize devices fabricated in Cree's 0.25 µm GaN-on-SiC process which is the same technology used for the RF frontend circuits design in this paper. The model benchmarked against these devices was used for the RF frontend design and simulation. In this section, the model is extracted and compared against dc *I-V*/*C-V*, small signal response, large signal power-sweep/load-pull, and NF measurements of the fabricated devices, using a small number of parameters with straightforward physical meanings.

The MVS-G-RF model captures static and dynamic device behavior through self-consistent current and charge expressions, as in (8) and (9).

$$\frac{I_D}{W} = Q_{inv,s} \cdot v_{sat} \cdot F_{sat}$$

, where v_{sat} is the saturation carrier velocity,

$$F_{sat} = \frac{V_{DS}/V_{DSAT}}{(1 + (V_{DS}/V_{DSAT})^{\beta})^{1/\beta}}$$

and

$$V_{DSAT} = \frac{v_{sat} \cdot L_g}{\mu} \tag{8}$$

$$Q_{inv,s} = C_g n \phi_t \ln(1 + exp\frac{(V_{GS}) - (V_T - \alpha\phi_t F_f)}{n\phi_t}) \tag{9}$$

Here C_g is the areal gate capacitance, L_g is the effective gate length, μ is the carrier mobility, φ_t is thermal voltage and n is sub-threshold factor. More details about the model can be found in [12] along with a description of implicit-gate transistor model for access regions of the device that play an important role in device linearity at high compression regions under high output power levels in PAs. The model includes the effect of self-heating, gate leakage, device parasitics, and RF device-noise. The details of the physical equations that are used to describe the device behavior are presented in [13].

The terminal dc measurements along with self-consistently solved non-linear terminal capacitances from the benchmarked model validated against device measurements are shown in Fig. 14. Dc output/transfer and output/trans-conductance plots of the 0.25 µm GaN HEMT are demonstrated in Fig. 14 (a), and good agreement has been achieved between the model and measurement. The drop in g_m beyond V_t is caused by the non-linear access region behavior and device self-heating. The charge model gives the input capacitance (Ciss) and reverse

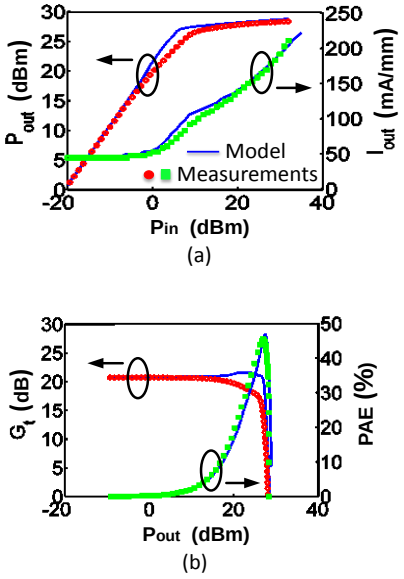


Fig. 16. Load-pull comparison between the model and measurements. (a) P_{out} and I_{out} versus P_{in}, (b) G_t and PAE versus P_{out}, for a 2x180 µm GaN HEMT.

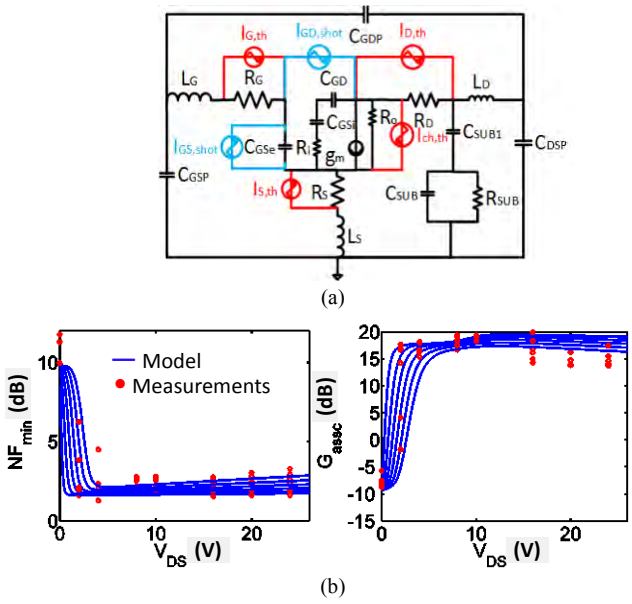


Fig. 17. Noise modeling. (a) Thermal and shot noise sources added to the model. (b) NF_{min}, and G_{ascc} are benchmarked against noise measurements.

transfer capacitance (Crss) fits which compare with the measured *C-V*s obtained from S-parameter measurements, as depicted in Fig. 14 (b). Fringing capacitance extracted from measurements is the only additional parameter needed for the fits.

The S-parameters of the test devices in the desired bias (up to 28 V) and frequency ranges (up to 20 GHz) are measured and the device model parasitic elements are extracted from the S-parameter fits, as shown in Fig. 15. Parasitics associated with contact pads, terminal leads, and substrate losses are added onto the core intrinsic model and the extracted model is compared

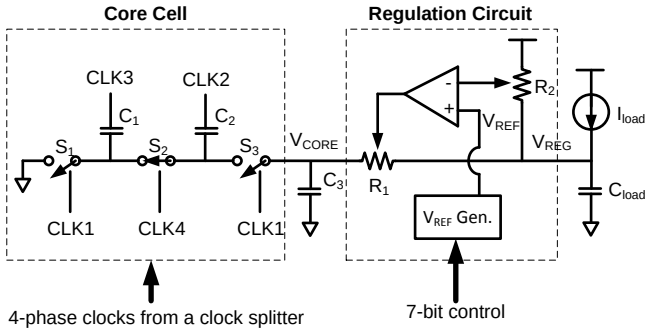


Fig. 18. Functional block diagram of the negative bias generator.

against measured small signal S-parameter fits over the desired bias and frequency ranges required for RF circuit design. The input gate parasitics affect S11 parameter and output drain parasitics including substrate parasitics can be extracted from S22 parameters.

The benchmarked model is able to predict large-signal device behavior in load-pull measurements without employing any additional parameters, thanks to the physical nature of the model. The device biased in class-AB mode is subjected to on-wafer load-pull measurements and the resulting power-sweep data are compared against the model, as shown in Fig. 16. The model is verified to be capable of accurately estimating the large-signal metrics such as P_{out}, G_t, power added efficiency (PAE), and I_{out} of a 2 × 180 µm device which is used for the PA design.

On top of modeling the large-signal device behavior, the MVS-G-RF is capable of modeling various RF noise sources in the device, which makes it suitable for estimating LNA NF while designing the Tx output stage. Fig. 17 (a) depicts the small signal sub-circuit. Device minimum NF (NF_{min}) and associated gain, comparing the model results with measurements is shown in Fig. 17 (b). Adding thermal noise sources to parasitic and channel resistances and shot noise sources to the gate heterostructure diodes is sufficient to model RF device noise. By capturing the shot and Johnson noise sources associated with device elements, the NF_{min} along with the associated gain can be predicted over the desired frequencies and bias points. The noise model depends only on small signal gain terms and dc terminal currents and requires no additional parameters. At bias of V_{DS}=12 V used in the LNA design and $V_{GS}=V_t$ + 0.15 V, NF_{min}=2 dB and G_{assc}=15 dB which is correctly predicted by the model.

VII. Future Direction for The Highly Integrated IEEE 802.11p Radio

As shown in [3] and [4], a 5GHz transceiver circuit except a high-power, high-efficiency RF frontend can be integrated in CMOS technology, taking advantage of the low cost integration of CMOS. To combine a CMOS transceiver with a GaN RF frontend, we intend to pursue process-level (i.e. single die) integration [2]. Recently reported new approaches also support the design of GaN circuits combined with CMOS ones which

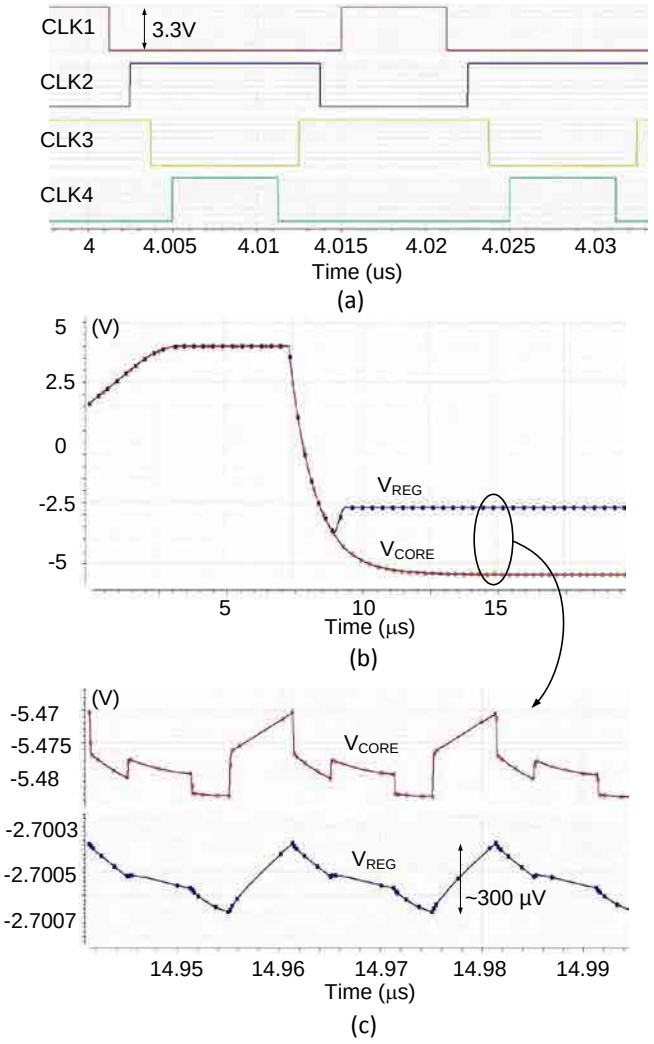


Fig. 19. Simulation results of the negative bias generation circuit: (a) multi-phase clock input, (b) negative voltage output, and (c) output ripple voltage

can be integrated together in process-level [14], package-level [15], or system-level [16]. The CMOS+GaN 802.11p radio can be integrated on mobile devices as well as cars for D2D communications, as depicted in Fig. I.

Another concern is that the designed GaN RF frontend requires several negative gate bias voltages since depletion mode GaN HEMT devices are used in the design. Unlike CMOS MOSFETs, GaN HEMTs have been developed with the focus of the performance of depletion mode devices. Although an enhancement mode GaN HEMT has advantages on circuit complexity and cost, it is not yet in the mainstream due to the difficulty in an accurate control of threshold voltage along with low on-resistance and high breakdown voltage. Thus, considering the GaN HEMT performance, adoption of depletion mode devices with negative bias generation circuity is preferable to achieve better performance and simple circuit design. In this section, a CMOS negative biasing circuit is proposed for the potential CMOS+GaN radio.

The functional block diagram of the CMOS negative bias generation circuit is illustrated in the Fig. 18. Aside from a core cell and a regulation circuit, the actual design comprises a ring oscillator and a clock splitter to generate multi-phase clock signals [17]. The circuits are designed using GlobalFoundries' CMOS 0.18 μm technology to demonstrate a promising negative biasing method with CMOS devices for depletion mode GaN HEMTs. The ring oscillator generates the fixed 50 MHz internal clock which is fed into the clock splitter. The reference generator utilizes a close-loop bandgap reference circuit to produce a stable temperature compensated V_{REF} between 0 to 300 mV with a resolution of 2.3 mV obtained through the 7 bit control input. The clock splitter generates 4-phase clocks with non-overlapping edges, as shown in Fig. 19 (a). The core cell utilizes these multi-phase clock signals to alternate charge pumping actions which push the negative charge towards its output. The negative voltage is mounted on a 5 pF hold capacitor, C_3, which limits the voltage ripple out of the core cell. Since this node is the most negative potential in the entire circuit, all the current rushes to discharge this node, which causes its voltage to increase momentarily. This is resisted by the core cell, thus generating the voltage ripple. The voltage ripple is, therefore, directly proportional to the load current and inversely proportional to the clock frequency as shown in (10).

$$V_{RIPPLE} \propto \frac{I_{LOAD}}{f_{CLK}} \tag{10}$$

The unregulated negative voltage is delivered to the regulation circuit which employs negative feedback loop and compares output sample to the clean reference, V_{REF} to filter out the input ripples and provide a stable and well regulated voltage at the output, as defined in (11).

$$V_{OUT} = 2\,V_{REF} - V_{DD} \tag{11}$$

In order to avoid potential device breakdown issues due to negative voltage generation, 3.3 V thick gate devices provided in the foundry design kit are employed. Cascode stages are also implemented to divide drain-to-source voltages such that they are safely bounded, and it is ensured that, at all instances, gate terminal voltages do not exceed the breakdown limit. Fig. 19 (b) and (c) show post-layout simulation results for a typical corner condition with I_{load} of 5 uA and C_{load} of 0.5 pF which are the modeled gate leakage and input capacitance of a GaN HEMT device, respectively. The stability of the feedback loop and the circuit performances have been thoroughly verified across all PVT corner variations. The circuit is powered up from 1.8/2.5/3.3 V dc sources and the generated output voltage can be tuned from -3.3 V to -2.7 V with 4.6 mV resolution obtained through 7-bit control input. The steady state output voltage ripple is less than 500 μVpp for a leakage load current of under 5 μA and with 50 MHz clock. In normal operation, the circuit achieves more than 30 dB of ripple rejection over the input ripple due to the internal switching operation. The designed negative bias generation circuit presents a completely integrated solution to generate a regulated negative voltage in CMOS for depletion mode GaN HEMT devices requiring negative gate bias voltages.

VIII. Conclusion

In this paper, a fully integrated, high-power, high-efficiency GaN RF frontend is designed with a physics-based RF compact model extracted from GaN HEMT devices. Prototype performances are verified with fabrication in 0.25 μm GaN-on-SiC process and COB implementation. By employing a newly proposed architecture and a dual-bias linearization technique, both high efficiency and linearity are achieved in the RF frontend circuit. The RF compact model for GaN HEMTs shows good match with measurement data in both device and circuit levels, and successfully reflects nonlinear characteristics of the devices on real RF frontend circuit performance. A negative bias generation circuit for the depletion mode GaN HEMTs with negative threshold voltage is also proposed and verified by simulation using 0.18 μm CMOS technology PDK, for future GaN+CMOS integration. This paper demonstrates the first physics-based GaN HEMT compact model that is calibrated and verified all the way from device to circuit level, and the first single-chip GaN RF frontend compliant with the IEEE 802.11p standard for future D2D communications.

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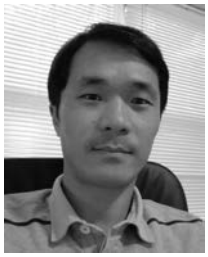

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