28.8dBm, High Efficiency, Linear GaN Power Amplifier with In-Phase Power Combining for IEEE 802.11p Applications

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***Abstract*— This letter presents a power amplifier (PA) for IEEE802.11p applications, adopting a new power combining technique in a 250nm GaN process. The proposed technique is used to improve the drain efficiency (DE) across the output power levels and meet the stringent error vector magnitude (EVM) requirement without any complicated input and output networks. The PA is implemented with a fabricated GaN die using the Chip-On-Board (COB) technology and tested with 27Mbps IEEE802.11p signal. It achieves -30.5dB EVM at 28.8 dBm output power with a back-off DE of 22.4% at 30V supply at 5.72GHz without pre-distortion. It also maintains more than 22% DE through supply voltage control while meeting its linearity requirement across the wide range of output power levels. The proposed circuit technique is viable for improving efficiency and optimizing linearity with its simple architecture.**

***Index Terms*— power amplifier, GaN, drain efficiency, error vector magnitude, IEEE 802.11p**

I. Introduction

Dedicated Short Range Communication (DSRC) based on IEEE 802.11p standard [1] is an emerging technology for vehicular communications. To mitigate multipath and highly mobile channel environments between cars, IEEE 802.11p specifies a double guard interval and a half guard band along with higher output power when compared with the IEEE 802.11a standard, which results in a maximum 27Mbps data rate in 10MHz bandwidth at 5.85~5.925GHz carrier frequency band with 28.8dBm maximum output power.

For the IEEE 802.11p standard PA's design, the high PAPR of OFDM signals should be considered while satisfying the EVM requirement. Since traditional Class AB PA suffers from significant reduction in efficiency at the back-off power, many studies have targeted to improve back-off efficiency by using a highly efficient nonlinear PA combined with a linear PA. The envelope elimination and restoration (EER) and envelope tracking (ET) [2] techniques introduce supply modulation as shown in Fig. 1(a). However, the technique requires a linear modulator and suffers from limited modulation bandwidth and delay mismatch between the envelope and phase paths. Another popular approach of combining linear and nonlinear PAs is called Doherty PA which is depicted in Fig. 1(b). Typically, a Doherty PA employs $\lambda/4$ transmission lines for power combining together with the load modulation, and requires a phase shifter to compensate for the phase shift from the load, resulting in the increase of design complexity. Recently, highly efficient GaN Doherty PAs [3] [4] are proposed, but they require complicated passive network design with large die area and show a sharp drop in efficiency below the back-off power.

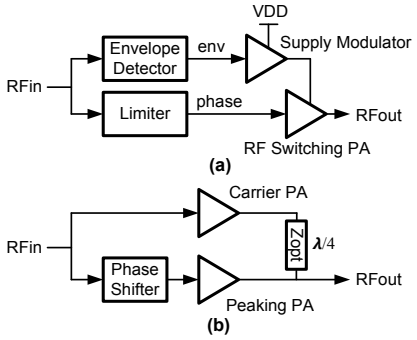

Fig. 1. (a) Classical EER PA architecture (b) Classical Doherty PA architecture

In this letter, a new power combining technique using Class AB and C biasing devices is proposed to achieve both linearity and efficiency across output power levels, while eliminating complex design issues in EER/ET and Doherty PAs.

II. PA Circuit with In-Phase Linear Power Combining Technique

Since conventional WiFi PAs for 5GHz band support up to 22dBm output power [5], our design focus is on the last PA stage to deliver 28.8dBm with around 10dB gain using high-power and high-voltage GaN HEMT devices. Fig. 2 shows the proposed schematic diagram including off-chip components on a PCB. In the proposed circuit, unlike the Doherty PA, the same RF input signal is applied to the M1 and M2 transistors' gate with different Class C and Class AB DC biasing while directly connecting the two transistors' drain, which greatly reduces the complexity of the input and output

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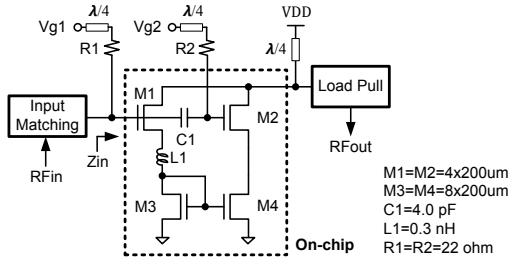


Fig. 2. Proposed PA circuit with off-chip biasing and load pull matching network

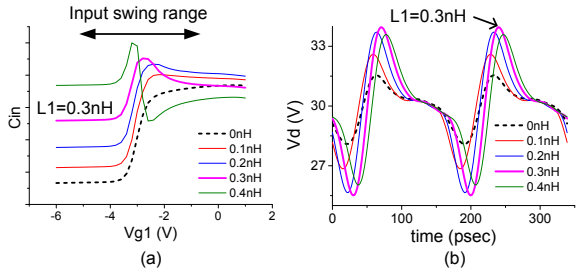


Fig. 3. Simulation of M1-L1-M3 Class C half circuit with encrypted GaN model : (a) C-V characteristics (b) drain voltage waveforms with L1 variations

networks by applying common load-pull method. Two tail devices, M3 and M4, act like a current mirror keeping the two in-phase signals from two devices linearly combined due to the inherent linear current relationship between two devices in the current mirror. The M3 and M4 tail devices are always self-biased in a saturation region regardless of the M1 and M2 biasing since GaN HEMTs are depletion mode devices with a negative pinch-off voltage. The DC biasing condition at the drain of M3 and M4 is around 1V. On the other hand, the supply voltage is 30V which is much higher than the Vds in the current mirror devices, thus the power loss induced by the current mirror is negligible in this GaN case.

A small L1 in the Class-C PA is used as shown in Fig. 2 that contributes to the reduction of the input capacitance variation. Since the input impedance of a GaN device can simply be modeled as both Cgs and Cgd in parallel, the input capacitance, Cin in (1) can be driven for the Class-C PA half circuit.

$$C_{in} = C_{gd} + \frac{C_{gs}(1-\omega^2 L C_{gs})}{(1-\omega^2 L C_{gs})^2 + (\omega R_s C_{gs})^2} \quad (1)$$

, where L=Ls+L1, and Ls and Rs are source parasitics in series

As depicted in Fig. 3(a), L1 should be carefully chosen to avoid undesirable peak and dip. Large capacitance variations due to the gate voltage swing cause large AM-PM distortion, so the reduction of the capacitance variation is helpful for achieving higher linearity. In addition, L1 helps to make the two drain voltage waveforms in-phase. Since Cin changes with L1 as shown in (1), the gate voltage waveform also changes with L1 and eventually generates a phase-shifted and higher-amplitude waveform at the drain of the Class-C PA as depicted in Fig. 3(b). Hence the two voltages from the two PAs can be combined efficiently at the drain. Fig. 4 illustrates the effects of the proposed techniques in simulation. With a maximum average input power around 21~22dBm, the

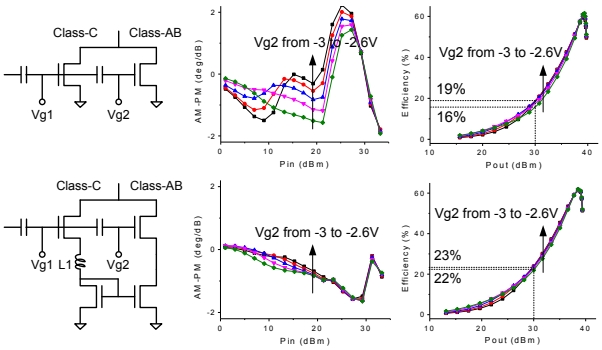


Fig. 4. Effects of the proposed techniques on linearity and efficiency

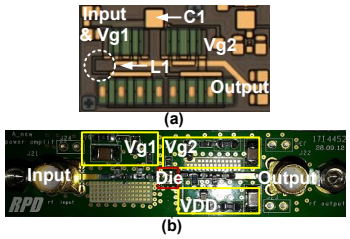


Fig. 5. (a) die microphotograph of the proposed PA, (b) a prototype board

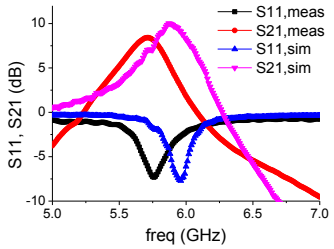


Fig. 6. Measured and simulated gain (S21) and input matching (S11)

proposed circuit shows less AM-PM distortion and better efficiency at the maximum average output power around 29~30dBm. The two circuit topologies are also compared with Vg2 variations when Vg1 (i.e. Class-C biasing) is fixed to a shallow Class-C biasing of -3.2V as shown in Fig. 4.

III. PA IMPLEMENTATION AND EXPERIMENTAL RESULTS

A prototype is designed and fabricated in Cree's 0.25um GaN HEMT process. The die microphotograph of the GaN circuit is shown in Fig. 5(a) and its area is 1.6mm x 0.8mm including pads. The input and output matching networks determined by load pull simulation are implemented on PCB with RO4350B material. A prototype board using the COB technology is depicted in Fig. 5(b). For gate biasing, two 22-ohm resistors for R1 and R2 in Fig. 2 are used for stabilizing the PA. The center frequency of the designed PA is shifted from 5.89GHz to 5.72GHz mostly due to the variations of external L and C components with limited values and models, including bond-wires. These together with the PCB metal loss affect the small signal gain, thus the measured gain is 8.4dB while the simulated gain is 9.9dB. Fig. 6 shows the measured and simulated gain (S21) and input matching (S11).

An IEEE802.11p OFDM signal with 10MHz bandwidth is used for all the EVM and efficiency measurements. The PA

Fig. 7. (a) Measured output power spectrum and (b) its constellation

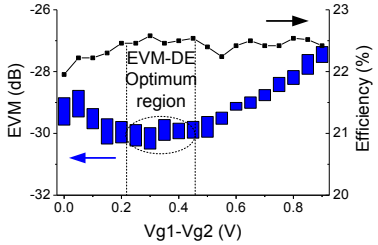


Fig. 8. Measured EVM (min-to-max) and DE with OFDM signals at 28.8dBm average output power against the offset between two gate bias voltages

achieves -30.5dB EVM and 22.4% DE at 28.8dBm average output power with 112.8mA at 30V supply, using -3.2V and -2.9V for Class-C and Class-AB biasing, respectively. Fig. 7 shows the 28.8dBm output power spectrum and constellation using 64-QAM signal, which meets the STA transmit power classification-D [1]. However, to satisfy the most stringent class D spectrum mask at more than 5MHz offset frequencies, digital pre-distortion (DPD) is required. DPD can also improve the EVM performance further. As shown in Fig. 8, high efficiency is maintained in the EVM-optimum bias offset between the Class AB and C devices. Since deep Class-C or shallow Class-AB biasing significantly degrade EVM or DE respectively, the best combination for the proposed combining is the deep Class AB and the shallow Class C PAs. This is because a shallow Class C PA preserves a certain degree of linearity with improved efficiency. Table I shows that the proposed PA can achieve higher efficiency while meeting the EVM requirement, compared to a conventional Class AB PA. Table I also shows that the proposed PA can maintain its high efficiency at lower output power. The lower output power is achieved in measurement by changing the supply voltage instead of using a complicated supply modulator. Fig. 9 illustrates the comparison of DEs across one-decade output power ranges with other efficiency enhancement techniques [2-8]. It can be seen that the average one-decade efficiency for this work is comparable with complex GaN Doherty PAs [3-4]. Considering that a PA usually operates at a lower power rather than a maximum power, system designers can benefit from the proposed PA. The die size of this work, [3] and [4] are 1.28mm^2, 21.62mm^2 and 3.15mm^2 respectively.

IV. Conclusion

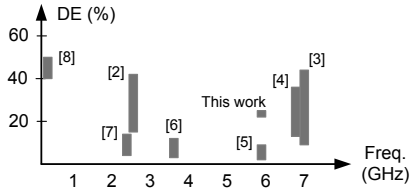
A new GaN PA circuit is proposed to enhance the overall efficiency across the output power with optimized EVM performance. A prototype PA is implemented using 0.25um GaN HEMT process and measured using IEEE 802.11p signal at 5.72GHz. The PA achieves -30.5dB EVM and 22.4% DE with 28.8dBm output power at 30V supply and maintains the DE at lower output power with lower supply voltage. This work allows for low cost PA design and the best performance of a PA for DSRC and WiFi applications at 100mW~1W output power in 5GHz frequency band, which enables system level power saving across output power levels with high efficiency.

TABLE I
Comparison between a Class-AB PA and the Proposed PA

	VDD (V)	Pout (dBm)	EVM (dB)**	DE (%)
Class AB*	30	30	N.A.	20.9
This Work	30	30	-26.4	25.6
	30	28.8	-30.5	22.4
	18	23	-25.1	22.8
	12	20	-25.7	22.3

* A conventional Class AB PA using the same GaN technology is simulated using a 5.72GHz single-tone signal with ideal load-pull matching conditions. The device size is chosen to be the same as the sum of M1 and M2 sizes in the proposed design. The DE is measured at the 6dB back-off power.

** EVM is measured using IEEE802.11p OFDM signals.



This work : Proposed, 20~30dBm, -30.5dB EVM @ 28.8dBm
[2] : GaAs/CMOS ET, 19-29dBm, -34.4dB EVM (w/ DPD) @ 29dBm
[3] : GaN Doherty, 20-30dBm (7-dB back-off), EVM N.A. (single-tone)
[4] : GaN Doherty, 17.5~27.5dBm (7.5-dB back-off), EVM N.A.
[5] : InGaP Class-AB, 12~22dBm, -30.5dB EVM @ 22dBm
[6] : CMOS Doherty, 9.4~19.4dBm, -26.6dB EVM @ 19.4dBm
[7] : CMOS Doherty, 4.5~14.5dBm, -26.4dB EVM @ 14.5dBm
[8] : CMOS Switch-mode PA, 15~25dBm, Nonlinear

Fig. 9. Comparison of DE across one decade output power ranges between the proposed and other PAs

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