

A Low Phase Noise 24/77 GHz Dual-Band Sub-Sampling PLL for Automotive Radar Applications in 65 nm CMOS Technology

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Abstract—A low phase noise 24/77 GHz dual-band sub-sampling PLL with a dual-band VCO is presented. Implemented in 65nm CMOS technology, the proposed PLL occupies an area of $900 \mu\text{m} \times 550 \mu\text{m}$. The measured phase noise is -120.0 and -108.5 dBc/Hz at 1 MHz offset in 24 and 77 GHz modes respectively. With 1.3 V supply, the power consumption is 26.4 and 31.5 mW for 24 and 77 GHz modes respectively. Compared with other state-of-the-art works, the proposed PLL has the best phase noise performance among all of reported PLLs for automotive radar applications.

Index Terms—Phase-locked loop (PLL), automotive radar, dual-band, sub-sampling, low phase noise, 24 GHz, 77 GHz, voltage-controlled oscillator (VCO), CMOS.

I. INTRODUCTION

Thanks to the advance of semiconductor technology, low cost millimeter-wave (mm-wave) circuits implemented in CMOS are demonstrated in recent years. The applications at mm-wave include high data rate communication, point-to-point wireless links, automotive radar, and mm-wave imaging. An automotive radar can make driving safe and comfortable. A radar operating in 24 GHz band is suitable for short or middle range applications including side-crash avoidance, parking assist, and so on. On the other hand, a 77 GHz radar is good for long range applications such as adaptive cruise control. The automotive radar combined both 24 and 77 GHz bands is desired to provide a complete solution and reduce area and cost [1].

Phase-locked loop (PLL) is an important component in the transceiver. The challenges of mm-wave PLL design are high frequency, wide locking range, low phase noise, and low power. However, generally there are trade-offs between these performances in CMOS technology. The PLL requirements for automotive radars are demanding especially the phase noise, because the close-in phase noise is a parameter of very strong influence to the resolution and sensitivity of a radar system. Many 24 or 77 GHz band CMOS PLLs have been reported, but their phase noise are limited by the classical PLL structure [1]–[3]. On the other hand, sub-sampling PLL has the potential of low phase noise by adopting sub-sampling phase detector (SSPD) and removing the noisy dividers [4], [5].

In this paper, a 24/77 GHz dual-band sub-sampling PLL is demonstrated in 65 nm CMOS technology. A dual-band VCO that can work in 24/77 GHz bands to save the area is presented.

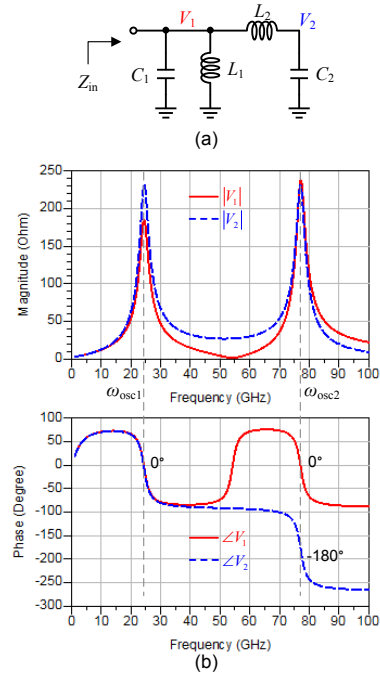


Fig. 1. (a) Schematic of dual-band LC tank, and (b) its frequency response.

The sub-sampling structure is adopted to achieve low phase noise. This paper is organized as follows. Section II presents the the dual-band VCO design. Section III describes the dual-band sub-sampling PLL. Finally, the measurement results are shown, and the conclusion is summarized.

II. DUAL-BAND VCO

To realize the dual-mode VCO, the dual-band loading is adopted. A properly designed fourth-order passive LC tank can provide two required resonant frequencies. Fig. 1(a) shows the schematic of a dual-band LC tank, where all of the components are ideal. Its input impedance (Z_{in}) can be expressed as

$$Z_{in} = \frac{sL_1(s^2L_2C_2 + 1)}{s^4L_1C_1L_2C_2 + s^2(L_1C_1 + L_1C_2 + L_2C_2) + 1}. \quad (1)$$

The circuit oscillates if the denominator of Z_{in} goes to zero. Consequently, the two oscillation frequencies, ω_{osc1} and ω_{osc2} ,

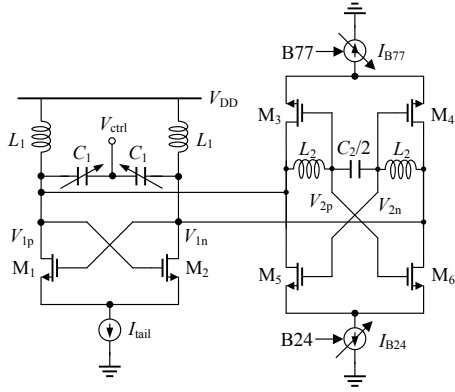


Fig. 2. Schematic of the proposed dual-band VCO.

are given by

$$\omega_{\text{osc}1,2}^2 = \frac{1}{2} \left(\omega_1^2 (1 + \alpha) + \omega_2^2 \mp \sqrt{\left((\omega_1 + \omega_2)^2 + \alpha \omega_1^2 \right) \left((\omega_1 - \omega_2)^2 + \alpha \omega_1^2 \right)} \right), \quad (2)$$

where $\omega_1 = 1/\sqrt{L_1 C_1}$, $\omega_2 = 1/\sqrt{L_2 C_2}$, and $\alpha = L_1/L_2$.

Fig. 1(b) plots the simulated frequency response of V_1 and V_2 . The magnitudes of both V_1 and V_2 peak at the two resonant frequencies $\omega_{\text{osc}1}$ and $\omega_{\text{osc}2}$. The phases of V_1 and V_2 at the first resonant frequency $\omega_{\text{osc}1}$ are both 0° . In other words, V_1 and V_2 are in phase at $\omega_{\text{osc}1}$. On the other hand, the phases of V_1 and V_2 at $\omega_{\text{osc}2}$ are 0° and -180° respectively, and hence V_1 and V_2 are in anti-phase at $\omega_{\text{osc}2}$. This important observation provide a solution to switch oscillation band between $\omega_{\text{osc}1}$ and $\omega_{\text{osc}2}$. Let us suppose that the gain condition of Barkhausen criteria is always met. If we force V_1 and V_2 to be in phase, the tank would resonate at $\omega_{\text{osc}1}$. If V_1 and V_2 are in anti-phase, the resonant frequency will be $\omega_{\text{osc}2}$.

The schematic of the proposed dual-band VCO is shown in Fig. 2. C_1 and C_2 include the parasitic capacitance of devices. The cross-coupled pair M_1 and M_2 is used to compensate the loss in tank. The control signal B24 and its inversion signal B77 are used to select the oscillation mode. When B24=1 and B77=0, tail current I_{B24} is on and I_{B77} is off, as shown in Fig. 3(a). M_6 will force V_{1n} to be in anti-phase with V_{2p} . Since V_{1p} and V_{1n} are differential, V_{1p} is in phase with V_{2p} . The phase condition of the peak at $\omega_{\text{osc}1}$ in Fig. 1(b) is met, so the VCO works in 24 GHz mode. Similarly, When B24=0 and B77=1, tail current I_{B77} is on and I_{B24} is off, as shown in Fig. 3(b). M_3 will force V_{1p} to be in anti-phase with V_{2p} , so the VCO works in 77 GHz mode. Compared with other band-switching methods such as switched-capacitor and switched-inductor, the proposed method has no penalty of lowering tank quality factor due to loss in switches.

III. DUAL-BAND SUB-SAMPLING PLL

Fig. 4 shows the schematic of the proposed dual-band sub-sampling PLL in a dual-band automotive radar system. The

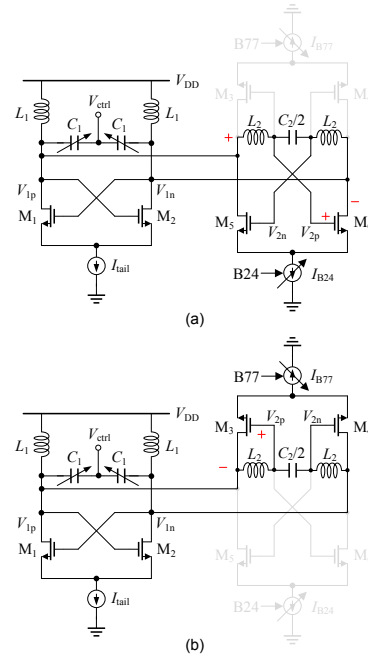


Fig. 3. Operations of the proposed dual-band VCO in (a) 24 GHz mode and (b) 77 GHz mode.

radar can be the pulse-based radar, or the frequency modulated continuous-wave (FMCW) radar. For the latter, an FMCW generator such as direct digital frequency synthesizer (DDFS) should be used as the reference input. The proposed PLL has been integrated with a dual-band low noise amplifier (LNA) [6] and a wideband mixer in a dual-band receiver to reduce the area. It can also work as the local oscillator (LO) in a two-step down-conversion W -band imaging system.

In order to reduce phase noise from divider, phase frequency detector (PFD), and charge pump (CP), the sub-sampling structure is adopted. The sub-sampling function can work as long as the ratio $N = f_{\text{fb}}/f_{\text{in}}$ is an integer. In our design, N is 16 for f_{in} is about 1.5 GHz. Thus, to avoid locking to a wrong frequency, the tuning range of 24 GHz mode should be less than 1.5 GHz, and that of 77 GHz mode less than 4.5 GHz. Since the divide-by-16 divider chain is removed, there is no noise contributed from dividers in 24 GHz mode. Even in 77 GHz mode, the divider's noise contribution is negligible. Moreover, the SSPD and CP noise in sub-sampling PLL is not multiplied by N^2 compared to that of a classical PLL [4]. Therefore, the phase noise of sub-sampling PLL can be very low if the reference input is clean.

The dual-band VCO, as discussed in the last section, is used to generate 24 or 77 GHz LO signal. For better isolation and driving capability, a dual-band 24/77 GHz buffer is inserted between the VCO and mixer or PA. Similar to the dual-band VCO, the dual-band buffer also uses a fourth-order LC tank as its load.

An dual-mode injection-lock oscillator (ILO), as shown in Fig. 5, is employed to realize two division modulus: one and three. When the PLL runs in 24 GHz mode, the ILO

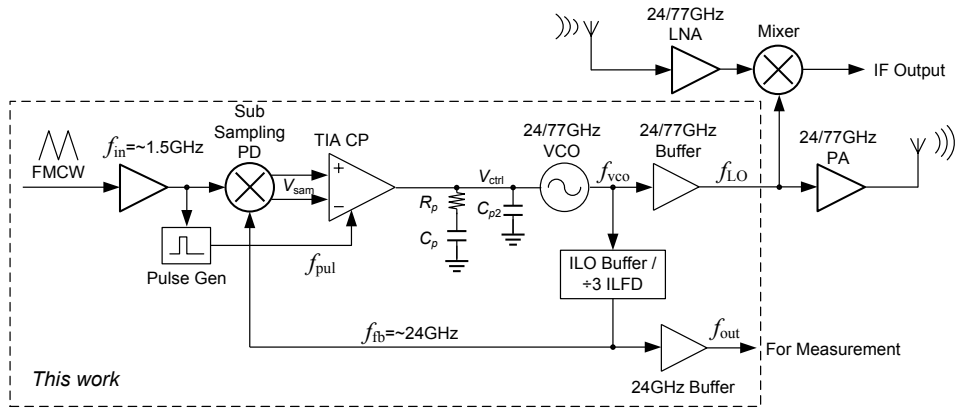


Fig. 4. Schematic of the proposed dual-band sub-sampling PLL in a dual-band automotive radar system.

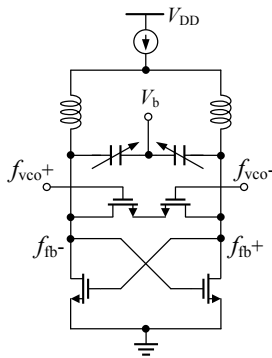


Fig. 5. Schematic of injection-locked oscillator (ILO) used as 24 GHz buffer or 77 GHz divide-by-3 divider.

severs as a 24 GHz buffer. While the PLL is switched to 77 GHz mode, the ILO works as a divide-by-3 injection-locked frequency divider (ILFD). For the second mode, the required oscillation frequency (about 25.7 GHz) of ILFD is a little higher than 24 GHz, so another varactor is used to tune its oscillation frequency. The voltage V_b can be tuned externally to compensate the frequency-drift due to PVT variations. A 24 GHz buffer is used to improve the driving capability for measurement.

The SSPD is a passive sample-and-hold circuit as shown in Fig. 6(a). It sub-samples the output of dual-mode ILO, f_{fb} , by using the clean reference input, f_{in} . The phase error between f_{fb} and f_{in} will be converted into the differential output voltage of SSPD, V_{sam} . A self-bias inverter is inserted to prevent the ILO affecting by the periodic change of input impedance of SSPD.

The output of SSPD, V_{sam} , is fed into the transimpedance amplifier charge pump (TIA-CP) and is converted into charge/discharge current, as shown in Fig. 6(b). Generally the loop bandwidth of sub-sampling PLL is too large for FMCW application. To reduce the loop bandwidth and maintain sufficient phase margin, large capacitor in LPF may be used but it is area consuming. One effective method is to reduce the CP turn-on period. The pulse generator shapes the

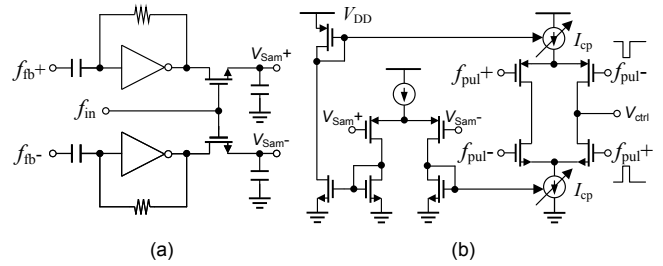


Fig. 6. Schematics of (a) sub-sampling phase detector (SSPD) and (b) tunable transimpedance amplifier charge pump (TIA-CP).

f_{in} into narrow pulses to reduce the loop bandwidth. Another practical method is to reduce the charge/discharge current. In our design, the charge/discharge current can be programmed to tune the loop bandwidth.

Next to the CP, the second-order low-pass filter (LPF) filters the output of CP, and presents its DC voltage to tune the VCO.

One often neglected block of the low phase noise PLL is the reference input buffer. In fact, the reference buffer will contribute significant phase noise if its slew-rate is small, especially when the reference is a slow sine-wave [4]. Thus, the driving capability of reference buffer should be large enough to ensure a high slew-rate and hence low phase noise.

IV. MEASUREMENT RESULTS AND CONCLUSION

The proposed dual-band PLL is implemented in GLOBAL-FOUNDRIES 65 nm CMOS technology. The die photograph is shown in Fig. 7. The area of PLL including pads is about $900 \mu\text{m} \times 550 \mu\text{m}$. The power consumption of the PLL including all buffers is 26.4 and 31.5 mW from 1.3 V supply for 24 and 77 GHz modes respectively. The output is taken from 24 GHz buffer through a 50Ω grounded coplanar waveguide (GCPW) transmission line, and directly measured by Agilent N5247A and E5052B.

The operation range of the PLL is from 24.12 to 24.88 GHz for 24 GHz mode. While in 77 GHz mode, the PLL is locked from 75.41 to 77.23 GHz. Fig. 8 illustrates the output

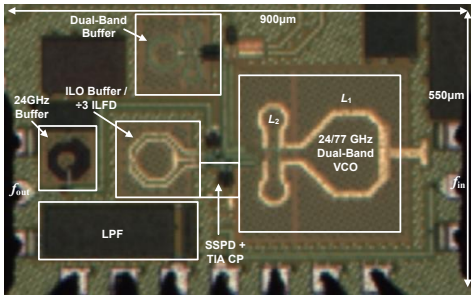


Fig. 7. Die photograph of the proposed PLL.

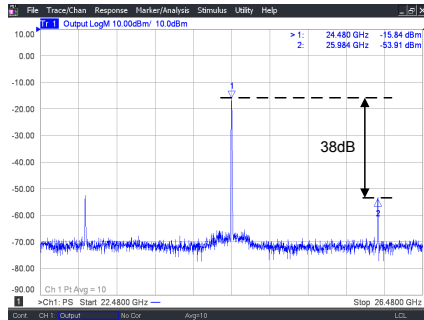


Fig. 8. Measured output spectrum of the proposed PLL in 24 GHz mode.

spectrum in 24 GHz mode. The reference spur is about 38 dB lower than the carrier.

Fig. 9 shows the phase noise of PLL. For small loop bandwidth, the PLL phase noise in 24 GHz mode is -120.0 dBc/Hz at 1 MHz offset. In 77 GHz mode, the PLL phase noise is about $-118.0+20\log(3)=-108.5$ dBc/Hz at 1 MHz offset for the measured output $f_{out} = f_{vco}/3$. For large loop bandwidth, the PLL phase noise is -113.4 and -103.2 dBc/Hz at 1 MHz offset in 24 and 77 GHz modes respectively. The measured performance of dual-band PLL is summarized is Table I.

A low phase noise 24/77 GHz dual-band sub-sampling PLL for automotive radar applications is presented and implemented in 65nm CMOS technology. A dual-band VCO is used to provide 24/77 GHz LO signals. The proposed PLL can achieve -120.0 and -108.5 dBc/Hz at 1 MHz offset in 24 and 77 GHz modes respectively. The power consumption is 26.4 and 31.5 mW from 1.3 V supply for 24 and 77 GHz modes respectively. To the best of authors' knowledge, this is the first 24/77 GHz dual-band PLL in CMOS technology, and it has

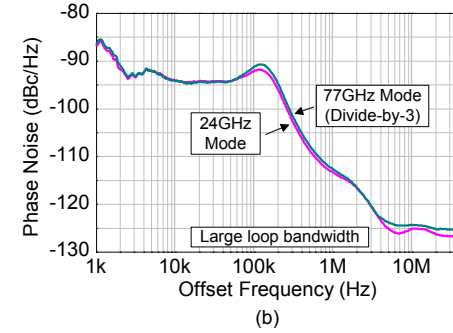
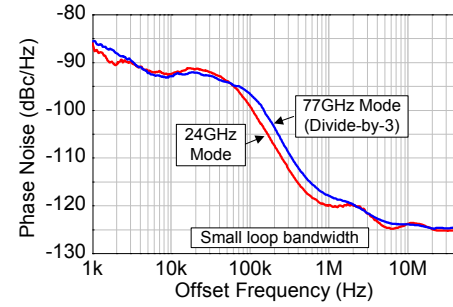


Fig. 9. Measured phase noise of the proposed PLL with (a) small and (b) large loop bandwidth.

the best phase noise performance among all of reported PLLs for automotive radar applications.

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TABLE I
COMPARISON OF STATE-OF-THE-ART PLLS FOR AUTOMOTIVE RADAR APPLICATIONS

Reference	Technology	Supply Voltage (V)	Reference Frequency (MHz)	Frequency Range (GHz)	Phase Noise (dBc/Hz) at 1 MHz Offset	Power Consumption (mW)
[1]	0.18 μ m BiCMOS	2.5	100	23.8~26.95 75.67~78.5	-114 -103.5	50 75
[2]	90nm CMOS	1.2	75	78.1~78.8	-85	101
[3]	65nm CMOS	1.2	700	75.6~76.3	-85.33	73
[5]	65nm CMOS	1.2	~1750	79.2~87.2	-100.2	54
This Work	65nm CMOS	1.3	~1500	24.12~24.88 75.41~77.23	-120.0 -108.5	26.4 31.5