LOW-POWER 2.4/5.15-GHz DUAL-BAND VOLTAGE-CONTROLLED OSCILLATOR

Yannan Miao, Chirn Chye Boon, Manh Anh Do, Kiat Seng Yeo, and Yuxiang X. Zhang
School of Electrical and Electronic Engineering, Nanyang Technological University, Nanyang Avenue, Singapore 639798; Corresponding author: miao0012@e.ntu.edu.sg

Received 28 January 2011

ABSTRACT: *We proposed a 2.4/5.15 GHz dual-band voltage-controlled oscillator which consists of a voltage-controlled oscillator and an injection-locked oscillator. Its upper and lower band frequencies are 4.48∼5.86 GHz and 2.24∼2.93 GHz, respectively. With the power consumption of 3.2 mW, their phase noises are −115 and −121 dBc/Hz at 1 MHz offset.* © 2011 Wiley Periodicals, Inc. Microwave Opt Technol Lett 53:2495–2497, 2011; View this article online at wileyonlinelibrary.com. DOI 10.1002/mop.26329

Key words: *differential injection; voltage-controlled oscillator; injection-locked frequency divider; dual-band VCO*

1. INTRODUCTION

The application of wireless LANs (WLANs) at the 2.4-GHz instrumentation, scientific, and medical (ISM) band has been experiencing significantly growth in the recent years. The newer WLAN at 5 GHz in the Unlicensed National Information Infrastructure (UNII) band has more bandwidth for more channels and higher data rates. With the increase in the demand for higher data rates, WLAN chips must be able to cover both the ISM and UNII bands to ensure smooth migration.

One of the major problems in a dual-band transceiver is the implementation of a dual-band voltage-controlled oscillator (DVCO). A voltage-controlled oscillator (VCO) with wide tuning range is a simple method to cover the two bands. However, the VCO needs a varactor with large variable percentage in capacitance, which is usually unavailable in a standard CMOS technology. Another method is that switching devices are used in the inductance capacitance (LC) tank to change either capacitance [1] or inductance [2]. The resistance of the switching devices, however, is likely to cause the degradation of the tank quality factor (Q) and, consequently, the phase noise of the VCO. Moreover, two independent VCOs with simple stacking topology can be used to provide two frequencies [3], but their phase noises are deteriorated due to a limited supply voltage. In addition, the total power consumption is unavoidably high if two phase-locked loops (PLLs) are implemented in a dual-band transceiver.

In this article, the design of a DVCO will be presented, which has low power consumption and low phase-noise outputs. In Section 2, the topology and schematic of the proposed circuit will be presented. Subsequently, the design techniques will be discussed and verified by simulation results. In Section 3, the measurement results will be showed, summarized, and compared with other DVCOs. Finally, the conclusions will be drawn in Section 4.

2. PROPOSED DESIGN OF DVCO

2.1. Topology of the Proposed DVCO

In a 2.4/5.15 GHz DVCO, the 5.15-GHz frequency band is far away from the 2.4-GHz frequency band but is near to the frequency of 4.8 GHz that is the second harmonic of 2.4 GHz. Thus, it is not necessary to design a VCO with wide tuning range from 2.4 to 5.15 GHz. Instead, it is easy to design a VCO with narrow tuning range from 4.8 to 5.15 GHz. Following to the VCO, a frequency divider is designed to operate at the 2.4-GHz frequency band, which is an injection-locked frequency divider (ILFD) in the DVCO for high-frequency operation and low power consumption.

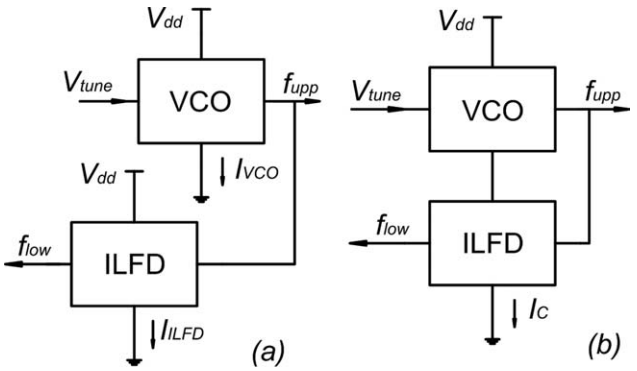

Figure 1 A VCO and an ILFD (a) on cascade structure (b) on stacking structure

Based on a conventional topology, the VCO and ILFD are implemented in cascade, shown in Figure 1(a). For the DVCO application, the power is consumed not only by the VCO but also by the ILFD. Thus, it is significantly increased, especially when large current is required to bias the passive components at high-frequency operation. The total power consumption P_{total} is $V_{\text{dd}}I_{\text{VCO}} + V_{\text{dd}}I_{\text{ILFD}}$, where I_{VCO} and I_{ILFD} are the bias currents in the VCO and ILFD, respectively. In a novel topology of the DVCO, the VCO can be stacked on top of the ILFD for reducing the power consumption. Thus, the bias current I_{C} in the VCO can be reused by the ILFD, shown in Figure 1(b). Conclusively, P_{total} is only $V_{\text{dd}}I_{\text{C}}$, which is smaller than in the conventional topology if I_{C} is smaller than the sum of I_{VCO} and I_{ILFD}.

2.2. Schematic of the Proposed DVCO

The schematic of the proposed DVCO is shown in Figure 2, which consists of a VCO (in the left box) and an ILFD (in the right box). The VCO is based on a complementary LC-tank oscillator, which consists of an inductor L_1, two n-type metal-oxide-semiconductor FET (NMOS), and two p-type metal-oxide-semiconductor FET (PMOS) transistors to regenerate the signal. At the differential outputs of the VCO, $v_{\text{upp+}}$, and $v_{\text{upp−}}$, the output frequency f_{upp} of VCO is used for the upper band operation. A varactor C_{var1} is connected between $v_{\text{upp+}}$ and $v_{\text{upp−}}$ and tuned by a DC voltage V_{tune}.

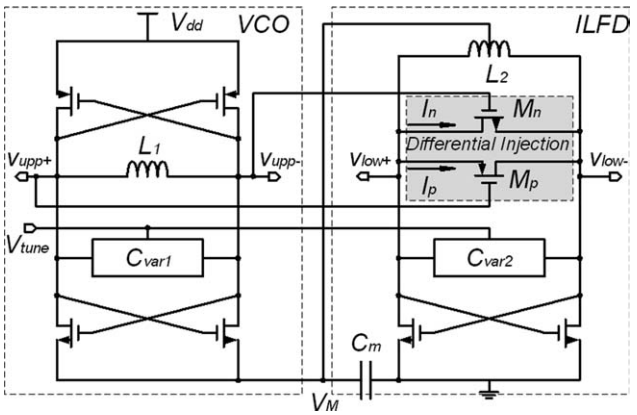

Figure 2 Schematic of the proposed DVCO

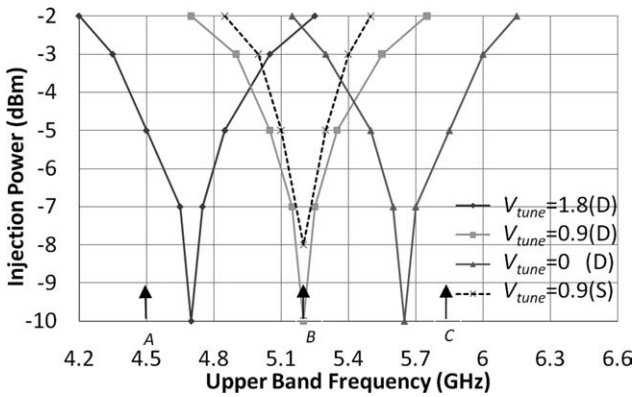

Figure 3 The output frequency of VCO and the operation range of ILFD

The ILFD is based on NMOS-only LC-tank oscillator, which consists of another inductor L_2 and a pair of cross-coupled NMOS transistors to regenerate the signal. At the differential outputs of the ILFD, v_{low+}, and v_{low-}, the output frequency f_{low} of ILFD is used for the lower band operation. One PMOS injection transistor M_p and one NMOS injection transistor M_n are connected in parallel between v_{low+} and v_{low-}. Their gates are connected to v_{upp+} and v_{upp-}, which generate the injection currents I_p and I_n, respectively. Another varactor C_{var2} between v_{low+} and v_{low-} is also tuned by V_{tune}. Moreover, a fixed capacitor C_m is placed between V_M and *gnd*, which is used to decouple the AC signal and to attenuate the voltage variation on V_M. In addition, another varactor is connected in parallel to C_{var2}, not shown in Figure 2 for simplicity. It will be independently tuned once and then fixed to offset the effect of process variation on the ILFD resonant frequency f_0.

2.3. Design Techniques of the Proposed DVCO

Phase noise is an important characteristic to measure the quality of an oscillator. The VCO based on complementary structure has better phase noise than the one based on NMOS-only structure [4]. In the proposed DVCO, the VCO is designed based on the complementary structure, which occupies larger voltage headroom. The phase noise of the output of ILFD is significantly dependent on the output of VCO. Without additional noise from the ILFD, the phase noise of the output of ILFD is 6 dB less than one of the VCO because f_{low} is equal to $(1/2)f_{upp}$.

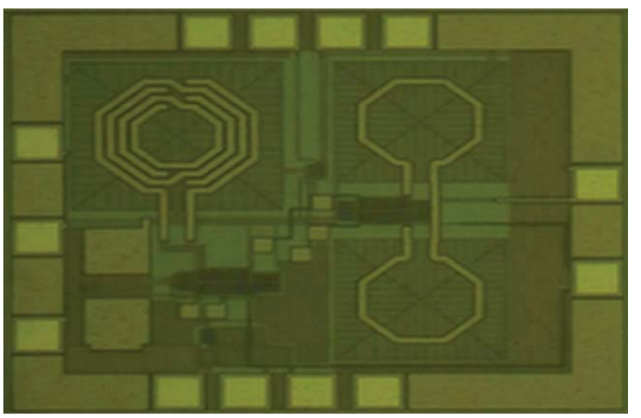

Figure 4 The die microphotograph of the proposed circuit. [Color figure can be viewed in the online issue, which is available at wileyonlinelibrary.com]

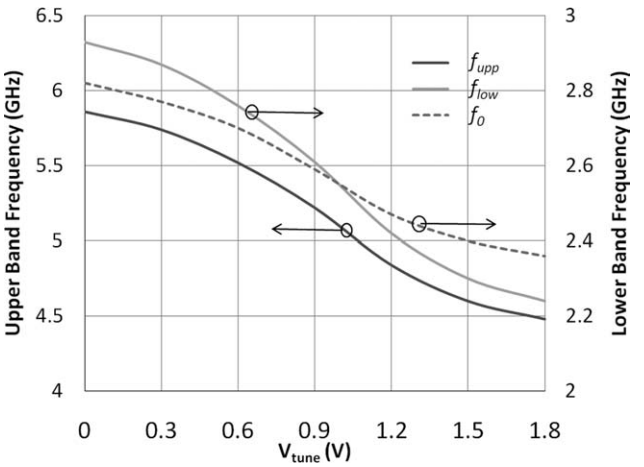

Figure 5 The tuning characteristics of the output frequencies

For low phase noise of the ILFD, it is required that the ILFD is injection locked by the output of VCO. Thus, it is important whether f_{upp} is in the operation range of the ILFD Δf. In the proposed circuit, the varactors C_{var1} and C_{var2} are implemented in the VCO and ILFD, respectively, which are tuned by V_{tune}. Thus, the capacitance of the LC tanks in the VCO and ILFD can be increased or decreased simultaneously. Consequently, f_{upp} varies with Δf. Because of parasitic capacitance and process variation, it is impossible that with any value of V_{tune}, $(1/2)f_{upp}$ is at the center of Δf. Therefore, it is also important to extend Δf with any fixed value of V_{tune}.

In a conventional ILFD [5], the injection signal is from single input and the differential output from the VCO is used insufficiently. With a limited transconductance of the injection transistor, the ILFD has small injection current and consequently, narrow operation range. In the proposed circuit, differential injection is implemented and shown in Figure 2 (in the gray area). The differential outputs of the VCO are both connected to the gates of M_p and M_n instead of single injection. The injection currents I_p and I_n are generated in the same direction by v_{upp+} and v_{upp-}, respectively. Based on Adler's lock-range equation in [6], Δf is extended by the increased injection current that is the sum of I_p and I_n.

These design techniques can be verified by simulation. First, the simulation results in Figure 3 show that Δf is extended by

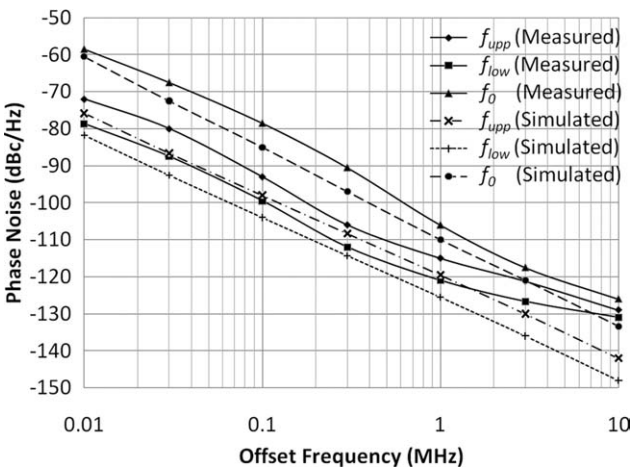

Figure 6 The phase noise of the output frequencies

TABLE 1 The Performance Comparisons of the DVCOs

References	V_{dd} (V)	P_{total} (mW)	f_{op} (GHz)/Δf (Hz)	Tuning Range (GHz)	Phase Noise (dBc/Hz)	FoM* (dBm)
[7]	1.8	8	5.7/1 M	1.3	−98	−164.1
			2.85/1 M	0.65	−110	−170
[3]	1.8	6.11	5.23/1 M	0.25	−120	−186.6
			2.44/1 M	0.11	−126	−186.1
[8]	1.8	16.5	5.74/1 M	1.01	−118	−184.4
			2.98/1 M	0.64	−124	−184.1
[2]	1.8	7.56	4.56/1 M	1.2	−121	−185
			2.3/1 M	0.25	−120	−179
This work	1.8	3.2	5.86/1 M	1.38	−115	−187.1
			2.93/1 M	0.69	−121	−190.1

* FoM = $L(\Delta f) - 20\ log\ (f_{op}/\Delta f) + 10\ \log\ (P_{DC}/1\ mW)$

differential (D) injection instead of single (S) injection. It is an example at V_{tune} of 0.9 V that Δf with single injection is narrower than the one with differential injection. Second, the simulation results show that Δf is shifted with f_{upp} by varying V_{tune}. At V_{tune} of 1.8, 0.9, and 0 V, f_{upp} are shown by three arrows A, B, and C, respectively. Simultaneously, the values of Δf with differential injection are shown at V_{tune} of 1.8, 0.9, and 0 V. It can be seen that f_{upp} is always covered by Δf when the injection power is larger than −5 dBm. Thus, the ILFD is always injection locked if the output power of VCO is larger than −5 dBm.

3. MEASUREMENT RESULTS

The proposed DVCO has been designed and fabricated in the 0.18 μm CMOS technology. The die microphotograph of the proposed circuit is shown in Figure 4. The overall die size is 0.85 × 0.92 mm^2. At the supply voltage of 1.8 V, the power consumption of the DVCO is 3.2 mW. Before the output buffers for measurement, the output power for f_{upp} and f_{low} are 0.9 and −2 dBm, respectively.

The tuning characteristics of f_{upp}, f_{low}, and f_0 are shown in Figure 5. If the injection transistors are properly set by DC biasing, f_{upp} is tuned from 4.48 to 5.86 GHz by varying V_{tune} while f_{low} is from 2.24 to 2.93 GHz. With any value of V_{tune}, f_{low} is exactly equal to $(1/2)f_{upp}$, so it can be concluded that the ILFD is always injection locked by the VCO. Otherwise, f_0 is tuned from 2.36 to 2.82 GHz by varying V_{tune}.

The phase noises of the VCO and ILFD are shown in Figure 6. The solid lines represent the measured results, whereas the dotted lines represent the simulated results. At the resonance of the ILFD, the phase noise of f_0 is only −106 dBc/Hz at 1 MHz offset. However, the phase noise of the ILFD can be suppressed by injection locking. With properly injection, the measured phase noises of f_{upp} and f_{low} are −115 dBc/Hz and −121 dBc/Hz at 1 MHz offset, respectively. As expected, the phase noise of ILFD is almost 6 dB less than the phase noise of VCO.

Table 1 summarizes the measured performance of the proposed DVCO, including the figure of merit (FoM) of VCO. In comparison with other DVCOs in the 0.18-μm CMOS technology, the proposed circuit achieves the lowest power consumption, the widest tuning range, and the best performance on the FoM.

4. CONCLUSIONS

This article proposed a 2.4/5.15 GHz DVCO, which has been fabricated in the 0.18-μm CMOS technology. The DVCO features state-of-the art performance on tuning range, power consumption, and the FoM. It can be used in a low-power dual-band transceiver, which supports both the ISM and UNII bands for WLAN applications.

REFERENCES

1. D. Baek, J. Kim, and S. Hong, A dual-band (13/22-GHz) VCO based on resonant mode switching, IEEE Microwave Wireless Compon Lett 13 (2003), 443–445.
2. H.L. Kao, D.Y. Yang, C.H. Kao, Y.C. Chang, and B.S. Lin, Switched resonators using adjustable inductors in 2.4/5 GHz dual-band LC VCO, Electron Lett 44 (2008), 299–300.
3. Y. Li, Y.O. Jing, Y.H. Shen, and Z.S. Lai, A stack-mode dual-band voltage-controlled oscillator for multistandard wireless applications, In: 8th International Conference on Solid-State and Integrated Circuit Technology, 2006. ICSICT '06, 2006, pp. 1925–1927.
4. A. Hajimiri and T.H. Lee, Design issues in CMOS differential LC oscillators, IEEE J Solid-State Circuits 34 (1999), 717–724.
5. T.-N. Luo and Y.-J.E. Chen, A 0.8-mW 55-GHz dual-injection-locked CMOS frequency divider, IEEE Trans Microwave Theory Tech 56 (2008).
6. R. Adler, A study of locking phenomena in oscillators, Proc Inst Radio Eng 34 (1946), 351–357.
7. J. Lin, et al., A 1.8-V 2.4/5.15-GHz dual-band LC VCO in 0.18-μm CMOS technology, IEEE Microwave Wireless Compon Lett 16 (2006), 194–196.
8. S.L. Jang, Y.H. Chuang, S.H. Lee, L.R. Chi, and C.F. Lee, An integrated 5/2.5-GHz direct-injection locked quadrature LC VCO, IEEE Microwave Wireless Compon Lett 17 (2007), 142–144.

DESIGN OF A NOVEL UWB OMNIDIRECTIONAL SEMICIRCULAR DISK ANTENNA

Pengyu Zhang, Lijia Chen, and Jinghui Qiu
Department of Microwave Engineering, Harbin Institute of Technology, Harbin, Heilongjiang, China; Corresponding author: pyzhang.mw@gmail.com

Received 28 January 2011

ABSTRACT: *In this article, a novel omnidirectional semicircular disk antenna is investigated both numerically and experimentally. Two prototypes of different dimensions are fabricated and measured, resulting in a best impedance bandwidth ratio of more than 80:1. The antenna is considerably promising for future ultrawide-band applications.* © 2011 Wiley Periodicals, Inc. Microwave Opt Technol Lett 53:2497–2501, 2011; View this article online at wileyonlinelibrary.com. DOI 10.1002/mop.26328

Key words: *UWB antenna; semicircular disk antenna; omnidirectional radiation pattern*