An Output Feedback-based Start-up Technique with Automatic Disabling for Battery-less Energy Harvesters

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Abstract—This paper presents a start-up circuit based upon output voltage feedback for thermal energy harvesting. The feedback loop consisting of an output load, a boost converter core, a charge-pump-based doubler and a CMOS inverter switch to track the output voltage and generate a reset signal to kick-start the boost converter. The proposed start-up circuit shows a remarkably improved start-up time of 35µs at the input voltage of 290mV. The start-up circuit is automatically disabled after the boost converter reaches steady-state. Only one off-chip component is required, improving the cost efficiency. The proposed start-up circuit consumes 3.2nW during the steady-state, aiding the boost converter to achieve an efficiency of 77% at input voltage of 290mV. It was designed in standard 65-nm CMOS process technology and occupies the area of 0.072mm².

Keywords—start-up; efficiency; energy harvesting; steady-state; disable

I. INTRODUCTION

Alternate ambient sources of energies have promising potentials for various biomedical and wearable applications that harvest them for long-term self-powered operations with or without batteries [1-3]. Thermal energy is an important source for such applications because of its easy accessibility in human body. However, a miniaturized TEG (Thermo-Electric Generator) usually exhibits sub-mW output power and an output voltage in the range of a few hundred millivolts from the limited available temperature difference between human body and the ambient, which is too low to directly support the electronic circuits. In addition, to achieve full energy autonomy, self-startup function is highly desired to kick-start the system operation from cold state. Furthermore, power hungry applications can deplete the stored harvested energy even before it can be recharged. Therefore, the major challenges in start-up circuit design are fast self-startup from low input voltages, up-conversion of the available low voltages to a higher usable voltage and executing these targets with high overall conversion efficiency.

Various state-of-the-art start-up techniques for energy harvesting have been reported [4-9]. Low start-up voltages have been achieved by utilizing MEMS switches, transistor threshold voltage trimming, off-chip transformers, and auxiliary LC oscillators to kick-start the boost converter operation. However, the mechanical motion-activated switch [4] requires external vibrational force that may not be ubiquitously available in the ambient condition.

Other fully electrical start-up techniques have also been reported [5-9]. However, post-fabrication threshold trimming and usage of large off-chip components reduce the cost efficiency in [5] and [7], respectively. Disabling of start-up section during circuit’s steady-state has been addressed by [6], [7] and [9], in order to enhance the overall efficiency. But usage of native NMOS transistors in [6-7] to achieve low voltage start-up, results in leakage even during the steady-state.

In this paper, a start-up circuit with automatic disabling function is presented with a highly efficient boost converter. It achieves fast start-up because of the constant feedback of the information about the output stage status. The feedback from the output generates a reset signal to turn on and off the switch to kick-start the auxiliary boost converter. The proposed harvester achieves the minimum start-up voltage of 290mV, and can generate the output voltage of 1V after 35µs.

II. PROPOSED ENERGY HARVESTER AND OPERATION

The block diagram of the proposed energy harvester system is illustrated in Fig. 1. The proposed harvester consists of three main units, namely, Starter, Main Control Unit, and Boost Converter Core. Starter comprises of a CMOS inverter-based switch (INV-SW), a charge-pump-based doubler (DOUBLER), and a ring oscillator. The Boost converter core consists of the power NMOS transistors NM0, NM1, and PMOS transistor PM, along with an off-chip inductor and an on-chip capacitor.

Unlike the start-up operation in [4], which relies on external ambient vibrations to turn on a MEMS switch, the proposed starter generates the one-time pulse necessary to turn NM0 on and off without any external source. Initially, when COUT is in discharged state, INV turns on NM0 and charges L. During this on-time of NM0 on and off without any external source. Initially, when COUT is in discharged state, INV turns on NM0 and charges L. During this on-time of NM0, some charges also leak through PM and raises VDD gradually. When VDD rises beyond the switching point of CMOS inverter INV-SW, INV turns NM0 off, thereby raising the node VDD from the stored energy present in the inductor. This feedback also ensures that NM0 will remain inactive until VDD is held at steady-state. The automatic reset of INV and hence the disabling of starter enhances the efficiency during the steady-
state. Fig. 2 shows the timing diagram explaining the start-up operation.

After the circuit is kick-started and the starter block is disabled, the main control unit is activated by VDD without using any other power source, and NM0 is replaced by NM1 to form the main boost converter. The level of VDD is regulated to be held at 1V or beyond by the clocked comparator (clocked by CLK2) with two inputs, VDIV and VREF. VDIV is the output of the voltage divider. It is at 0.7V when VDD is 1V. VREF is the output of the reference generator (Ref-Gen), which is 0.7V when VDD is 1V and above. The comparator output is directly fed to the gate of NM1. When VDD falls below 1V, the comparator output follows CLK2. This makes the main boost converter operate in the steady-state to maintain VDD at 1V. If VDD is above 1V, the comparator output turns off NM1 until VDD falls below 1V.

### III. CIRCUIT IMPLEMENTATION

#### A. Boost Converter Core

The boost converter comprises the power transistors NM1, NM0 and PM, where NM1 and NM0 swap roles for Auxiliary and Main Booster respectively, as shown in Fig. 3. The power transistors have been optimally sized to minimize the conduction losses. The switching losses have been minimized by choosing optimum frequency of operation in steady-state. The primary losses in a boost converter can be expressed as follows:

\[
\text{Conduction Loss} = \sum (I_{\text{IN,RMS}}^2 \times R_{\text{DS,N/P}}) + I_{\text{IN,RMS}}^2 \times R_{\text{ESR}} \quad (1)
\]

\[
\text{Switching Loss} = \sum (C_{\text{G,N/PVGATE}} \times f_s) + 0.5 \times C_{\text{PAR,VDD}} \times f_s \quad (2)
\]

#### B. Starter

The most essential circuit block in starter is INV-SW which acts as one-time reset for the power switch NM0, thus enabling the inductor L to discharge the stored energy and charge COUT during the second clock half-cycle. The VDD is directly fed back to the gates of the transistors in INV-SW. The power supply for INV-SW is supplied by the charge-pump-based DOUBLER output CP, which doubles the input voltage, as shown in Fig. 4. This is necessary to increase the voltage swing at INV so that it can turn on NM0 even if the available input voltage is in the sub-threshold region. The clock signals for the DOUBLER are provided by a ring oscillator powered only from VIN. The sizing of the transistors in INV-SW is adjusted in a manner such that the switching point of the inverter output INV is much lower than half of the voltage at CP. This ensures that INV is reset at a much lower VDD level, resulting in a smaller start-up time and start-up voltage.

During start-up, the final voltage across the capacitor approximately follows the relation:

\[
VDD \approx \sqrt{VD^2 + QT^2 + VIN^2} \quad (3)
\]

where, VD, QT and VIN are the diode-drop voltage, quality...
factor of the start-up network, and input source-voltage, respectively. QT takes into account the conduction losses in NM0, series resistance of L and resistive losses in the Starter. VDD is, however limited by the voltage drop VD, in the diode-connected PMOS, which is taken into account in the expression above.

C. Main Control Unit

The Main Control Unit consists of the blocks Ring Oscillator (Ring Osc), COMP, Voltage Divider and Ref-Gen. The Ring Osc here consists of a chain of current-starved inverters, where diode-connected MOSFETs are connected in series with the transistors of a conventional CMOS inverter, as shown in Fig. 5. COMP is a dynamic latched comparator that compares two signals during each clock pulse CLK2, generated by the ring oscillator. It utilizes the latching mechanism of two cross-coupled inverters as shown in Fig. 6 and functions in two different modes- pre-charge and evaluate. During the half cycle when CLK2 is off, the comparing branches are deactivated, and the nodes X and Y are pulled to VDD by the PMOSes parallel to both inverters, which is the pre-charge mode. The evaluate mode occurs during the on-time of CLK2, in which VDIV and VREF are compared. When VDIV is greater than VREF, the latch adjusts itself and the nodes X and Y are pulled to VDD, respectively, setting OUTN at 0 and OUTP at VDD. The nodes swap the values when VREF is greater than VDIV.

IV. PERFORMANCE AND DISCUSSIONS

A. Performance Analysis

The proposed harvester circuit was designed in standard 65-nm CMOS technology. The layout of the proposed harvester is depicted in Fig. 7. The active area including the on-chip capacitor is 0.072mm². The value of the capacitor implemented is 650pF, and the inductance of the off-chip inductor is 1mH. Fig. 8 shows the simulated waveforms of the start-up operation at the input voltages of 290mV (Fig. 8(a)) and 550mV (Fig. 8(b)), respectively. The harvester output is 1V at the input voltage of 290mV. The start-up times are 35µs and 30µs at the input voltage of 290mV and 550mV, respectively. The output voltage at 550mV input which achieves a higher gain during start-up, is controlled at 1.3V during steady-state as shown. Fig. 9(a) depicts the efficiency of the harvester over various loads. The peak efficiency of the boost converter is 77%. Fig. 9(b) shows the efficiency and the starter power at the steady-state for the input range of 0.3 – 1V, both of which degrade with input voltage. With the input level of 290mV, the quiescent power of the start-up circuit at the steady-state is 3.2nW, which is 0.0054% of the total circuit power consumption. The power consumption of the main control unit varies between 2 – 5µW for the input range of 0.3 – 1V.

B. Discussion

The primary benefits of the proposed start-up circuit are, (i) small start-up time, (ii) efficiency improvement by the proposed automatic disabling technique of start-up section, and (iii) active area reduction and minimization of off-chip components. With the exception of [8], the start-up circuits in [4-9] have start-up voltages less than 100mV, but either by

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<td>Min. Start-up Voltage (V)</td>
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<td>.095</td>
<td>.05</td>
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<td>Typical Input (V)</td>
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<td>.1</td>
<td>.03</td>
<td>25-.5</td>
<td>25-1</td>
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<td>Peak Efficiency (%)</td>
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<td>72††</td>
<td>73</td>
<td>--</td>
<td>77††</td>
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<tr>
<td>Area (mm²)</td>
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<td>.998</td>
<td>--</td>
<td>.072*</td>
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<tr>
<td>Start Time (µs)</td>
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<td>2.6E5</td>
<td>5E3↑↑</td>
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<td>35</td>
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<td>--</td>
<td>--</td>
<td>16E3↑↑</td>
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†Uses post-fabrication threshold trimming; †† External POR triggered.
**Area includes off-chip capacitor; *Area includes the on-chip capacitor.
††Boost Converter only; ↑↑Calculated at 100mV input
using motion activated off-chip mechanical switches, programmed dedicated clock generators, bulky transformers, native transistors or LC oscillators. Although [9] has addressed some of the shortcomings, it uses more than one off-chip component. In addition, it requires external power-reset-assisted switching to initiate the operation. In comparison, this work is a fully electrical self-start-up operating from sub-threshold input levels using only one off-chip component. Table I compares the proposed energy harvester with other state-of-the-art circuits. To be noted that this work has not dealt with output ripple regulation.

V. CONCLUSION

A low input voltage start-up technique for TEG-based energy harvesting circuits is proposed. The proposed technique utilizes the output voltage as feedback to generate a reset signal at sub-threshold input voltages, which improves the speed of the start-up circuit. The proposed harvester can boost the input voltage of 290mV up to 1V with the start-up time of 35µs. The start-up circuit is deactivated during the steady state for better conversion efficiency. The measured peak efficiency is 77% and the quiescent power of the start-up circuit is 3.2nW at 290mV during the steady state. The harvester does not require post-fabrication processing or native devices and uses only one off-chip component making it easily applicable to various ultra-low power applications such as portable electronics, wearable devices, etc.

REFERENCES