

An analogue video interface for general-purpose DSP

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Abstract

This paper presents a real-time, high speed interface for the capture of live analogue video for DSP based video processing applications. The interface makes use of the link ports, which are standard features of general-purpose digital signal processor (DSP). Hence the interface can be used for the different DSPs with minimum customisation. Current technologies for video processing are either based on application-specific integrated circuit (ASIC) or programmable processors specialised for video or video DSP as well as a hybrid of the above with a host computer. Such technologies come equip with software tools and application programming interfaces (APIs) to support a variety of common video processing tasks. Some of these may have support for analogue video interfaces while others simply cater only to digital video inputs/outputs. Unfortunately, the majority of video sources in daily life are analogue in nature. Video application designers are thus faced with the problem of finding a suitable simple analogue video interface for their applications. Moreover, for those designers who design their own video processing algorithms using general-purpose DSP to circumvent the cost and limitations imposed by these suites of standard solutions, the need for a simple analogue video interface is further underscored. The proposed interface thus serves to provide a simple, flexible, high speed and low-cost analogue interface to resolve the analogue video conversion problem and allow designers to concentrate on their DSP based applications. The interface can support both real-time and non real-time applications. © 2001 Elsevier Science B.V. All rights reserved.

Keywords: Analogue video interface; Video processing; DSP; Link ports

1. Introduction

Recent advances in VLSI technology, high-speed processor designs, Internet/Intranet applications, broadband networks such as ATM and ISDN and compression standards are leading to the popularity of multimedia applications. Video intensive multimedia systems are a large and growing segment of both the computing and the consumer electronics marketplace. Examples of such applications include video-on-demand system, video conferencing, interactive TV, distance learning, remote video monitoring, tele-medicine. Digital video processing is computationally intensive and requires high video data rate. In an attempt to capitalize on the emerging video market and gain widespread consumer acceptance, companies and research organizations are designing integrated circuits as well as

new and faster implementations for video algorithms with performance and cost which are acceptable to the market.

Currently, video processing technologies are based on video dedicated solutions, namely, application-specific integrated circuit (ASIC) [1,2] or programmable processors specialized for video [3,4] or video DSP [5,6] as well as a hybrid of the above with a host computer [7]. Others used general purpose DSP for their applications [8]. The video dedicated solutions usually possess a set of software tools and/or application programming interfaces (APIs) to support a variety of common video processing tasks. Most of these solutions work on digital video input and output with no interface to analogue video, assuming that conversion from analogue video has been done. Typically, only those vendors who provide board level solutions such as Ref. [7] have incorporated the analogue video interface. These board level solutions would require the use of a host computer. Unfortunately, the majority of video sources in daily life are analogue in nature (e.g. TV, VCR, CCTV etc). Thus there is a need to provide for an analogue video interface so that such video can be processed digitally. Moreover, for designers who design their own video

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algorithms on general purpose DSP to circumvent the cost and limitations imposed by these suites of standard solutions, the need for a simple analogue video interface is underscored.

The advantages of using a general purpose DSP is that it allows high computational performance at low cost. It is also highly flexible and can be easily reprogrammed for different applications. It can therefore also be a standalone product without the need for a host controller. However, like the other video processing solutions, the main drawback of using a general purpose DSP is that it lacks a dedicated high data rate video interface although they usually have multi-channel serial ports for glueless audio interfacing. There is also a variety of analogue to digital converters (A/D) called Analogue Interface Circuits (AIC) [9] to support such serial interface to the DSP. However, these AICs cannot meet the high data rate required of video signal.

Interfacing a DSP to analogue video requires precise clocking synchronization and large amount of bandwidth. The video sampling rate is at 13.5 MHz and the video samples have to be read at precise intervals otherwise pixels will be missed or displaced. Conventional input–output (I/O) interfacing will not work for such high data rate. The DSP using conventional I/O will have the address bus and data bus busy at all the active video intervals, leaving no time for any significant processing. This is because a memory read and write have to be performed in one video pixel clock cycle (13.5 MHz). It can only process the digital video during the horizontal and vertical flyback intervals and blanking intervals. The amount of time available for processing is only 25% of the total time available. This is clearly inefficient.

This paper will provide a simple and efficient interface technique for interfacing the analogue video to the DSP so as to free up the DSP host for other purposes. This is accomplished through the use of high speed link ports, which are standard features of most DSPs [10]. The feasibility of the proposed technique is proven through its integration with an Analog Device general purpose SHARC (Super Harvard Architecture Computer) 21062 DSP [11]. The interface is capable of capturing the live analogue video, converting digital video into its analogue form for display. The interface can be easily customised for the different DSPs and has been designed to cater to both real-time and non real-time video processing applications.

2. System design

The overall block diagram for the proposed interface is shown in Fig. 1. The analogue composite video interface A/D conversion is achieved by a video decoder SAA 7111 [12], while the video D/A conversion is implemented using a video encoder SAA 7185B [13]. The host DSP communicates with the video encoder and decoder through the I²C bus [14].

The digital video after the A/D conversion is a 16-bit YUV data according to CCIR 4:2:2 multiplexed format. The information has to be multiplexed and fed into the DSP via two 4-bit link ports. The link ports are double clocked to take in 2 nibble per pixel clock cycle. The digital video output from the DSP is also accomplished via the 4-bit link ports. They are recombined to form the 16-bit YUV data in the digital video output interface. The digital video is then converted into composite video using the SAA 7185B.

A power-on reset circuit resets the DSP, video decoder and video encoders. Upon reset, the DSP will fetch the instructions from the bootstrap ROM, built from a 1 Mbyte EPROM. It also interfaces with 8 Mbyte of high

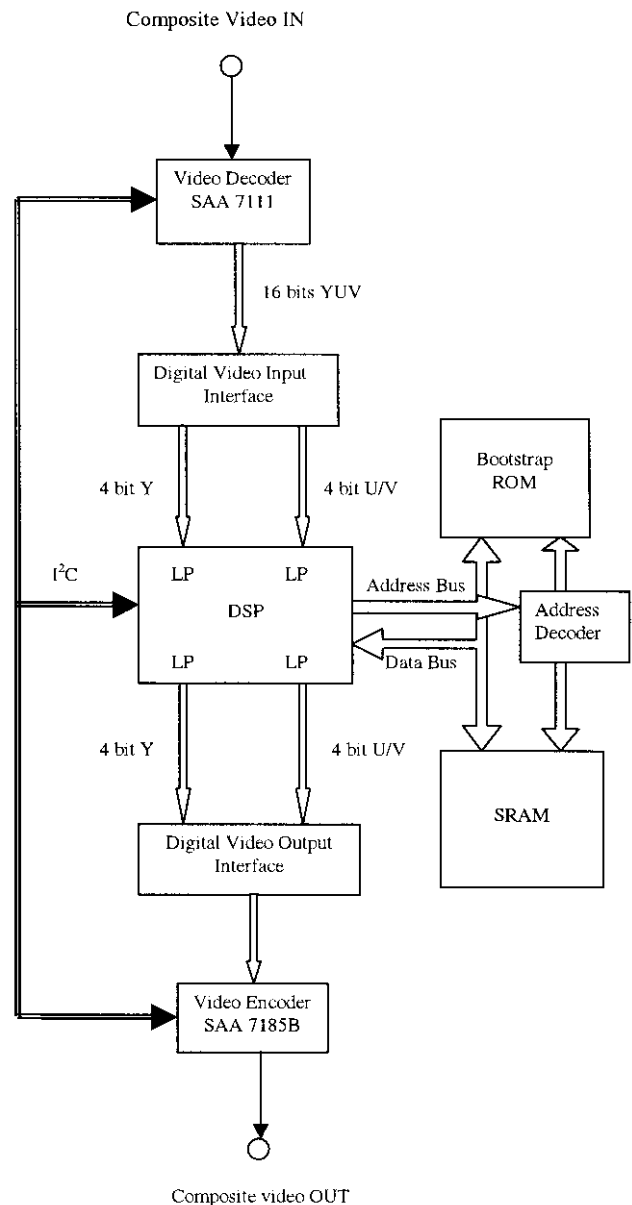


Fig. 1. System block diagram.

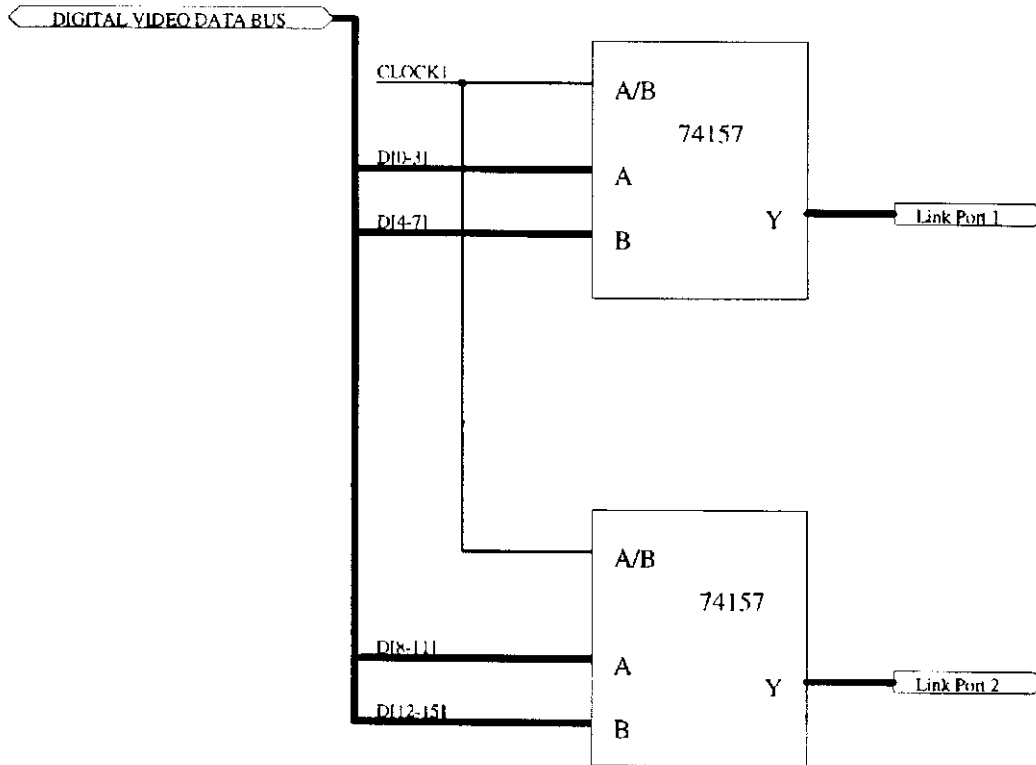


Fig. 2. Input video interface block diagram.

speed SRAM which is sufficient to store at least 10 video frames.

3. DSP

The ADSP-21062 SHARC is a high performance 32-bit DSP for speech, sound, graphics and imaging applications. It is popular among designers as it presents the best compromise between low cost and high performance. Hence it is used here to illustrate the feasibility of the proposed

analogue video interface. The DSP is a complete system on a single chip with dual ported on-chip SRAM and integrated I/O peripherals supported by a dedicated I/O bus. The high performance DSP core is integrated with a host processor interface, DMA controller, serial ports, link ports and shared bus connectivity for glueless DSP multi-processing.

It also has an on-chip instruction cache which allows the processor to execute every instruction in a single cycle. Four independent buses for dual data, instructions, I/O plus crossbar switch memory connections made up the SHARC

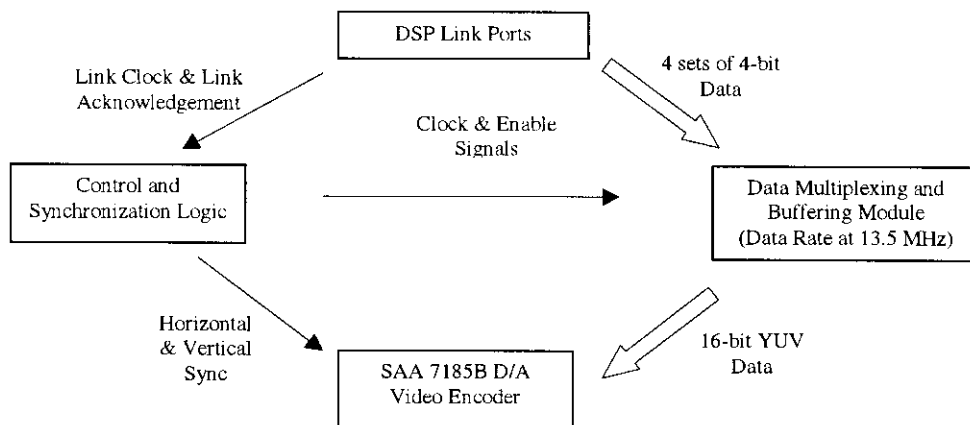


Fig. 3. Block diagram of the video output interface.

architecture. The DSP is operated with a clock speed of 40 MHz.

4. Video input interface

The analog video is digitized using the video input processor (VIP) SAA7111. The VIP is a highly integrated circuit which has an anti-aliasing filter, A/D converter, an automatic clamp and gain control, a clock generation circuit, a multi-standard decoder (PAL and NTSC), a brightness/contrast/saturation control circuit and a colour space matrix. It can convert PAL and NTSC signals into CCIR-601 compatible colour component values. It also accepts colour composite video or S-video (Y/C) format. The various options for this device can be programmed using the I²C bus. This renders it highly flexible as a software change is all that is needed to cater for the different video standards.

The digital output is programmed to be in 16 bit YUV format, which consists of 8 bits of Y component and 8 bits of U/V component, appearing at a frequency of 13.5 MHz. The link ports of ADSP-21062 are parallel ports with only

four data pins, an acknowledge pin and a clock pin. The data that is read in from the link port is stored in the link buffer, which is in turn read by the DSP.

Fig. 2 shows the digital video input interface. A minimum of two link ports (Link ports 1 and 2) are required to handle the data rate. Link port 1 is used for the 8-bit Y component while Link port 2 is used for the 8-bit U/V component. Since the link ports can take in only four bits at a time, the 8 bits (at 13.5 MHz frequency) have to be multiplexed into 2 cycles of 4 bits each to each link port at the rate of 27 MHz. The link ports latch the incoming data at the falling edge of the link port clock.

5. Video output interface

Fig. 3 shows the block diagram of the video output interface. It essentially comprises the DSP link ports, the data multiplexing and buffering module, the control and synchronization logic as well as the D/A video encoder. The processed digital video is output via Link ports 3 and 4 as shown in the detailed data multiplexing circuit in Fig. 4. Link port 3 handles the 8-bit Y data while Link port 4

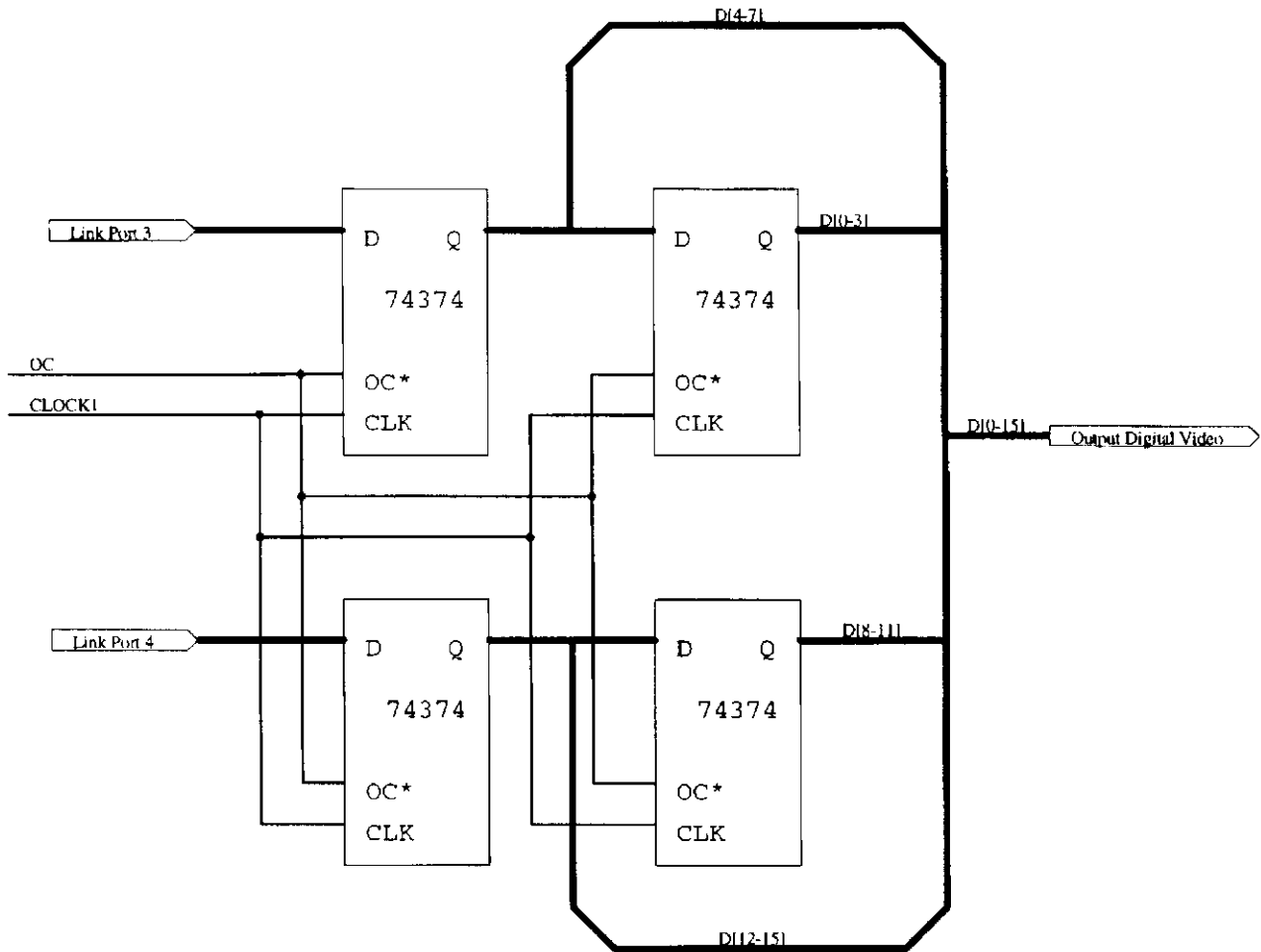


Fig. 4. Data multiplexing circuits for video output interface.

handles the U/V data. The link ports will send the most significant 4 bits first (D4–D7, D12–D15 shown in Fig. 4) followed by the least significant 4 bits (D0–D3, D8–D11 shown in Fig. 4) in two cycles. The four sets of nibbles are then buffered using double latches into a 16-bit YUV format. The 16-bit YUV data is the format required by the video encoder SAA 7185B for conversion to live video.

The control and synchronization logic ensures that data flow to the buffer and the encoder is regulated and is also responsible for video synchronization at the encoder. Enable and clock signals derived from the acknowledge and clock pins of the DSP link ports serve to control the data multiplexing and buffering module to ensure proper ordering and packing of the data.

The vertical and the horizontal video synchronization signals for frame and line synchronization, respectively, are provided by a free running, video sync generator, the Fairchild 74ACT715 [15]. In fact, the video sync signals can actually be extracted from the live video inputs at the video input interface. This is the most economical solution as it can dispense with the additional IC. This approach requires the availability of live video at the input, which is the case for real-time video processing. For non real-time applications where processed digital video may only be output after some delay and without live video input, an alternative video sync source has to be provided. Therefore, in the proposed analogue interface design, the provision of the 74ACT715 is to cater to both real-time as well as non real-time applications.

6. Memory interface

The ADSP-21062 can be booted up during power-on reset from an 8-bit EPROM. The 8-bit data are transferred over bits D16 to D23 of the data bus. A 1-Mbyte EPROM is constructed from four 27C201K EPROMs.

The 8-Mbyte main memory is constructed using 5-ns access time SRAM and arranged in 32-bit wide format and they are connected to the DSP data bus bits from D16 to D47. The address decoder is constructed using logic gates and 3 to 8 line decoders to keep costs down.

7. Evaluation

The proposed analogue video interfacing technique is tested on a popular and typical general purpose DSP, the Analog Devices ADSP-21062. To demonstrate the analogue video input interface, live video is captured from a camera, digitised and stored in memory using the link ports of the DSP. The DSP is able to keep up with the video data rate of 13.5 Mbytes per second in real-time. This is verified by reading in the digitised video data from the memory and directing the video stream to a monitor through the video output interface. The video output interface does the D/A

conversion. The monitor is able to track the camera input in real-time.

The proposed interface is targeted to support video processing designers who are building applications on general purpose DSPs. The designers can easily integrate the interface with the DSP through the DSP link ports without compromising the computational performance of their processors. The interface fills the void left by market products for the DSP. To better appreciate the merits of the proposed interface, a comparison is made with commercially related products. The four factors used in the comparison are namely, ability to support real time video rate, ability to provide analogue to digital video conversion and vice versa, ease of interface to DSP as well as the utility value.

Existing analogue interface products for video applications can be classified as chip level or board level.

7.1. Chip level products

Two families of chip level products can be identified, namely, the A/D and D/A converters exemplified by Texas Instrument's Analogue Interface chips for DSP [9] and the video DSP chips such as the Oxford Micro Devices' video DSP chip [6]. The former is simply a general purpose A/D and D/A converter (ADC/DAC) which can support analogue video conversion data rate. The former can be interfaced directly to the DSP via the DSP's serial links but such links are unable to support video data rate. The latter is dedicated for video processing with buffered parallel ports for connection to external video encoder and decoder chips. It usually provides for parallel ports to host computer and can thus be linked to a DSP indirectly. However, designers using this type of chips just for analogue video conversion is not fully utilizing its main functions and is thus not cost effective.

7.2. Board level products

Board level products can be classified broadly as the video framegrabber family as typified by Ref. [16] and the integrated video processing boards, examples of which are the Krell's product [7] and the Tranquair's module [17]. These board level products need to be incorporated into host computers and thus the interface is based on local bus standards such as the PCI bus. Video framegrabber essentially captures the analogue video in real time, digitizes it and stores them onboard its video RAM. The data can then be transferred to the host computer. Video framegrabber, however, only supports one-way conversion for analogue video as its primary function is to provide the digitised video data for host computer processing. Hence, to use it for DSP applications will require an indirect link via the host computer as well as to perform the D/A conversion for the digital video.

Integrated video processing boards are much more sophisticated than video framegrabber. It integrates video

Table 1
Summary of comparison results

	Chip-level		Board-level		Proposed video interface
	ADC/DAC	Video DSP chip	Video framegrabber	Video processing board	
Real time video rate	Compromised	Yes	Yes	Yes	Yes
Video capture and display	Yes	Yes	No	Yes	Yes
Ease of interface to DSP	Direct serial link to DSP	Indirect link to DSP via host computer	Indirect link to DSP via host computer	Indirect link to DSP via host computer	Direct link to DSP via link ports
Utility value	Maximum	Low	Constrained	Low	Maximum

capture with a host of video processing functions. Similarly, they require the use of host computers/host processors and cannot interface directly to a general purpose DSP.

7.3. Comparison results

Table 1 summarises the comparison results of the proposed analogue interface with the different related products based on the four factors stated.

7.3.1. Support for real time video rate

All products are specially designed to support real time video rate conversion. This is essential for the capturing of the live analogue video data as well as for displaying the converted digital video signal in real-time. However the ADC/DAC's support for real time video rate is compromised when it is interfaced to the DSP via its serial port as the serial port is too slow to support the video data rate.

7.3.2. Video capture and display

This factor refers to the ability to support both the capture and the display of analogue video. All products except for the video framegrabber have incorporated both the ADC and DAC to perform two-way video conversions. The video framegrabber, however, is used for digitising and storing the digital video for onward host processing. It does not support real-time conversion of digital to analogue video for display.

7.3.3. Ease of interface to DSP

This is an important performance parameter as the sole purpose of the proposed analogue video interface is to provide a simple and efficient means of capturing and displaying video in real-time for DSP processing. ADC/DAC is designed to be linked to the DSP directly via the serial ports. The only disadvantage is that the serial port is too slow to support the video rate transfer. Other chip and board level products are designed to be linked to host computers via parallel ports or PCI local bus. This means that to interface them to a DSP will require an indirect link through the host computer. This is cumbersome. As for the

proposed interface, direct links to the DSP are provided by way of the link ports.

7.3.4. Utility value

As it is not possible to directly compare the cost of the different categories of related products, the utility value is used instead. A high utility value means the product has fulfilled the needs of the particular application that it is used for while a low utility value means that the product has more features than is needed by the application. The latter implies that there are superfluous features, which are not utilised in the application, which will therefore translate to a higher cost incurred for the application. The ADC/DAC as well as the proposed interface are both maximally utilised for the two-way analogue video conversion for DSP application. As for the video DSP chips and the video processing boards, they are under-utilised as these are highly integrated products bundled with general video processing functions. To use them just for their analogue video interface is an overkill. The video framegrabber has a constrained utility value since it is unable to perform the D/A conversion.

7.4. Summary

From Table 1, it can be seen that the proposed analogue interface technique is not only able to link directly with the DSP but also able to achieve the required high data rate for video. There are also no superfluous functions, which will incur additional cost unlike the use of the video DSP chips or video processing boards. In addition, the proposed analogue video interface is flexible enough to perform both video capture and display as well as simple enough to be interfaced to any general purpose DSP. There is no necessity for host computer intervention. Therefore, the proposed interfacing technique provides DSP video designers with a simple, efficient and lean means of analogue video conversion.

8. Conclusion

This paper presented an interfacing technique for

analogue video I/O for general-purpose DSP. The interface makes use of the link ports of the DSPs to carry out the high data rate video transfer. It can support both real-time and non real-time applications on the DSP.

The interface bridges the gap left by current video interface solutions through providing both input and output for analogue video using a simple, lean and direct interface to the DSP. All these are achieved without the need for any third party interconnection such as a host computer and at the required high video data rate without compromising the computational performance of the DSP.

References

- [1] P. Pirsch, H.J. Stalberg, VLSI implementation of image and video multimedia processing systems, *IEEE Transactions on Circuits and Systems for Video Technology* 8 (7) (1998) 878–891.
- [2] E.G.T. Jaspers, P.H.N. de With, G.W.M. Janssen, A flexible heterogeneous video processor system for television applications, *IEEE Transactions on Consumer Electronics* 45 (1) (1999) 1–12.
- [3] A.Y. Wu, K.J. Ray Liu, A. Raghupathy, System architecture of an adaptive reconfigurable DSP computing engine, *IEEE Transactions on Circuits and Systems for Video Technology* 8 (1) (1998) 54–73.
- [4] M.Y. Siyal, M. Fathy, A programmable image processor for real-time image processing applications, *Microprocessors and Microsystems* 23 (1999) 35–41.
- [5] TMS320C80 Multimedia Video Processor, Texas Instrument, <http://www.ti.com>.
- [6] A236 Parallel Video DSP Chip, Oxford Micro Devices, Inc, <http://www.oxfordmicrodevices.com/tech796.html>.
- [7] Krell Multimedia Video Digital Signal Processor (MV-DSP) PCI Board, Light Science Technologies Inc, <http://www.lightscience.com/products/mvDSP.html>.
- [8] Y. Naito, I. Kuroda, Mobile video codec based on a low power consumption DSP, *IEEE International Conference on Acoustics, Speech and Signal Processing*, vol. 5, 1998, pp. 3041–3044.
- [9] TLC320AD56 DSP Analog Interface, Texas Instrument, <http://www.ti.com>.
- [10] Introduction to DSP processors: Input and output interface, http://www.bores.com/courses/intro/chips/6_io.htm.
- [11] ADSP-2106x SHARC, DSP Microcomputer Family, Analog Devices.
- [12] Video Input Processor SAA7111, Philips Semiconductors Product Specification.
- [13] Digital Video Encoder SAA7185B, Philips Semiconductors Product Specification.
- [14] Inter-Integrated Circuit (I2C) Bus Standards, Philips Corporation.
- [15] ACT715, Programmable Video Sync Generator, Fairchild Semiconductors Product Specification.
- [16] FlashBus MVPlus-Video Frame Grabber for PCI Bus, Integral Technologies, <http://www.ehd.de>.
- [17] HETVIO2 8-bit Video Frame Capture/Display, Traquair Data Systems, <http://www.traquair.com/catalog/family/tim>.



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