

ISMVL 2006. Accepted papers

Title: Arithmetic-Haar spectral transform decision diagrams
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Title: Properties of matrix-valued spectral coefficients with the Fourier Transform on a non-Abelian group
Authors: C. Moraga, R. Stankovic, J. Astola
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Title: On the range of algebraic functions on lattices. A preliminary report.
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Title: Generation and Relation of Quaternary and Binary Linearly Independent Transforms
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Title: Representation of elementary functions using decision diagrams
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Title: Efficiency of multiple-valued encoding in SAT-based ATPG
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Title: Multi-Valued Quantum Logic
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Title: Random multiple-valued networks: Theory and applications
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Title: Implementation of multiple-valued CAM functions with LUT cascades
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Title: On Designs of Radix Converters Using Arithmetic Decompositions
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Title: A quaternary half-adder using current mode operation with bipolar transistors
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Title: New data encoding method with a multiple-valued logic for low power asynchronous circuit design
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Title: The new architecture for radix-4 Chinese abacus
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Title: Switch block architecture for multi-context FPGAs using hybrid multiple-valued/binary context switching signals
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Title: Commuting hyperoperations
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Title: Completeness of a hypersequent calculus for some first-order Gödel logic with delta.
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Title: Investigation of multi-state system reliability depending on changes of some system component states
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Title: A quantum CAD accelerator based on Grover's algorithm for finding the minimum fixed polarity Reed Muller form
Author(s): Lun Li, M. Thornton, M. Perkowski
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Title: Theoretical basis of commutation theory for partial clones
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Title: A novel balanced ternary adder using recharged semi-floating gate devices
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Title: Highly reliable multiple-valued circuit based on dual-rail differential logic
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Title: A High-Density Ternary Content-Addressable Memory Using Single-Electron Transistors
Author(s): Katsuhiko Degawa, Takafumi Aoki, Tatsuo Higuchi, Hiroshi Inokawa, Katsuhiko Nishiguchi and Yasuo Takahashi.
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Title: Embedding and assembling technique for spatial computing structure design using decision trees and diagrams
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Title: Associativity test in hypergrupoids
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Title: Fine-grain cell design for multiple-valued reconfigurable VLSI using a single differential-pair circuit
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Title: Evaluation of multiple-valued packet multiplexing scheme for network-on-chip architecture
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Title: Algorithm level interpretation of fast adder structures in binary and multiple-valued logic
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Title: Towards solving many-valued maxSAT
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Title: Design of a microprocessor datapath using four-valued differential-pair circuits
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Title: A feedback-signal shaping technique for multi-level continuous-time delta-sigma modulators with clock-jitter
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Title: QMDD: A decision diagram structure for reversible and quantum circuits
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Title: Some observations on minimal clones
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Title: Assumption based multiple-valued semantics for extended logic programs
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Title: Upper and lower bounds on the number of disjunctive forms
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