

ISMVL-2006 Program

| Date | Activities | | | |
|-----------------------------|--|---|---|---|
| Wed, 17 May 2006 | ULSI Workshop 10.30 – 16.45 Coffee break | | | ISMVL Welcome Reception 18.00 – 20.00 |
| Thu, 18 May 2006 | Opening Address 8.50 – 9.00 Invited Address 9.00 – 10.00 Coffee break | Session 2: Circuits I 10.10 – 12.00 Lunch | Session 3: Algebra and Logic 13.30 – 14.50 Coffee break | Session 4: Circuits II 15.00 – 16.50 |
| Fri, 19 May 2006 | Session 5: Invited Address 9.00 – 10.00 Coffee break | Session 6: Circuits III 10.10 – 12.00 Lunch | Session 7: Algebra and Clones 13.30 – 14.50 Coffee break | Session 8: Systems and Satisfiability 15.00 – 16.00 City tour and Banquet |
| Sat, 20 May 2006 | Plenary Session 9.00 – 10.00 Coffee break | Session 9: Decision Diagrams and Decision Trees 10.10 – 11.30 | Session 10: Quantum Logic and Spectral Techniques 11.30 – 12.30 | |

15th International Workshop on Post-Binary ULSI Systems
May 17, 2006, Nanyang Technological University, Singapore

Program

10:30-10:35 Opening Remark

ULSIWS Chair, Tetsuya Uemura, Hokkaido University, Japan

Session 1: New-Paradigm VLSI Circuits and Systems I

10:35 – 11:50

Fine-Grained Architectures for Field-Programmable VLSIs

Masanori Hariyama and Michitaka Kameyama (Tohoku University, Japan)

Properties and Hardware Implementation of New Fastest Linearly Independent Ternary Arithmetic Transforms

Cicilia C. Lozano, Bogdan J. Falkowski (Nanyang Tech. Univ., Singapore)

Susanto Rahardja (Institute for Infocomm Research, Singapore)

A Study on Equalization Techniques for Multiple-Valued Data Transmission

Yasushi Yuminaka (Gunma University, Japan)

Session 2: Fuzzy, Immunological and Quantum controlled Robots

1:30 - 2:45

Artificial Immune-Neuro-Fuzzy System to control a walking robot Hexor

Dong Hwa Kim (Hanbat National University, Korea)

Christopher Brawn (Portland State University, USA)

Maciej Sajkowski (Silesian University of Technology, USA)

Tomasz Stenzel (Stenzel Company, USA)

Tsutomu Sasao (Kyushu Institute of Technology, Japan)

*Jeff Allen, Martin Lukac, Tzewen Wang, and Marek Perkowski
(Portland State University, USA)*

Hexor, a Walking and Talking Robot with Quantum and Fuzzy Inference

Christopher Brawn, Natalie Metzger, Jake Biamonte, Martin Lukac, Akashdeep Aulakh,

Indudhar Devanath (Portland State University, USA)

Maciej Sajkowski, Tomasz Stenzel (Silesian University of Technology, USA)

Dong Hwa Kim (Hanbat National University, Korea)

Tsutomu Sasao (Kyushu Institute of Technology, Japan)

Marek Perkowski (Portland State University, USA)

The Vagueness of Robot Emotions

Phil Serchuk, Ehud Sharlin (University of Calgary, Canada)

Martin Lukac, Marek Perkowski (Portland State University, USA)

2:45 - 3:05 Break

Session 3: Invited Session

3:05 – 3:45

Novel Quantum Nanodevice-based Logic Circuits utilizing Semiconductor Nanowire Networks and Hexagonal BDD Architecture

Seiya Kasai (Hokkaido University, Japan)

Session 4: New-Paradigm VLSI Circuits and Systems II

3:45 - 4:35

Recharged Comparator and Multiple-Valued N-ary Frequency Divider

Rene Jensen, Henning Gundersen, Johannes G. Lomsdalen and Yngvar Berg

(University of Oslo, Norway)

Design and Analysis for Magnetic Random Access Memory based on Magnetic Tunnel Junction and Tunnel Diode

Tetsuya Uemura and Masafumi Yamamoto (Hokkaido University, Japan)

4:35 Closing

May 17, 2005

Welcome reception: 6.00 pm – 8.00 pm

May 18, 2005

Opening address: 8.50 am -9.00 am

Session 1: Invited Address (Chair: B. Falkowski)

9.00 am – 10.00 am

Design Methods for Multiple-Valued Input Address Generators

T. Sasao

Coffee break

Session 2: Circuits I (Chair: Y. Yuminaka)

10.10 am – 12.00 pm

Algorithm Level Interpretation of Fast Adder Structures in Binary and Multiple-Valued Logic

N. Homma, T. Aoki, and T. Higuchi

On Designs of Radix Converters using Arithmetic Decompositions

Y. Iguchi, T. Sasao, and M. Matsuura

New Data Encoding Method with a Multiple-Valued Logic for Low Power Asynchronous Circuit Design

E. J. Choi, J. H. Lee, and K. R. Cho

Highly Reliable Multiple-Valued Circuit Based on Dual-Rail Differential Logic

A. Mochizuki and T. Hanyu

Evaluation of Multiple-Valued Packet Multiplexing Scheme for Network-on-Chip Architecture

H. M. Munirul, T. Hasegawa, and M. Kameyama

Lunch

Session 3: Algebra and Logic (Chair: H. Machida)

1.30 pm - 2.50 pm

On the Range of Algebraic Functions on Lattices - A Preliminary Report

S. Rudeanu and D. Simovici

Upper and Lower Bounds on the Number of Disjunctive Forms

H. Tatsumi, M. Miyakawa, and M. Mukaidono

Completeness of a Hypersequent Calculus for Some First-Order Gödel Logic with Delta

M. Baaz, N. Preining, and R. Zach

Assumption Based Multiple-Valued Semantics for Extended Logic Programs

D. Stamate

Coffee break

Session 4: Circuits II (Chair: T. Waho)

3.00 pm – 4.50 pm

Implementation of Multiple-Valued CAM Functions with LUT Cascades

T. Sasao and J. Butler

The New Architecture for Radix-4 Chinese Abacus

S.-C. Yi, K.-T. Lee, J.-J. Chen, C.-H. Lin, C.-C. Wang, C.-F. Hsieh, C.-Y. Lu

Fine-Grain Cell Design for Multiple-Valued Reconfigurable VLSI Using a Single Differential-Pair Circuit

H. M. Munirul and M. Kameyama

Design of a Microprocessor Datapath Using Four-Valued Differential-Pair Circuits

A. Mochizuki, T. Kitamura, H. Shirahama, and T. Hanyu

A Quaternary Half-Adder Using Current Mode Operation with Bipolar Transistors

C. R. Mingoto

May 19, 2005

Session 5: Invited Address (Chair: R. Drechsler)

9.00 am – 10.00 am

Signal Processing Algorithms and Multiple-Valued Logic Design Methods

J. Astola

Coffee break

Session 6: Circuits III (Chair: M. Kameyama)

10.10 am – 12.00 pm

Switch Block Architecture for Multi-Context FPGAs Using Hybrid Multiple-Valued/Binary Context Switching Signals

Y. Nakatani, M. Hariyama, and M. Kameyama

A Novel Balanced Ternary Adder Using Recharged Semi-Floating Gate Devices

H. Gundersen and Y. Berg

A High-Density Ternary Content-Addressable Memory Using Single-Electron Transistors

K. Degawa, T. Aoki, T. Higuchi, H. Inokawa, K. Nishiguchi, and Y. Takahashi

A Feedback-Signal Shaping Technique for Multi-Level Continuous-Time Delta-Sigma Modulators with Clock-Jitter

M. Tanihata and T. Waho

Lunch

Session 7: Algebra and Clones (Chair: D. Simovici)

1.30 pm - 2.50 pm

Commuting Hyperoperations

J. Pantović and G. Vojvodić

Theoretical Basis of Commutation Theory for Partial Clones

L. Haddad, H. Machida, and I. Rosenberg

Associativity Test in Hypergrupoids

I. Rosenberg, M. Miyakawa, and H. Tatsumi

Some Observations on Minimal Clones

H. Machida and M. Pinsker

Coffee break

Session 8: Systems and Satisfiability (Chair: S. Yanushkevich)

3.00 pm – 4.00 pm

Efficiency and Multiple-Valued Encoding in SAT-Based ATPG

G. Fey, J. Shi, and R. Drechsler

Towards Solving Many-Valued MaxSAT

J. Argelich, X. Domingo, C.-M. Li, F. Manyà, and J. Planes

Multi-Valued Quantum Logic

Michael Katz

Random Multiple-Valued Networks: Theory and Applications

E. Dubrova

Investigation of Multi-State System Reliability Depending on Changes of Some System Component States

E. Zaitseva, and S. Puuronen

Take bus to the city for city tour and banquet – 4 pm

May 20, 2005

Plenary Session

9.00 am – 10.00 am

Coffee break

Session 9: Decision Diagrams and Decision Trees (Chair: T. Sasao)

10.10 am – 11.30 am

Representation of Elementary Functions using Decision Diagrams

T. Sasao and S. Nagayama

Embedding and Assembling Technique for Spatial Computing Structure Design using Decision Trees and Diagrams

S. Yanushkevich, O. R. Boulanov, and V. Shmerko

QMDD: A Decision Diagram Structure for Reversible and Quantum Circuits

D. M. Miller and M. Thornton

Arithmetic-Haar Spectral Transform Decision Diagrams

B. J. Falkowski and S. Yan

Session 10: Quantum Logic and Spectral Techniques (Chair: M. Miller)

11.30 am – 12.30 pm

A Quantum CAD Accelerator Based on Grover's Algorithm for Finding the Minimum Fixed Polarity Reed-Muller Form

L. Li, M. Thornton, and M. Perkowski

Generation and Relation of Quaternary and Binary Linearly Independent Transforms

B. J. Falkowski and C. Fu

Properties of Matrix-Valued Spectral Coefficients with the Fourier Transform on a Non-Abelian Group

C. Moraga, R. Stanković, and J. Astola