



Institute of Electrical and
Electronics Engineers



IEEE Computer
Society



TC on
Multiple-
Valued Logic



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36th International Symposium on Multiple-Valued Logic

Nanyang Technological University, Singapore
May 17-20, 2006

CALL FOR PAPERS

The Multiple-Valued Logic Technical Committee of the IEEE Computer Society will hold its 36th annual symposium on May 17-20, 2006 in Nanyang Technological University, Singapore.

The event is sponsored by the IEEE Computer Society, Nanyang Technological University, and Singapore Tourism Board.

You are invited to submit an original paper, survey or tutorial paper on any subject in the area of multiple-valued logic, including but not limited to:

Algebra and Formal Aspects
Automatic Reasoning
Communication Systems
Data Mining
Image Processing
Logic Programming
Nano Technology
Quantum Computing
Spectral Techniques

ATPG and SAT
Circuit/Device Implementation
Computer Arithmetic
Fuzzy Logic and Soft Computing
Logic Design and Switching Theory
Machine Learning and Robotics
Philosophical Aspects
Signal Processing
Verification

Authors should submit papers by **November 1, 2005** to:

Dr. Claudio Moraga, Program Chair

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Electronic submissions by PDF or PS files are strongly preferred. In exceptional cases, submissions of four (double-spaced typed) paper copies are also acceptable. Each manuscript should include a 50-100 word abstract and should not exceed 6 pages in the proceedings format.

Authors will be notified about acceptance by **February 1, 2006**.

Photo-ready copies of accepted papers are due on **March 1, 2006**.

For additional information contact:

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The symposium will be preceded by the Post Binary ULSI Workshop on May 17, 2006.