A Low-Power 24-GHz Frequency Synthesizer for Automotive Radar Application

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Abstract—We proposed a 24-GHz frequency synthesizer (FS) for automotive radar application, which consists of a phase-locked loop (PLL) and an injection-locked frequency multiplier (ILFM). Based on a novel topology, the multiply-by-2 ILFM consists of a double-balanced mixer and an injection-locked oscillator (ILO). The PLL is designed with a 12-GHz voltage-controlled oscillator (VCO) and an injection-locked frequency divider (ILFD) on a stacking topology. The proposed FS is designed and simulated in 130 nm CMOS technology. With a power supply of 1.5 V, it has the power consumption of 9.3 mW and the phase noise of -104 dBc/Hz at 1 MHz offset.

Keywords—RF CMOS, injection-locked frequency multiplier (ILFM), Phase-locked Loop (PLL), 24-GHz application, stacking topology

I. INTRODUCTION

Automotive collision warning radar (ACWR) is a key equipment in the advanced vehicle safety system, which is one of the main issues in the intelligent transportation system (ITS) [1]. In previous study, several frequency bands, such as 10, 24, 77, and 94 GHz, have been used for automotive radar applications [2][3][4]. Among these frequency bands, 10 GHz have much longer wavelength, which limits the design of a high-directivity antenna in size. Conversely, the wavelengths in the frequency of 77 and 94 GHz are much shorter. Thus, the devices and fabrication cost for the applications are extremely high. Therefore, the wavelength in 24 GHz is good for high-directivity antenna array design within a reasonable size. Moreover, the fabrication cost of the CMOS process for the 24 GHz is acceptable in market.

In the 24-GHz ACWR, the frequency synthesizer (FS) is a key building block to generate the reference signal at 24 GHz. In the conventional FS, the desired frequency of 24 GHz is generated from the voltage-controlled oscillator (VCO) in a phase-locked loop (PLL), so the operating frequency of the VCO is normally the highest frequency in the FS. Typically, it is necessary of large bias current for the good performance of the active and passive devices in the high-frequency VCO. Also, the first frequency divider (FD) is operating at the highest frequency because of its input signal directly from the VCO. Thus, an injection-locked frequency divider (ILFD) is used for high-frequency operation because of its relatively low power consumption. Both blocks always dominate the total power consumption of the FS.

For further improvement of the FS, a novel structure is composed of a low-frequency PLL cascaded with a frequency multiplier (FM). In this structure, the PLL generates a signal at the sub-harmonic of the desired reference frequency. Due to lower operating frequency, it has lower power dissipation from the VCO and the first FD. Subsequently, the FM generates the reference frequency driven by the output frequency of the PLL. However, it is difficult to design the FM. In [5]-[6], the design exploited the nonlinearity of active devices to generate harmonic of the input signal. However, due to its single input and output, the design of FM could not be used for the applications with differential input and output. In [7], an up-conversion mixer was used to generate the second harmonic as the output of the FM. The solution could be used for differential input and output applications, but both the designs require high-quality filters and suffer from low conversion gain. To improve the capability of driving the next stage, amplifiers would be used to increase the swing of their output signals. Consequently, the total power consumption for the FM is unavoidably increased due to a high-gain amplifier. Thus, a low-power and high-gain FM is a key issue in the FS structure.

In this paper, we proposed a 24-GHz FS using for automotive radar application. The proposed FS consists of a 12-GHz PLL and an injection-locked frequency multiplier (ILFM), which has the multiplier of 2. Based on a novel topology, the ILFM has low power consumption and large output swing for the next stage. In the PLL, a novel block of VCO-ILFD is used instead of both blocks of VCO and ILFD. Based on a stacking topology, the bias current of the VCO can be reused by the ILFD. With voltage redistribution and proper design, the total power consumption can be largely reduced with similar performance. In Section II, the proposed architecture of the FS is firstly introduced. Then, the two novel blocks, ILFM and VCO-ILFD, are described in detail. In Section III, the simulation results are shown. Comparing with previous works, a conclusion is drawn.

II. CIRCUIT DESIGN

A. Architecture of the proposed FS

![Figure 1. Architecture of the proposed FS.](image-url)

The architecture of the proposed FS is shown in Fig. 1, which consists of ILFM, VCO-ILFD, divide-by-512 FD, phase-frequency detector (PFD), charge pump (CP) and low-frequency generator.
pass filter (LPF). The reference frequency \( f_{\text{ref}} \) of 11.72 MHz is fed from the external signal generator. The VCO-ILFD's output frequencies \( f_{\text{PLL}} \) and \( f_{\text{div}} \) are designed as 12 GHz and 6 GHz, respectively. To compare with \( f_{\text{ref}} \), the feedback frequency \( f_{\text{FB}} \) is generated from the divide-by-512 FD, which consists of a series of true single-phase clock (TSPC) FDs.

The output frequency \( f_{\text{out}} \) of the proposed FS is generated from the ILFM, where \( f_{\text{PLL}} \) is multiplied by 2. In this FS, the multiplier of 2 is used for its optimized performance, such as the phase noise and operation range. With smaller multiplier, the ILFM would have lower phase noise and wider operation range.

B. Topology and schematic of the proposed \( \times 2 \) ILFM

The new topology of the \( \times 2 \) ILFM, shown in Fig. 2 (a), consists of a frequency pre-generator and an injection-locked oscillator (ILO). The frequency pre-generator is build by a up-conversion mixer, which has two inputs both connecting to the output signal of the PLL at \( f_{\text{PLL}} \). Subsequently, an injection current \( i_{\text{inj}} \) is generated at \( 2f_{\text{PLL}} \) and injected into the ILO. The ILO is built based on a positive feedback loop, which consist of an impedances \( H(\omega) \) and a transconductance \( G_m \). With the proper injection signal, \( f_{\text{out}} \) of the ILO is equal to \( 2f_{\text{PLL}} \).

Based on the new topology, the schematic of the \( \times 2 \) ILFM is designed and shown in Fig. 2(b). In the proposed ILFM, the mixer based on a double-balanced Gilbert cell is used as the frequency pre-generator. The differential inputs \( v_{\text{PLL}+} \) and \( v_{\text{PLL}-} \) are connected to six NMOS transistors \( M_{n1} \) to \( M_{n6} \). The differential injection currents \( i_{\text{inj}+} \) and \( i_{\text{inj}-} \) are generated with different harmonics of the input.

The ILO is designed based on a complementary LC-tank oscillator, which has larger output amplitude than a oscillator based on nMOS-only structure with same bias current [8]. If the oscillator’s resonant frequency \( f_0 \) is close to \( 2f_{\text{PLL}} \), other harmonics and inter-modulations in the injection current are filtered out by the LC tank. Therefore, it can be assumed that the injection frequency \( f_{\text{inj}} \) is equal to \( 2f_{\text{PLL}} \). Due to injection-locked by the injection signal, \( f_{\text{out}} \) is exactly equal to \( 2f_{\text{PLL}} \). The ILO is used to amplify the injection signal with high voltage gain for driving its next block, such as output buffer or mixer. In addition, there are two more dc voltages \( V_B \) and \( V_{\text{tune}} \). \( V_B \) is used to bias the ILO at oscillation. \( V_{\text{tune}} \) is connected to a varactor in the ILO, which is used to tune \( f_0 \) by changing the capacitance of the ILO’s LC-tank and further to extend the operation range of the ILFM.

C. Schematic of the proposed VCO-ILFD

Based on a stacking topology, the schematic of the VCO-ILFD is shown in Fig. 3, which consists of a VCO and an ILFD. The VCO is based on complementary structure, which output frequencies \( f_{\text{PLL}} \) is for the ILFM. Moreover, the ILFD is based on NMOS-only structure, where \( f_{\text{div}} \) is generated for the divide-by-512 FD. A large fixed capacitor \( C_m \) is connected from the head of the ILFD to \( \text{gnd} \). It is used to decouple the ac signal and to attenuate the voltage variation on this point.

Two varactors \( C_{\text{var1}} \) and \( C_{\text{var2}} \) are in the VCO and ILFD, respectively, and also tuned by \( V_{\text{tune}} \). Thus, the operation range of the ILFD is always shift with \( f_{\text{FB}} \). The ILFD is injection-locked by the VCO’s differential signal at the gates of NMOS and PMOS injection transistors, \( M_{n6} \) and \( M_{p6} \). Based on Adler’s locking range equation in [9], differential injection is used to widen the operation range of the ILFD. Moreover, the output impedance of the VCO can be made more balanced by differential injection.

D. Schematic of the divide-by-512 FD, PDF and CP
The divide-by-512 FD consists of a series of 9 TSPC FDs, shown in Fig. 4. The TSPC dynamic CMOS circuit is used in designing synchronous circuits to reduce circuit complexity, increase operating speed, and reduce power dissipation [10]. Moreover, it is operated with one input signal to avoid clock skew problems. Its input frequency is $f_{\text{div}}$ from the VCO-ILFD, which is normally around 6 GHz.

**Figure 5.** Simplified schematic of the PFD.

The schematic of the PFD is shown in Fig. 5 [11]. The TSPC dynamic D-FF is used for low frequency operation. A NOR gate with delay is used for reducing the dead-zone problem. Moreover, complementary pass-transistor gates are used to match the delay of an inverter in the output of PFD. Thus, the skew between the complementary outputs can be reduced.

**Figure 6.** Simplified schematic of the CP.

The function of the CP is to sink or source a current to a LPF. The schematic of the balanced charge pump is shown in Fig. 6. The CP has two pairs of differential inputs and a single-ended output. The input signals from the phase frequency detectors are designated as ‘UP’, ‘UPB’, ‘DN’ and ‘DNB’, respectively. The ‘UP’ and ‘UPB’ signals are connected to a pair of NMOS transistors as well as the ‘DN’ and ‘DNB’ signals are connected to a pair of PMOS transistors. In this circuit, the input differential pairs steer current either to a dummy load or into the current-controlled transistor. The signal paths from the input to the charge pump output can be optimized to be equal for the both up and down signals. Thus, the CP can be designed in balance.

### III. Simulation Results

The proposed FS is designed and simulated in 0.13 µm CMOS process. The power consumption of the proposed FS is 9.3 mW at a power supply of 1.5 V, where the PLL and the ILFM consume 5.25 mW and 4.05 mW, respectively. Due to two parts of the whole FS, it is important that $f_{\text{PLL}}$ is always in the operation range of the ILFM, where the ILFM is always at injection locking. The tuning characteristics of the PLL and ILFM is shown in Fig. 7. With $V_{\text{tune}}$ from 0 to 1.5 V, $f_{\text{PLL}}$ is tuned from 11.2 GHz to 13.1 GHz while the resonant frequency of the ILFM, $f_{\text{ILFM,0}}$ is also tuned from 22.8 GHz to 25.8 GHz, which is always close to $2f_{\text{PLL}}$. When the operation range of the ILFM is enough large, $f_{\text{out}}$ is always twice of $f_{\text{PLL}}$.

In Fig. 8, it is shown that the operation range of the ILFM is increased by decreasing the ILFM’s current consumption $I_{\text{ILFM}}$. However, the output power of the ILFM is reduced by decreasing $I_{\text{ILFM}}$. In the proposed circuit, $I_{\text{ILFM}}$ is designed to be 2.7 mA. Thus, shown in Fig. 7, the ILFM’s operation range of 2.4 GHz is enough wide to keep $f_{\text{PLL}}$ between its upper and lower boundaries $f_{\text{up}}$ and $f_{\text{low}}$.

**Figure 7.** The tuning characteristics of the PLL and ILFM.
Fig. 9 shows that the phase noises of $f_{PLL}$ and $f_{ILFM}$ are -110 dBc/Hz and -104 dBc/Hz at 1 MHz offset, respectively. The ILFM’s phase noise is almost 6 dB more than its input's because of doubling the frequency. That means the phase noise is almost not deteriorated by the ILFM. The simulation results has been summarized in Table 1 and compared with other work for the automotive radar application. The proposed circuit achieves very low power consumption and very good on other performance. Therefore, it is most applicable to generate a 24-GHz reference frequency for the automotive radar application.

### Table 1. The Performance Summary and Comparison

<table>
<thead>
<tr>
<th>Technology</th>
<th>[12] SiGe 130 nm BiCMOS</th>
<th>[13] 130 nm CMOS</th>
<th>This Work 130 nm CMOS</th>
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<tr>
<td>Supply Voltage</td>
<td>2.5</td>
<td>1.5</td>
<td>1.5</td>
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<tr>
<td>Output Freq. (GHz)</td>
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<td>24</td>
<td>24</td>
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<tr>
<td>Ref. Freq. (MHz)</td>
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<td>10</td>
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<td>Tuning Range</td>
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<td>15.8%</td>
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<tr>
<td>Phase Noise (dBc/Hz at 1 MHz)</td>
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<td>-101</td>
<td>-104</td>
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<td>$P_{dc}$ (mW)</td>
<td>70</td>
<td>88</td>
<td>9.3</td>
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**REFERENCES**


